Motor Control IP Design and Quality Evaluation from the Viewpoint of Reuse (ICCAS 2004)

Sang-Deok, Lee*, Sung-Ho, Han**, Min-Soo, Kim**, and Young-Jun, Park**

*Department of Mechatronics, Samsung Heavy Industries Co., Ltd., Daejeon, Korea
(Tel: +82-42-865-4671; Fax: +82-42-865-4688; E-mail: sdcontrol.lee@samsung.com,)
**Department of Mechatronics, Samsung Heavy Industries Co., Ltd., Daejeon, Korea
(E-mail: mountain.han@samsung.com, himinsoo.kim@samsung.com, pyjcruiser.park@samsung.com)

Abstract: In this paper we designed the motor control IP Core and evaluate its quality from the viewpoint of IP reuse. The most attractive merit of this methodology, so called IP-based hardware design, is hardware reuse. Although various vendors designed hardware with the same specification and got the same functional results, all that IPs is not the same quality in the reuse aspect. As tremendous calls for SoC have been increased, associated research about IP quality standard, VSIA(Virtual Socket Interface Alliance) and STARC(Semiconductor Technology Academic Research Center), has been doing best to make the IP quality evaluation system. And they made what conforms to objective IP design standard.

We suggest the methodology to evaluate our own designed motor control IP quality with this standard. To attain our goal, we designed motor control IP that could control the motor velocity and position with feedback compensation algorithm. This controller has some IP blocks : digital filter, quadrature decoder, position counter, motion compensator, and PWM generator. Each block's functionality was verified by simulator ModelSim and then its quality was evaluated. To evaluate the core, We use Vnavigator for lint test and ModelSim for coverage check. During lint process, We adapted the OpenMORE's rule based on RMM (Reuse Methodology Manual) and it could tell us our IP's quality in a manner of the scored value form. If it is high, its quality is also high, and vice versa. During coverage check ModelSim-SE is used for verifying how our test circuits cover designs. This objective methods using well-defined commercial coverage metrics could perform a quantitative analysis of simulation completeness.

In this manner, We evaluated the designed motor control IP's quality from the viewpoint of reuse. This methodology will save the time and cost in designing SoC that should integrate various IPs. In addition to this, It can be the guide for comparing the equally specified IP's quality. After all, we are continuously looking forward to enhancing our motor control IP in the aspect of not only functional perfection but also IP reuse to prepare for the SoC-Compliant motor control IP design.

Keywords: Motor Control IP, Lint, Coverage, IP Quality, IP Evaluation, SoC, FPGA, Motor Control IP

1. INTRODUCTION

As Increasing the call for the SoC and IP Trading system[1], Many concerns about the verification for Soft IP Core are also heading for the summit. VSIA(Virtual Socket Interface Alliance)[2] has announced the reusability of soft IP using well-defined verification methods.

In this paper, We made the sample motor control IP equipped with quadrature decoder which counts the revolutional pulse ratio of the motor and forms a loop-back system. This manner of controlling motor is very public in making the FPGA-based motor controller because of the easiness of configuring the hardware using HDL. But, SoC-Compliant IP core has an additional meaning. Just Synthesis of RTL code is not sufficient in that it requires more formal notification to the IP Consumer who make it a rule to verify its quality and then use it on a whole system.

This thesis will deal with the problem how can we verify the quality of the Soft IP from the viewpoint of Reuse. This IP quality evaluation method might be the important factor of verifying the quality of IP in developing the huge SoC-compliant system.

Firstly, We designed the sample IP which is including : DIGITAL FILTER, QEP DECODER, COUNTER REGISTER, QEP LATCH, DVA CALC, SUBTRACTOR, COMPENSATOR, PWM-TIMER. And simulate its functionality.

Second, We introduce the OpenMORE ratings which should support the IP users in deciding the most appropriate Core for integration in a system design. As mentioned at VSIA[2] and RMM(Reuse Methodology Manual)[3], there are already commercial tools which has an functionality in checking for the OpenMORE ratings. The results of these tools show the compliance of design guidelines and help the IP user to select an reliable IP. In this manner, Our motor control IP blocks could be evaluated. We suggest the methodology how we could evaluate the motor control IP using lint processor.

Code coverage is another important material in verifying the quality of Our own IP. We introduce coverage metrics that are often classified as code coverage. Sometimes, different names are used for similar types of coverage metrics. : Statement Coverage, Block Coverage, Decision Coverage, Path Coverage, Expression Coverage. These metrics use some special PLI(Programming Language Interface) routines of the HDL simulator to measure the execution statistics of the source code during simulation. Because the job of coverage measurement is to monitor the actions in a simulation, the supports from the simulator are necessary, So we use Modelsim-SE simulator for coverag.

In this manner, We evaluated the sample-designed motor control IP's quality from the viewpoint of reuse.

2. SAMPLE IP DESIGN : MOTOR CONTROL IP

To attain the goal of IP quality evaluation, most of all, We designed the sample IP Core which has a role to control DC motor. The specification includes :

- N : Encoder Pulses per revolution : 500 changes
- f(Hz) : Encoder Inertia of code disc : up to 100 KHz
- Velocity(rpm) : f(Hz)*60/N = 12000 rpm
- x4 Quadrature Decoding
- PPS(pulses/sec) : 12000/60*500*4 = 400000
- PPM(pulses/ms) : PPS/1000 = 400000/1000 = 400

- PWM Bandwidth : 10 bits
- System Clock : 8MHz
- PWM Frequency : 8000000/1024 ≅ 8KHz
- Encoder Sampling Rate : 1MHz
- Encoder Counter Latch Interrupt Interval : 1 KHz(1 ms)
- Motion Profile Command : 100 Hz (10ms)
- Speed Resolution : 0 ~ 400 Pulses/1(ms)
- Distance Resolution : 0 ~ 400 Pulses
- PID Compensator Resolution : 10 (turns) / Motion Profile Command

Encoder has a two phases (Phase-A, Phase-B) and during 1 revolution of the encoder respective phase has 500 turns state variation. x4 decoding will make 2000 pulses during one revolution. Over 100KHz sampling is required because encoder sampling rate can be decided by encoder code disc inertia-frequency. We designed 1MHz Quadrature Decoding block and this block needs clock divider which divide a system clock by 8 clock-cycles. Motion Profile Command can regenerate the destination velocity every 10 mili-second. During this interval, PID Compensator can produce the adequate command which is generated by Digital PID compensation algorithm. Distance, Velocity, and acceleration factors are counted every 1ms and then updated by 1 ms interval interrupt timer from QEP LATCH block. The Maximum count value during 1 ms are 400. If we change the interrupt timer interval, we can change the resolution of maximum motion variation figure during sampling interval. For example, If we adapt 10 ms then we get 4000 counts.

Table 1. RTL code of motor control IP

RTL /TESTBENCH	FUNCTION
TOP.VHD TB_TOP.VHD	Top level unit
DIGITAL_FILTER.VHD TB_DIGITAL_FILTER.VHD	Encode synchronize unit
QEP_DECODER.VHD TB_QEP_DECODER.VHD	Encoder decode unit
COUNTER_REG..VHD TB_COUNTER_REG.VHD	Encoder counter unit
QEP_LATCH.VHD TB_QEP_LATCH.VHD	Irq generator unit
DVA_CALC.VHD TB_DVA_CALC.VHD	Calculation unit
SUBT.VHD TB_SUBT.VHD	Error detection unit
COMPENSATOR.VHD TB_COMPENSATOR.VHD	PID filter unit
PWM.VHD TB_PWM.VHD	PWM timer unit

We, firstly, design the RTL(Register Transfer Level) code which is satisfactory with this specification. This Codes can be classified with source codes and testbench codes. We use VHDL language for hardware design language.

A. DITAL FILTER BLOCK : This block can eliminate the input phase noise of encoder. The optical shaft encoder would generate short duration noise spike during motor movement. Protection from this phenomena, Three-clock-cycle delay filter is used and this filter can eliminate the noise and enhance Noise rejection. Figure 1 shows the circuit and noise rejection. We designed this filter and simulate it.

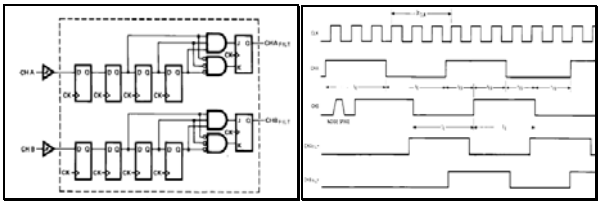


Fig 1. Simplified Digital Noise Filter Specification

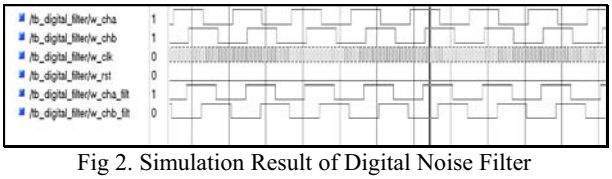


Fig 2. Simulation Result of Digital Noise Filter

B. QEP DECODER BLOCK : After digital noise filter, Encoder input phases should be decoded by QEP DECODER BLOCK. Through the state-machine which monitors the state of the phase, this block play a role to count up and down. For more exact counting for this state we adapt x4 decoding.

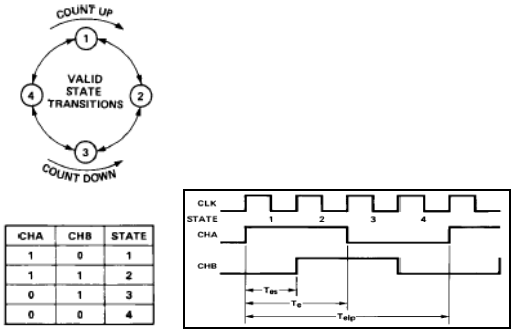


Fig 3. 4x Quadrature Decoder Specification

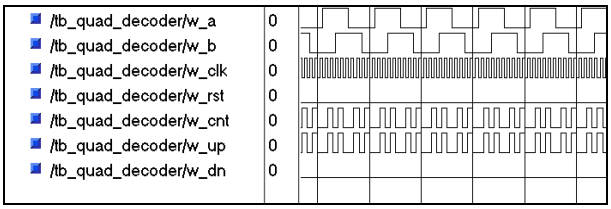


Fig 4. Simulation Result of Quadrature Deocder

We can get four counts every one transition as above waveform. During count up sequence, this circuit should trigger W_CNT and W_UP signal. And during count down sequence, trigger W_CNT and W_DN signal. We use 1MHz clock to satisfy the demand of encoder sampling rate.

C. COUNTER BLOCK : The information from QEP DECODER BLOCK is accumulated by the counter block. This block has register which can store the count pulses up to 8,589,934,591.

D. QEP LATCH BLOCK : one mili-second interval timer can latch counter block information. The maximum value of this information is integer 400. This data is used for calculation of Distance, Velocity, and Acceleration.

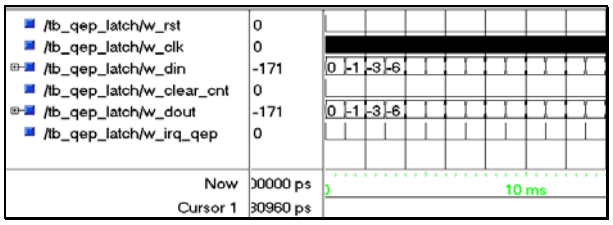


Fig 5. Simulation Result of Quadrature Deocder

W_IRQ_QEP signal is the interrupt signal which triggered one shot pulse per one mili-second. The data will be transferred by the rate of this resolution.

E. DVA_CACL BLOCK : This module calculates the current distance, velocity, acceleration of the encoder. There are two algorithms to find the velocity of sampling signal. One is a fixed sampling period, and the other is fixed position interval method. The former is a traditional method and we use it to calculate the velocity.

$$v(k) \cong \{x(k) - x(k-1)\} / T \quad (1)$$

$$v(k) \cong X / \{t(k) - t(k-1)\} \quad (2)$$

where

v is velocity
x is position
t is time
T is a fixed sampling period
X is a fixed position interval

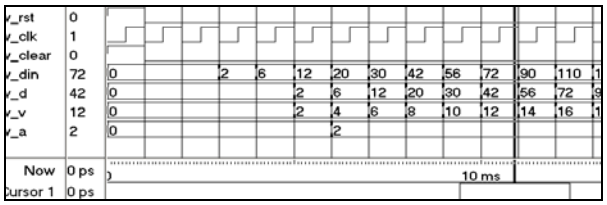


Fig 6. Simulation Result of DVA CALCULATION

F. Error Feedback Unit : Error Feeback Module produces the error term which will be the input of the compensation module. The error means the difference between destination value and actual value.

G. COMPENSATOR : Digital PID Compensation Filter can be formulated by this equation.

$$y[n] = y[n-1] + C_0 x[n] + C_1 x[n-1] + C_2 x[n-2] \quad (3)$$

Where C0, C1, C2 are tuning parameters combined with proportional gain term, Integral gain term, and derivative term. In this paper, we search for the proper value from simulation results. The block diagram shows how to design the hardware.

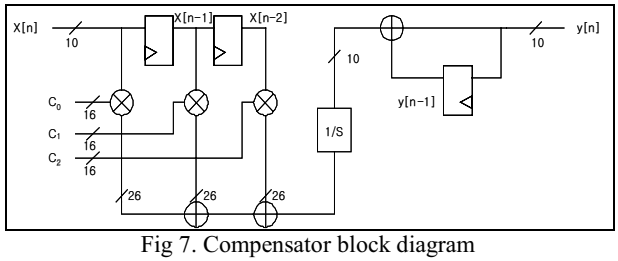


Fig 7. Compensator block diagram

H. PWM : In general, Pulse Width Modulation can keep the track of the motor speed. Because Motor has its own inertia moment, the average supply voltage is varying with pulse width. In this system, We use 8 KHz PWM frequency. According to w_data_value coming from PID compensator, motor speed will change

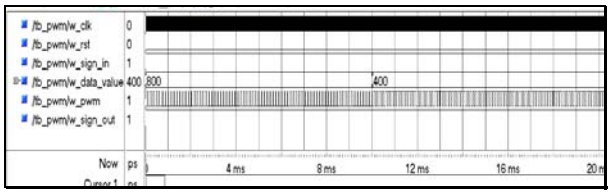


Fig 8. PWM Timer simulation result

I. TOP : Tob Level Block Diagram

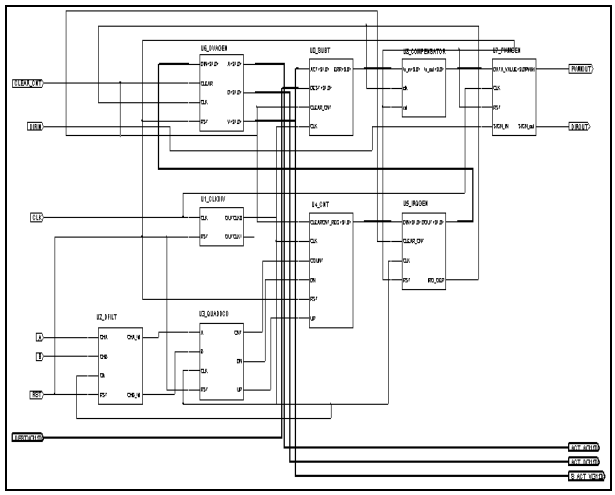


Fig 9. TOP Module

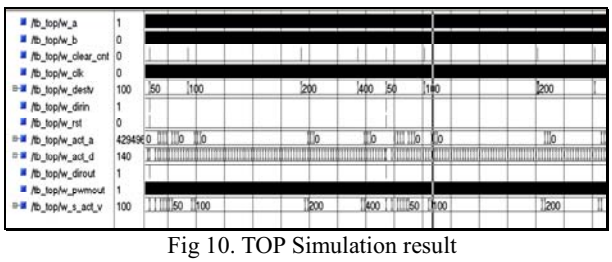
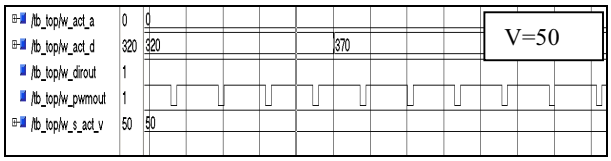
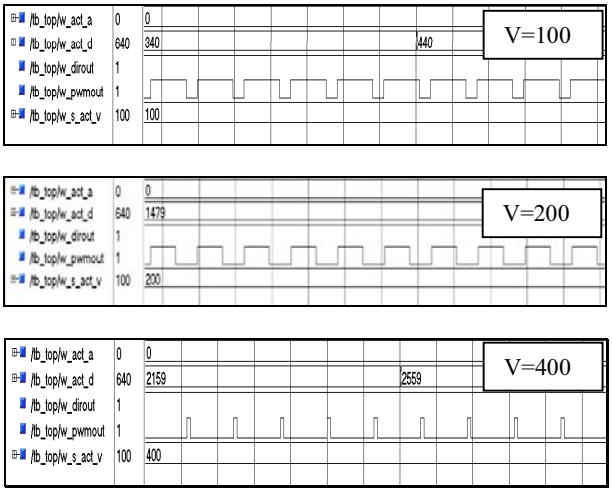


Fig 10. TOP Simulation result





This is the simulation how our top module conforms to velocity control. Fig 10 is the entire wave during simulation and below waves are detailed results.

3. IP QUALITY EVALUATION : LINT

Although various vendors designed hardware with the same specification and got the same functional results, all that IPs is not the same quality in the reuse aspect. But, the application of reusable IP has become a regular point of modern SoC design. The IP Quality evaluation keeps growing in this reason, and various researches have followed up. VSIA(Virtual Socket Interface Alliance)[2] and STARC(Semiconductor Technology Academic Research Center)[4] are the representative organizations for standardization of IP Qualify evaluation. And they made some standards like coding guideline and code check method like OpenMORE Assessment program. OpenMORE Assesment program is based on the Reuse Methodology Manual(RMM). This program is co-authored by Synopsys and Mentor Graphics. OpenMORE is based on over 150 rules and guidelines from the RMM[2] which are encapsulated into a weighted spreadsheet. Answering the rules and guidelines contained in OpenMORE spreadsheet for an IP core computes a weighted score. Based on the weighted score(%), a rating between 1 and 4 stars is assigned according to Table 2. OpenMORE has Coding rule, Style rule, Documentation rule, Naming rule, and User-define rule. And during lint process, these items are scored by sub-classified rule of respective rules. Fig 11 is the lint process picture.

Table 2. OpenMore Score

Weighted Score % (S)	Result
S < 60	
60 <= S <75	*
75 <= S <87	**
87 <= S < 95	***
95 <= S	****

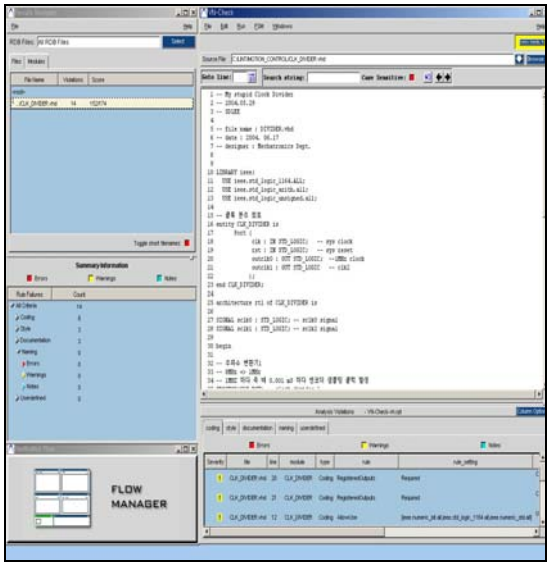


Fig 11. VN-Check Lint Process(Code Check)

Table 3. OpenMore Lint Results

IP SOURCE	(S)	Result
CLK_DIVIDER.VHD	87	***
COUNTER_REG.VHD	78	**
DIGITAL_FILTER.VHD	91	***
DVA_CALC.VHD	86	**
PID_COMPENSATOR.VHD	77	**
QEP_LATCH.VHD	85	**
QUAD_DECODER.VHD	83	**
PWM.VHD	86	**

Table 3 shows the result of lint process. The Result is not sufficient for a highly qualified IP. It must be upgraded to acquire a high score, or so high quality. But There is a meaningful point that we checked the code following the guidelines from VSIA which should be accounted for Qualified IP design.

4. IP Quality Evaluation : Coverage

In addition to the lint process, IP Quality should be checked from testbech's quality. The idea of coverage is originated from traditional software development methodology. IP Coverage means how testbench covers the source code. Nowadays, observability based coverage detection is studied to reinforce the controllability-based coverage methodology[11]. In this paper, we verify our IP based on functional coverage using ModelSim coverage tool from Mentor Graphics. This coverage includes :

- Statement and branch coverage, which provide a quick indication of verification progress
- Condition and path coverage, which are crucial in

situations where there are complex terms in branches or where there are consecutive decision blocks

- Toggle coverage, which identifies signals that have been inactive during a simulation
- Triggering coverage, based on the examination of the sensitivity lists in VHDL constructs
- Variable and signal trace coverage, useful for checking coverage of vector-based HDL representations.

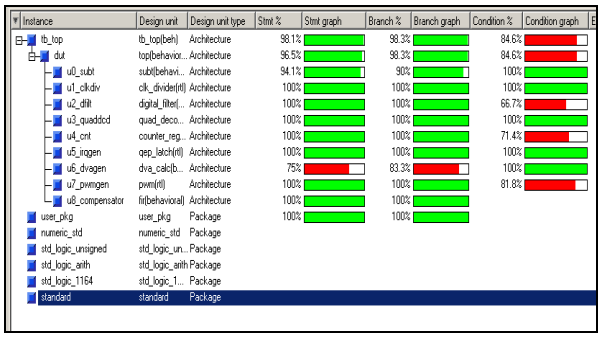


Fig 12. Coverage Result

We check for the coverage that how our test circuit covers the design source. In general, coverage means just a statement coverage. But branch coverage and condition coverage is also important.

Figure 12 shows how our test vector can cover design module. As depicted by graph, almost circuits are covered except for some uncovered parts. But, It is not difficult problem to correct it. Because we can observe the source code where there is an omitted phase during coverage.

5. RESULTS AND FUTURE WORK

As a result, We designed sample motor control IP Core and synthesized it and then evaluate its quality form the viewpoint of reuse.

Table 4. Synthesis Result

Macro Statics	Register	28
	Counter	2
	Multiplexers	2
	Adder/Subtractors	11
	Multipliers	3
	Comparators	4
Cell Usage	BELS	1220
	FlipFlops/Latchs	315
	Clock Buffers	1
	IO Buffers	135
	MULTs	3

The development configuration is :

- Development Language : VHDL
- Compiler : Xilinx ISE6.01 OEM.
- Functional simulation : ModelSim-XE5.7c
- Lint : TransEDA VN-Check eva.
- Coverage : ModelSim-SE Plus 5.8c

Though evaluation results are not sufficient for our expectation because of the shortage of design term, we think we will get a believable IP through quality evaluation. This is meaningful.

The verification problem of soft IP is keeping pace with progress in a field of IP reuse design. Moreover, Motion controller designed by Field Programmable Gate Array keeps growing in control area. So, the need for its quality evaluation is more and more important.

A new commit named SoC is coming as suddenly but there is not total solution because of its difficulty in verifying analog IP. Nevertheless, Digital solution for IP quality verification is continuously going on appearing.

In motion control applications, many robots needs SoC and motion control IP. We expect Qualified IP design is one of the most important element in developing such a control system.

To conclude, we are continuously looking forward to enhancing our motor control IP in the aspect of not only functional perfection but also IP reuse to prepare for the SoC-Compliant motor control IP design.

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