Multiplierless Digital PID Controller Using FPGA

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Abstract: This paper proposes a design and implementation of multiplierless digital PID (Proportional-Integral-Derivative) controller using FPGA (Field Programmable Gate Array) for controlling the speed of DC motor in digital system. The multiplierless PID structure is based on Distributed Arithmetic (DA). The DA is an efficient way to compute an inner product using partial products, each can be obtained by using look-up table. The PID controller is designed using MATLAB program to generate a set of coefficients associated with a desired controller characteristics. The controller coefficients are then included in VHDL (Very high speed integrated circuit Hardware Description Language) that implements the PID controller onto FPGA. MATLAB program is used to activate the PID controller, calculate and plot the time response of the control system. In addition, the hardware implementation uses VHDL and synthesis using FLEX10K Altera FPGA as target technology and use MAX+plusII program for overall development. Results in design are shown the speed performance and used area of FPGA. Finally, the experimental results can be shown when compared with the simulation results from MATLAB.

Keywords: PID Controller, Digital Control, Distributed Arithmetic FPGA

1. INTRODUCTION

Generally, an implementation of digital PID controller is widely used microprocessor or microcontroller which has disadvantage in speed of operations because the operations depend on software which has the sequence of operations and multiplication command needs many machine cycles for execute. Also, FPGA-based digital PID controller is proposed because the operations of FPGA are hardware concurrent operations. However, FPGA-based digital PID controller still needs multipliers for computation. These multipliers will decrease the speed of processing time since the multiplying stage is consumption process and use large silicon area in VLSI design. These multiplications can change to DA architecture, DA architecture was first proposed by Peled and Liu in 1974 [1]. The DA is a direct method for sum of products operations, partial products and can pre-compute by difference equation and stored in look-up table containing in memory, input signals can be used for addressing. The product can be computed by scaling accumulate of partial products from memory, therefore, the multipliers don't necessary for this method, the proposed digital PID controller will be multiplierless.

2. PRINCIPLE OF DIGITAL PID CONTROLLER

Considering a block diagram of the digital control system

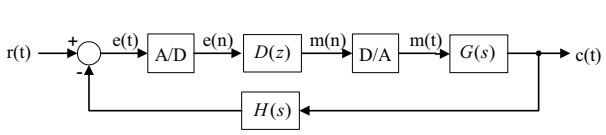

Fig.1 Block diagram of the digital control system

Fig.1, r(t) is the reference input or called set-point, c(t) is the control output, D(z) is the digital controller, G(s) is the plant transfer function and H(s) is the sensor transfer function. A digital PID controller can be derived as follows.

In continuous-time system, a transfers function for PID controller [2-3] is

$$m(t) = k_p e(t) + k_i \int e dt + k_d \frac{de}{dt} \tag{1}$$

Where

k_p is gain of proportional controller
k_i is gain of integral controller
k_d is gain of derivative controller
$e(t)$ is error signal
$m(t)$ is output signal

Use Laplace transform in equation (1) will give.

$$M(s) = k_p E(s) + \frac{k_i}{s} E(s) + k_d s \tag{2}$$

Also, the transfer function of PID controller is

$$D(s) = \frac{M(s)}{E(s)} = k_p E(s) + \frac{k_i}{s} E(s) + k_d s \tag{3}$$

Transform Eq.(3) to digital domain and will be obtained the transfer function of digital PID controller as follows.

$$D(z) = K_P + K_I \frac{T}{2}\frac{z+1}{z-1} + \frac{K_D}{T}\frac{z-1}{z} \tag{4}$$

Eq. (4) can be realized to be direct form I structure by

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \tag{5}$$

Normally, for digital PID controller $b_2 = 0$ and $b_1 = -1$ with

$$a_0 = K_P + \frac{K_I T}{2} + \frac{K_D}{T}$$

$$a_1 = -K_P + \frac{K_I T}{2} - \frac{2K_D}{T}$$

$$a_2 = \frac{K_D}{T}$$

Where K_P, K_I and K_D are the proportional, integral and derivative parameters of digital PID controller, and T is the sampling period. Fig.2 shows the direct form I structure of digital PID controller that correspond to Eq. (5).

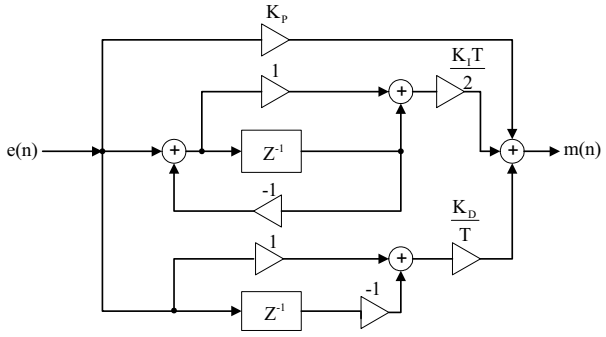

Fig.2 Direct form I structure of digital PID controller

3. ARCHITECTURE OF DIGITAL PID CONTROL BASED DA

Distributed Arithmetic (DA) is an efficient way to compute an inner product using partial products, each can be obtained by using look –up table method. Normally, DA used in may applications in digital signal processing [1, 4, 5]. For simple explanation, consider the second order linear difference equation as follow,

$$y(n)=\sum_{i=0}^{2}a_i x(n-i)-\sum_{j=1}^{2}b_j y(n-j) \tag{6}$$

Where x(n) and y(n) are the input and output signal respectively, a_i and b_j are constant coefficients.

Assuming all signals are bounded by ± 1 and define in two's complement format, B bit a curacy including sign bit by;

$$x(n)=\sum_{k=1}^{B-1}x_k(n)2^{-k}-x_0(n) \tag{7}$$

$$y(n)=\sum_{k=1}^{B-1}y_k(n)2^{-k}-y_0(k) \tag{8}$$

This Eq. (6) can be rewritten as

$$\begin{aligned}y(n)=&\sum_{i=0}^{2}a_i[\sum_{k=1}^{B-1}x_k(n-i)2^{-k}-x_0(n-i)]\\&-\sum_{j=0}^{2}b_j[\sum_{k=1}^{B-1}y_k(n-j)2^{-k}-y_0(n-j)]\end{aligned} \tag{9}$$

Rearrange the summation in Eq. (9) yields.

$$\begin{aligned}y(n)=&\sum_{k=1}^{B-1}[\sum_{i=0}^{2}a_i\cdot x_k(n-i)2^{-k}-\sum_{i=0}^{2}a_i\cdot x_0(n-i)]\\&-\sum_{k=1}^{B-1}[\sum_{i=1}^{2}b_j\cdot y_k(n-i)2^{-k}-\sum_{j=1}^{2}b_j\cdot y_0(n-j)]\\=&\sum_{k=1}^{B-1}[\sum_{i=0}^{2}a_i\cdot x_k(n-i)-\sum_{j=1}^{2}b_j\cdot y_k(n-j)]2^{-k}\\&-[\sum_{i=0}^{2}a_i\cdot x_0(n-i)-\sum_{j=1}^{2}b_j\cdot y_0(n-j)]\end{aligned} \tag{10}$$

Define the function $F(\cdot)$ as follow,

$$\begin{aligned}F_k=&(x_k(n),x_k(n-1),x_k(n-2),y_k(n-1),y_k(n-2))=\\&a_0x_k(n)+a_1x_k(n-1)+a_2x_k(n-2)\\&+b_1y_k(n-1)-b_2y_k(n-2)\end{aligned} \tag{11}$$

Since each $x_k(n-i)$ and $y_k(n-j)$ where k=0,1,…,B-1 is only 0 or 1, we also pre-compute the values of this function that called partial products stored in memory such as ROM and using the input signals and feedback output signals for addressing. Therefore, the output can be computed by shifting and adding of partial products as follow in Eq. (12),

$$y(n)=\sum_{k=1}^{B-1}F_k(\cdot)2^{-k}-F_0(\cdot) \tag{12}$$

This equation can be realized to be hardware by using the distributed arithmetic and be shown that multipliers have not used in this structure as shown in Fig. 3.

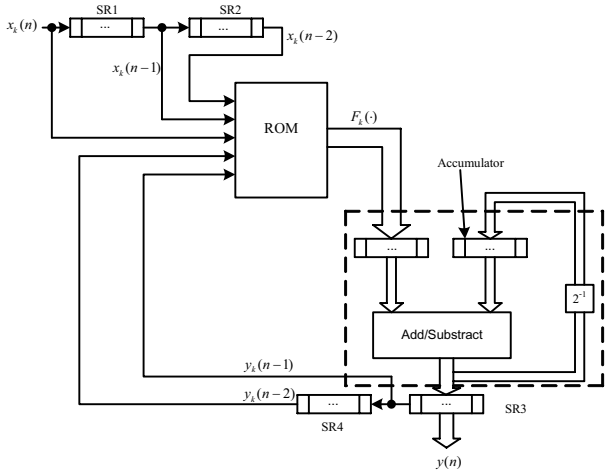

Fig.3 Architecture of 2^{nd} difference equation operations based DA

The operation can be described as follow,

1. Clear all data in accumulator registor
2. Compute $F_k(\cdot)$ for k=B-1 by look-up table
3. adding $F_k(\cdot)$ value with value in accumulator
4. shift right data in accumulator 1 bit
5. repeat in 2-4 for k=B-2,…,1
6. compute $F_0(\cdot)$
7. subtract $F_0(\cdot)$ value form value in accumulator

The proposed digital PID controller can be realized with the same scheme. From Eq. (5) and Fig. 2 can be obtained

$$D(z)=\frac{M(z)}{E(z)}=\frac{a_0+a_1z^{-1}+a_2z^{-2}}{1-z^{-1}}$$

Take inverse z-transform and derive into difference equation it will give

$$m(n)=a_0e(n)+a_1e(n-1)+a_2e(n-2)+m(n-1) \tag{13}$$

In experiment, the speed control of DC motor will be performed. The plant is DC motor, a tachometer as the speed sensor. The transfer function of this motor is

$$G(s)=\frac{20}{s+4} \tag{14}$$

The speed sensor has a ratio of 0.2, the input signal was 100 mV, representing a desired output speed of 12.5 rps or 750 rpm. The PID parameters for this required output speed are $k_P=0.75$, $k_I=4.75$ and $k_D=0$. It corresponds to $a_0=0.7502$, $a_1=-0.7498$ and $a_2=0$ by using sampling frequency 10 kHz or T = 0.0001 s. Also, Eq. (13) can be reduced to

$$m(n)=a_0e(n)+a_1e(n-1)+m(n-1) \tag{15}$$

All of possible values containing in ROM equal to 8 values, each value will be convert to 16 bit two's complement format before stored in ROM, addresses for tapping ROM come form sequence of bit level inputs $e_k(n)$, $e_k(n-1)$ and $m_k(n-1)$ respectively. Table 1 shows evaluation of values contention ROM

Table 1 Evaluation of values content in ROM

Address			Values contention In ROM
0	0	0	0
0	0	1	1
0	1	0	a_1
0	1	1	a_1+1
1	0	0	a_0
1	0	1	a_0+1
1	1	0	a_0+a_1
1	1	1	a_0+a_1+1

Also, the proposed multiplierless digital PID controller can be shown in Fig. 4

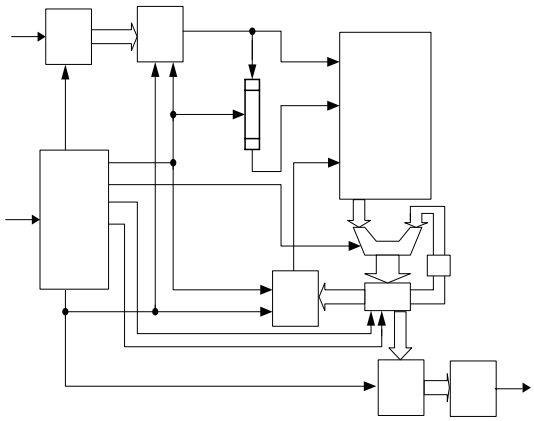

Fig. 4 Architecture of proposed multiplierless digital PID controller

The operation can be described by 5 steps as follow;

1. A/D that controlled by signal ***sc*** will be converted analog signal e(t) to 8 bit digital signal e(n)
2. signal ***lr*** will be loaded input data to PISO (parallel in serial out shift register)
3. signal ***clk*** will be shifted data in each shift register, output of each shift register used for each ROM addressing, output of ROM will be accumulated by scaling accumulator that control by signal ***s/a***, results will be loaded to ACC by signal ***lacc***.
4. ***clk*** will be shifted continue and repeat in step 3 until shift to last bit, output of ROM will be subtracted form ACC, the results will be loaded to buffer by signal ***lr*** for D/A
5. clear ACC using signal ***clacc*** and repeat in step 1-5, respectively.

The timing diagram of control unit is used for the proposed hardware architecture can be shown in Fig. 5.

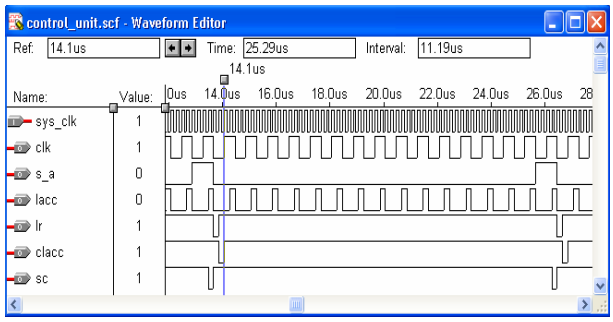

Fig.5 Timing diagram of control unit

4. SYNTHESIS AND EXPERIMENTAL RESULTS

An EPF10K10LC84-4 device in FLEX10K device family used for circuit synthesis. Device summary of multiplierless digital PID controller is shown in Fig. 6

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** DEVICE SUMMARY **

Chip/                          Input Output Bidir  Memory  Memory            LCs
POF      Device                Pins  Pins   Pins   Bits %  Utilized  LCs  % Utilized

pid      EPF10K10LC84-4        17    17     0      128       2  %    228      39 %

User Pins:                     17    17     0
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Fig. 6 Device Summary

From device summary, 17 input pins used for 16 bit input data and one for system clock, 17 output pin for 16 bit output data and one for signal ***sc***, 128 memory bits used for implementing ROM. Others component which using VHDL for design will use 228 LCs (logic cells) for implementing. Timing summary shows the maximum frequency of synthesized circuits is show in Fig. 7.

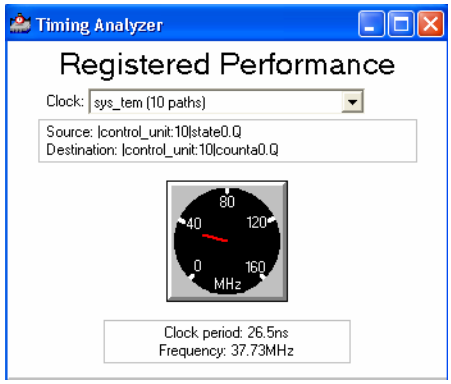

Fig. 7 Timing Summary

For experiment, the first test was to run the motor without controller. The output speed was only about half of the desired output is about 6.25 rps or 375 rpm. Fig. 7 shows the simulation result and Fig. 8 shows the experimental result.

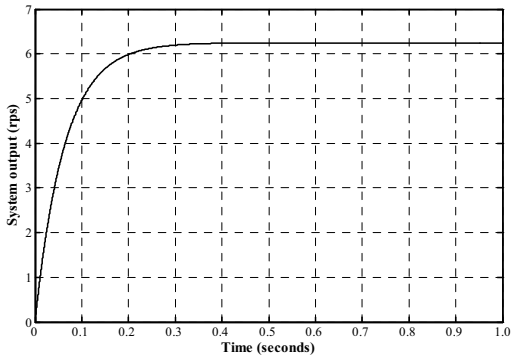

Fig.7 Simulation result in case of without controller

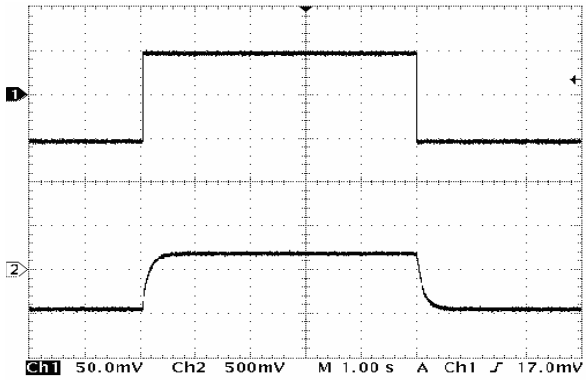

Fig. 8 Experiment result in case of without controller

Fig.8, motor speed at 375 rpm corresponding with output voltage about 750 mV. Fig. 9 and Fig. 10 shows the simulation result and experimental result of the second test that performed with a proposed multiplierless digital PID controller added.

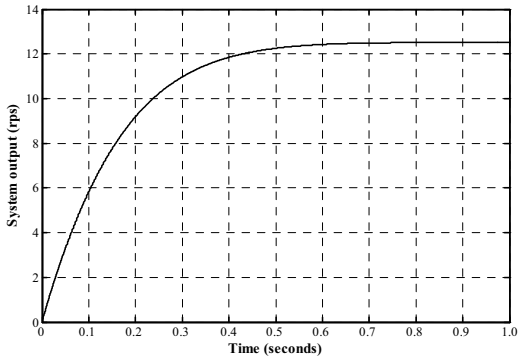

Fig. 9 Simulation result in case of with controller

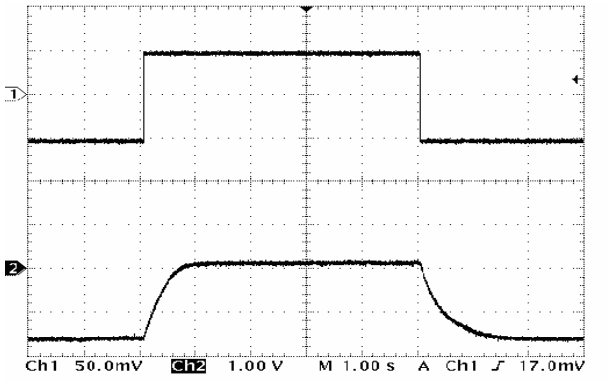

Fig. 10 Experimental result in case of with controller

Fig. 9, this achieved a steady state output speed of 750 rpm as desired output speed which its about 2 times of the first test. Also, the motor speed at 750 rpm will be corresponded to output voltage about 1.5V as shown in Fig. 10. However, the rise-time is longer with the controller added. The rise-time can be reduced by increasing K_I but it possible to have an overshoot.

5. CONCLUSION

The proposed method in this paper can obtain the multiplierless digital PID controller using distributed arithmetic realization, The hardware is satiable for implementing on FPGA, high processing speed and reduce power consumption when compared with using discrete components in implementation. Form experimental results when compared with simulation results, it can be ensured that the proposed hardware can operated correctly.

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