Digital Control of UPS Inverter with Time Response Specifications

Young-Tae Woo*, and Young-Chol Kim**

* Department of Electronics Eng., Chungbuk National University, Cheong-ju, Korea
(Tel : +82-43-261-2475; E-mail: wytnice@hanmail.net)
**School of Elec. & Computer Eng., Chungbuk National University, Cheong-ju, Korea
(Tel : +81-43-261-2475; E-mail: yckim@cbu.ac.kr)

Abstract: This paper presents two approaches for designing a digital controller of UPS inverter with time response requirements and a fixed sampling time, which are inward and outward approaches based on a double loop feedback structure. In both approaches, the emulation method. is occupied. Thus we first design continuous-time controllers and then obtain digital controllers by using discretization. We apply the characteristic ratio assignment (CRA) in order to achieve the time response specifications. Also, the internal model control has been used for compensating phase delay in outward approach. The performances of the proposed controller are evaluated through several simulations carried out with Simpower system toolbox 3.0 of Simulink®.

Keywords: UPS inverter, Inward approach, Outward approach, Digital control, CRA

1. INTRODUCTION

In most modern UPS inverters, the system requires the controller which results in the following performances: maintaining the desired output voltage waveform, faster response, and lower total harmonic distortion (THD) over all loading conditions. Several different methods for the purpose of these objectives have been presented [1]. However, there are few constructive methods that are applicable to the controller design problems for which time response requirements shall be satisfied. In addition, the inverter systems with feedback controller are generally constructed in the form of double loop feedback. The latter consists of a current feedback loop as an inner loop and a voltage feedback one as an outer loop, respectively. Each loop has its compensator. One of difficult problems associated with this control structure is caused by the fact that two loops are closely interconnected. This means that each controller in two loops can not be designed independently. Another problem may occur in a fixed sampling time when a digital controller is implemented. It is well known that the lower sampling rate used to be a constraint that one can not make the speed of response faster than a certain value as long as the digital controller is determined by the emulation method. In many cases, the digital controller for UPS inverter must be designed under a previously given sampling time because of the cost. Also, it is limited by the switching frequency of PWM inverter.

In this paper, we present two different design approaches for the digital controller of a single phase UPS inverter. The specifications to be considered are to maintain THD lesser than 5%, small overshoot against the abrupt load change (e.g. the case of that the full load is applied from no load state at the peak phase of output voltage), to have fast step response. The sample frequencies for the PWM inverter and the controller are 8 kHz here. The performance evaluations of the resulting system are conducted under the conditions of no load and a resistive load of 10[kW]. Digital control design is dealt with by means of either the discrete design or the emulation. In this paper, only the emulation method is dealt with. In other word, we first design a continuous time controller for a continuous time plant and then make the discretization of the controller with the previous given sample time. The weakest point of this method is that its fidelity depends on the sample rate and on the discretization methods. But it has a big advantage that one can apply sufficient design methods developed for continuous time linear systems. The design approaches that we consider here are as follows: (1) inward approach and (2) outward approach based on a double loop feedback structure.

For the two approaches, the orders of each controller in the individual loop, which has been properly selected a priori, are equal to or lesser than 2. Also, the time delay effect due to zero-order holder and processing time is modeled in the loop when the continuous time controller is designed. In the inward approach, all controllers in both inner and outer loops are designed simultaneously so as to meet the performances as well as stability of overall system. But one must examine whether the dynamics of the resulting inner loop has proper time response characteristics. If the response is too fast compared with the sampling rate, the digital implementation of such a controller may lose the stability. In outward approach, the design process is divided into two steps: the inner loop controller is first determined and then designs the outer loop controller. In all two approaches above, we introduce the characteristic ratio assignment (CRA) [2] to achieve the time response requirements.

This paper consists of four main parts. Section 2 provides the mathematical model of UPS inverter and its system parameters. Additionally, the theoretical backgrounds on the design method (CRA) are introduced. Section 3 presents the procedure of designing a digital controller by way of inward and outward approach. In section 4, the performances of the proposed controllers are evaluated through the simulation results carried out with Simpower system toolbox 3.0 of Simulink®. Finally, the concluding remarks are drawn in section 5.

2. UPS INVERTER MODEL AND CRA

In this section, to design a digital controller, the model of UPS inverter is built up and described as a transfer function. Also the system parameters in this configuration and some theoretical backgrounds on the CRA are given.

2.1 Basic configuration of UPS inverter

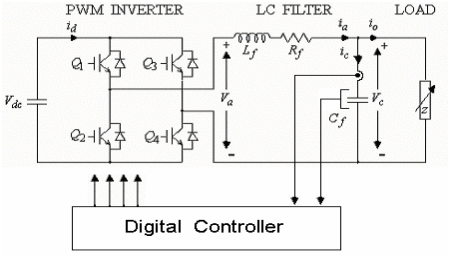

Fig. 1 Configuration of UPS inverter system

Fig. 1 shows the basic configuration of a single-phase UPS inverter system. From Fig. 1, we can draw the block diagram for UPS inverter system as shown in Fig. 2. To model this plant, we consider the feedback variables as the capacitor current i_c and the capacitor voltage V_c.

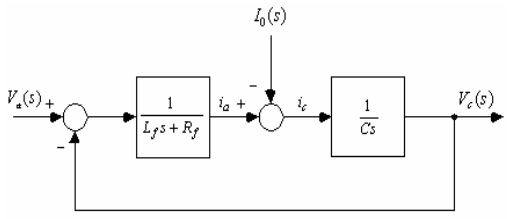

Fig. 2 Block diagram of UPS inverter

Then the transfer function from $V_a(s)$ and $I_o(s)$ to $V_c(s)$ is expressed by

$$V_c(s)=\frac{1}{L_fC_fs^2+R_fC_fs+1}V_a(s)-\frac{L_fs+R_f}{L_fC_fs^2+R_fC_fs+1}I_o(s). \quad (1)$$

Also we have the following transfer functions for inner loop $G_I(s)$ and outer loop $G_O(s)$.

$$G_I(s)=\frac{I_c(s)}{V_a(s)}=\frac{C_fs}{L_fC_fs^2+R_fC_fs+1}, \quad (2)$$

$$G_O(s)=\frac{V_c(s)}{V_a(s)}=\frac{1}{L_fC_f(s)s^2+R_fC_fs+1}. \quad (3)$$

In the frame of the digital control scheme for UPS inverter, the following system parameters in Table.1 are commonly used through the proposed two approaches.

Table.1 System parameters

System parameters		Values
Filter	Filter inductance (L_f)	200 $[\mu H]$
	Filter resistance (R_f)	0.08 [Ω]
	Filter capacitance (C_f)	120 $[\mu F]$
Input voltage $(V_c^*(t))$		±150[V]
DC-link (V_{dc})		270[V]
IGBT's switching frequency (f_{switch})		8[kHz]
Sampling frequency (f_s)		8[kHz]

2.2 Theoretical backgrounds on CRA

A. Definitions

Let us consider a real characteristic polynomial as follows:

$$\delta(s)=a_ns^n+a_{n-1}s^{n-1}+\cdots+a_1s+a_0,\ \forall a_i>0. \quad (4)$$

Herein, we define characteristic ratios as:

$$\alpha_1:=\frac{a_1^2}{a_0a_2},\ \alpha_2:=\frac{a_2^2}{a_1a_3},\cdots,\ \alpha_{n-1}:=\frac{a_{n-1}^2}{a_{n-1}a_n}, \quad (5)$$

and the generalized time constant as:

$$\tau:=\frac{a_1}{a_0}. \quad (6)$$

Then the coefficients a_i of $\delta(s)$ can be represented in terms of α_i s and τ as follows:

$$a_1=a_0\tau, \quad (7)$$

$$a_i=\frac{a_0\tau^i}{\alpha_{i-1}\alpha_{i-2}^2\alpha_{i-3}^3\cdots\alpha_2^{i-2}\alpha_1^{i-1}},\ i=2,3,\cdots,n. \quad (8)$$

It is evident that the corresponding polynomial $\delta(s)$ can be completely rewritten as a given set of values α_i s, τ and a_0. τ is related to the speed of time response of $\delta(s)$. And α_i s are related to the damping and stability [2]. With these results, we can expand the properties of α_i to an all-pole transfer function.

Theorem 1 [2] Let $G(s)$ be an all-pole transfer function:

$$G(s)=\frac{a_0}{\delta(s)}=\frac{a_0}{a_ns_n+\cdots+a_1s+a_0},\ a_i>0$$

and let α_i be the characteristic ratios of $\delta(s)$. Then

1) the frequency magnitude function $|G(j\omega)|$ is monotonically decreasing and

2) $\delta(s)$ is Hurwitz:

If the following two conditions hold:

A) $\alpha_1>2$;

B) $\alpha_k=\dfrac{\sin(\frac{k\pi}{n})+\sin(\frac{\pi}{n})}{2\sin(\frac{k\pi}{n})}\cdot\alpha_1$, for $k=2,3,\cdots,n-1$.

Theorem 1 shows how to construct an all-pole stable transfer function whose magnitude is monotonically decreasing. The construction mechanism involves only α_1 which we require to be greater than 2. Thus, this result allows us to characterize the reference all-pole systems by adjusting a single parameter α_1 to achieve the desired damping. Since the generalized time constant τ can be chosen independently of α_i, the coefficients of $\delta(s)$ are calculated as follows: For arbitrary a_0 and τ

$$a_1=\tau a_0, \quad (9)$$

$$a_i=\frac{\tau^ia_0}{\alpha_{i-1}\alpha_{i-2}^2\alpha_{i-3}^3\cdots\alpha_1^{i-1}},\ \text{for}\ i=2,3,\cdots,n. \quad (10)$$

It is seen that the larger α_1 values to $\alpha_1>2$ correspond to greater damping in all-pole transfer functions. Fig. 3 shows the relation on overshoot with respect to α_1.

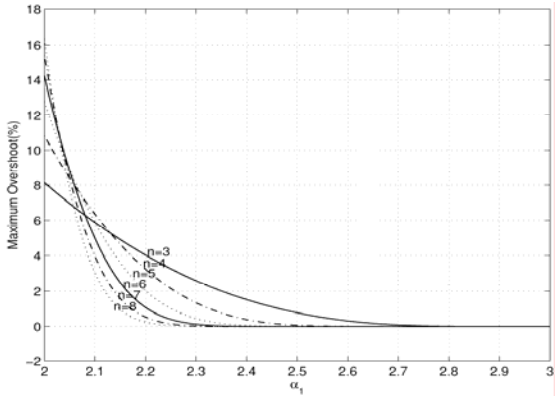

Fig. 3 Relationship between overshoot and α_1

B. Stability conditions in terms of α_i

The sufficient conditions for Hurwitz stable and unstable, which are translated in terms of α_i are as follows:

Theorem 2 [3] $\delta(s)$ is stable if

$$\sqrt{\alpha_i \alpha_{i+1}} > 1.4656 \text{ for } i = 1,2,\cdots,n-2. \tag{11}$$

Theorem 3 [3] $\delta(s)$ is stable if

$$\alpha_i > 1.2374\alpha_i^* \text{ for } i = 2,3,\cdots,n-2 \tag{12}$$

Theorem 4 [3] $\delta(s)$ is unstable if

$$\alpha_i \alpha_i^* < 1 \text{ for } i = 1,2,\cdots,n-2 \tag{13}$$

3. DIGITAL CONTROLLER DESIGN

In this section, we design each continuous controller using the proposed two approaches, the order of each controller in the individual loop, which has been properly selected a priori, are equal to or lesser than 2. Also, the time delay effect due to zero-order holder and processing time is modeled in the loop when the continuous time controller is designed. In last, the designed continuous-time controller is discretized by applying Tustin approximation.

3.1 Digital Controller Design by Inward Approach

In the inward approach, all proposed controllers in both inner and outer loops are designed simultaneously so as to meet the performances as well as stability of overall system. Also the configuration, called the two-parameter configuration is used in each loop. It implies that the effect on adding 'zero' onto overall transfer function of the closed loop does not exist. The time response characteristics of inner loop and its relation to the sampling rate are taken into consideration. Fig. 4 shows the proposed control scheme for inward approach.

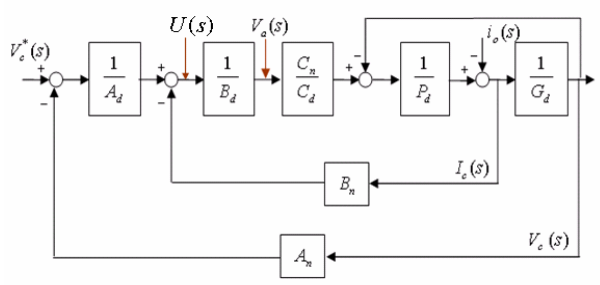

Fig. 4 Block diagram of the Inward approach controller

The structure of the proposed controller is considered as follows:

$$\begin{aligned} A_n &= b_1 s + b_0, & C_n &= 1 - \frac{3T_s}{4}s, \\ A_d &= s, & C_d &= 1 + \frac{3T_s}{4}s, \\ B_n &= a_1 s + a_0, & G_d &= C_f s, \\ B_d &= s + a_0, & P_d &= L_f s + R_f. \end{aligned} \tag{14}$$

In (14), T_s denotes the sampling time and $\frac{C_n}{C_d}$ is added in order to cover the time delay effect of zero-order holder when the continuous controller is discretized. Basically, the structure of (14) is PI controller. Then the transfer function of the closed-loop system is expressed by

$$\begin{aligned} V_c(s) &= \frac{C_n}{(G_d P_d B_d C_d A_d + G_d A_d C_n B_n + C_n A_n + C_n A_n + B_d C_d A_d)} V_c^*(s) \\ &= \frac{P_d B_d C_d A_d}{(G_d P_d B_d C_d A_d + G_d A_d C_n B_n + C_n A_n + C_n A_n + B_d C_d A_d)} I_0(s). \end{aligned} \tag{15}$$

Substituting (14) into (15), the characteristic polynomial is given by

$$\begin{aligned} \delta(s) = {} & \frac{3C_f L_f T_s}{4}s^5 + \left(-\frac{3C_f T_s a_1}{4} + \frac{3C_f L_f a_0 T_s}{4} + \frac{3C_f R_f T_s}{4} + C_f L_f\right)s^4 \\ & + \left(C_f a_1 - \frac{3C_f T_s a_0}{4} + \frac{3T_s}{4} + C_f R_f + \frac{3C_f R_f a_0 T_s}{4} + C_f L_f a_0\right)s^3 \\ & + \left(C_f R_f a_0 + 1 + \frac{3T_s a_0}{4} + C_f a_0 - \frac{3T_s b_1}{4}\right)s^2 + \left(b_1 - \frac{3T_s b_0}{4} + a_0\right)s + b_0. \end{aligned} \tag{16}$$

Next, we set the target polynomial of overall system by choosing $\alpha = 2.8$ and $\tau = 390\mu[\text{sec}]$.

$$\begin{aligned} \delta^*(s) = {} & 2.4\times10^{-8}\,s^5 + 2.48\times10^{-3}\,s^4 + 91.21s^3 + 1.48\times10^{6}\,s^2 \\ & + 1.06\times10^{10}\,s + 2.73\times10^{13} \end{aligned} \tag{17}$$

Then the control gains are determined from the algebraic relation between (16) and (17) as follows:

$$\begin{bmatrix} b_1 \\ b_2 \\ a_1 \\ a_2 \end{bmatrix} = \begin{bmatrix} -2.36\times10^4 \\ 2.35\times10^7 \\ 1.51 \\ 5.46\times10^4 \end{bmatrix}. \tag{18}$$

Fig. 5 shows Simulink® block of the implemented voltage loop controller. Also Fig. 6 shows the implemented current loop controller.

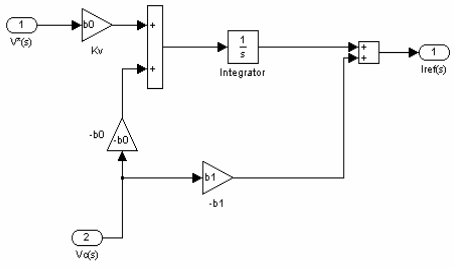

Fig. 5 The implemented voltage loop controller

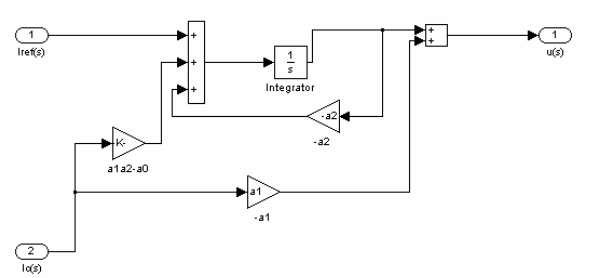

Fig. 6 The implemented current loop controller

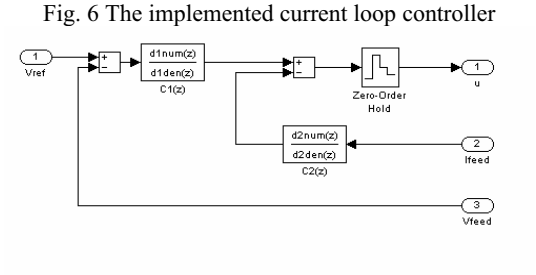

Fig. 7 The implemented digital controller

Lastly, by applying the digitization as Tustin approximation to the designed continuous-time controller, the digital controller is given by

$$C_{inner,inward}(z) = \frac{1.13z + 0.44}{z + 0.54}, \quad (19)$$

$$C_{outer,inward}(z) = \frac{-0.32z^2 + 0.04z + 0.36}{z^2 - 0.46z - 0.54}. \quad (20)$$

Fig. 7 shows the implemented digital controller by inward approach.

3.2 Digital Controller Design by Outward Approach

In outward approach, the design process consists of two main steps: the inner loop controller is first determined and then designs the outer loop controller.

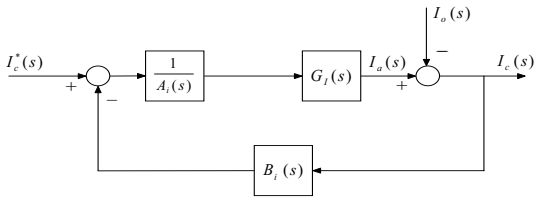

Fig. 8 Block diagram of the current loop controller

As the first step, we design the controller for inner loop $G_I(s)$ to reject the disturbances. This means that the overall transfer function of inner loop should have a fast speed of step response. Fig. 8 shows the proposed current loop control scheme for outward approach. And the structure of the proposed controller is considered as follows:

$$A_i(s) = s + x_3^i, \qquad B_i(s) = x_1^i s + x_2^i. \quad (21)$$

From Fig. 8, the transfer function of inner loop is expressed by

$$G_T(s) = \frac{I_c(s)}{I_c^*(s)} = \frac{C_f s}{(s + x_3^i)(L_f C_f s^2 + R_f C_f s + 1) + (x_1^i s + x_2^i) C_f s}. \quad (22)$$

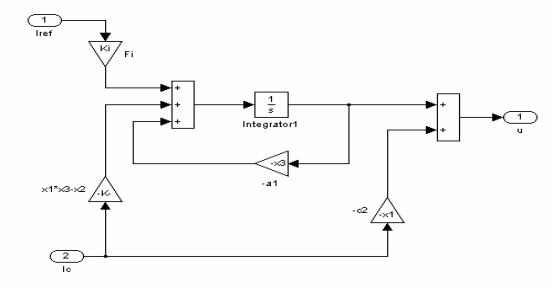

Fig. 9 The implemented current loop controller

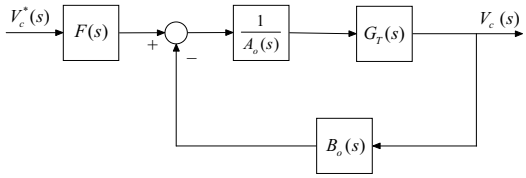

Fig. 10 Block diagram of the voltage loop controller

Let us set the target polynomial of inner loop by choosing $x_3^i = 384000$, $[\alpha_1 \quad \alpha_2] = [5 \quad 10]$ and $\tau = 2.5 * 10^{-4}$.

$$\delta_i(s) = 2.4\times10^{-8}s^3 + 4.8\times10^{-3}s^2 + 5.9\times10s + 1.1\times10^6 \quad (23)$$

The control gains of inner loop are determined from the relation between (22) and (23) as follows:

$$[x_3^i \quad x_2^i \quad x_1^i] = [384000 \quad 760946 \quad -36.88]. \quad (24)$$

Fig. 9 shows the implemented current loop controller.

Next, we design the controller for outer loop $G_T(s)$ as shown in Fig. 10. IMC (Internal Model Control) scheme is used for the robust voltage tracking. The proposed voltage controller is considered as follows:

$$A_o(s) = s^2 + 2\zeta\omega_n s + \omega_n^2, \quad B_o(s) = x_1^0 s + x_2^0, \quad (25)$$

where $\zeta = 0.3$ and $\omega_n = 120 * \pi$.

The values of ζ and ω_n in (25) are predetermined with the consideration of the characteristics of input signal. Then the overall transfer function of outer loop including $G_T(s)$ can be expressed by

$$G_{OT}(s) = \frac{V_c(s)}{I_o^*(s)} = \frac{1}{(s + x_3^i)(L_f C_f s^2 + R_f C_f s + 1) + (x_1^i s + x_2^i) C_f s}. \quad (26)$$

With the given condition of ζ and ω_n, we choose α_i, τ as

$$[\alpha_1 \quad \alpha_2 \quad \alpha_3 \quad \alpha_4] = [2.5 \quad 2 \quad 4.83 \quad 9.91], \tau = 8.333 * 10^{-4}. \quad (27)$$

Using (27), we set the target polynomial as

$$\delta_v(s) = 2.4*10^{-8}s^3 + 1.08*10^2 s^2 + 9.47*10^3 s + 3.84*10^4. \quad (28)$$

Then the control gains of outer loop are determined from (26) and (28) as follows:

$$[x_2^0 \quad x_1^0] = [78896853 \quad 900006]. \quad (29)$$

Finally, the digital controller is given by

$$C_{inner,outward}(z) = \frac{-2.34z + 5.86}{z + 0.78}, \quad (30)$$

$$C_{outer,outward}(z) = \frac{0.036z^3 + 0.037z^2 - 0.03z - 0.04}{z^3 - 1.21z^2 - 0.56z + 0.77}. \quad (31)$$

Fig. 11 shows the implemented digital controller by outward approach.

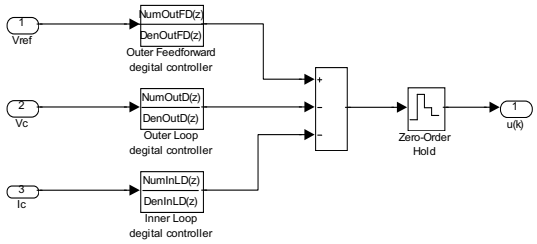

Fig. 11 The implemented digital controller

4. SIMULATION RESULTS

To evaluate the performance of the proposed controller, several simulations are carried out with Simpower system toolbox 3.0 of Simulink®. Fig. 12 shows the common UPS inverter system with the proposed controller. The simulations are conducted under two load conditions as follows: (1) no load, (2) a resistive load of 10[kW].

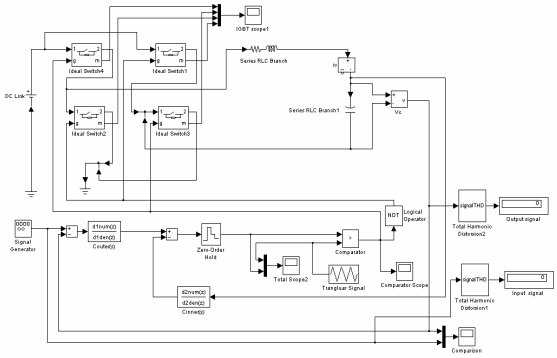

Fig. 12 UPS inverter system with the proposed controller

In the Simulink block of Fig. 12, the parameters of IGBT used are as follows:

Initial state: open, $R_{snubber} = 0.1[\Omega]$,

$R_{on} = 0.01[\Omega]$, $C_{snubber} = 0.22[\mu F]$.

Under no load change, Fig. 13 shows the output response of UPS system by inward approach. The result shows that the proposed controller gives the low steady-state error but has the phase delay effect of output signal. The THD of the response was about 4.7%.

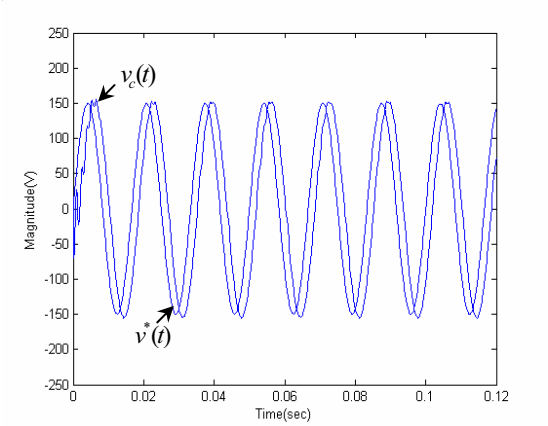

Fig. 13 Output response under no load (Inward Approach)

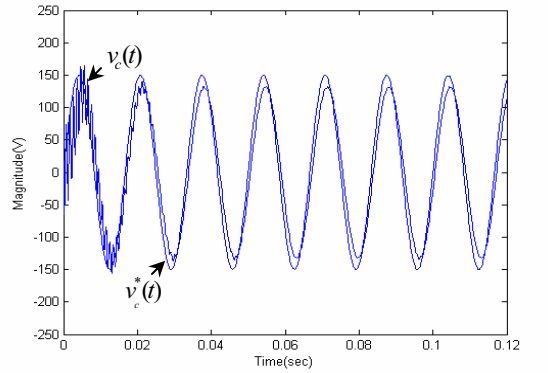

Fig. 14 Output response under no load (Outward Approach)

On the other hand, Fig. 14 shows the output response by outward approach. The THD of the response was about 4.99%. This means that the proposed controller eliminates the phase delay effect but has relatively a high steady-state error. In both approaches, the steady-state error and phase delay effects are inversely proportional to each other.

As the second load condition, a 10[kW] resistive load is abruptly applied at the peak phase (around $t = 0.0037$ sec). This is for the examination on how large the overshoot occurs and how fast the controller responds. Under a linear load change, Fig. 15 shows the output response by inward approach. In this case, the THD is about 4.4%. And Fig. 16 shows the output response by outward approach. The THD is about 4.9%. It is seen that the both proposed controllers satisfy the given time response requirements and the step change has been settled down within one and half period.

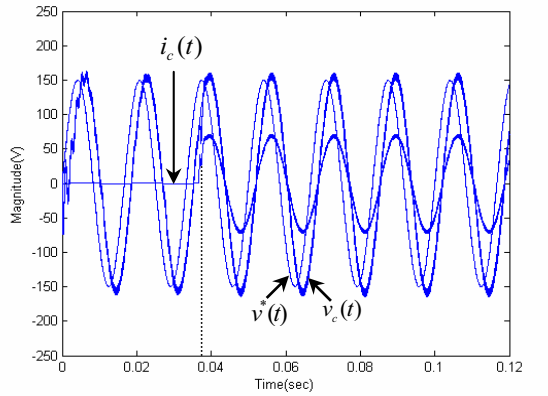

Fig. 15 Output response under a linear load change (Inward Approach)

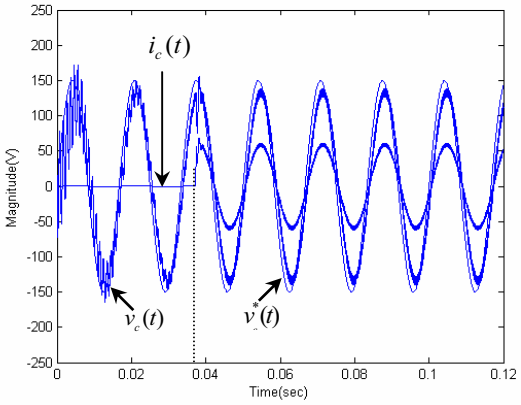

Fig. 16 Output response under a linear load change (Outward Approach)

The results in Fig. 15 and Fig. 16 show that the output response of inward approach has a lesser overshoot than that of outward approach but inevitably has a low tracking ability.

5. CONCLUSIONS

For designing a digital controller of UPS inverter, two different approaches are mainly applied with a design method of the characteristic ratio assignment. With a fixed sampling time, the continuous controller is discretized by means of the emulation method. The proposed controllers satisfy the given time response specifications with holding the stability of the closed-loop system. The summarized features of the proposed controllers for each approach are as follows:

In the framework of inward approach, this approach results in a good system performance in the viewpoint of robustness for an in-line type UPS. The designed controller has got a fast transient response and relatively small overshoot over a linear load change. On the other hand, it can not evade the phase delay and steady-state error.

In the framework of outward approach, the internal model control (IMC) method has been applied in outer loop so as to track the reference voltage. This approach results in a good robust tracking performance and small steady-state error. But, it has relatively high overshoot with respect to the abrupt change of loads. Therefore, this controller seems to be sensitive to the disturbance.

Within the limitation on the speed of time response, the CRA is applied to the problem of time response requirement such as overshoot and settling time. The simulation results using Simulink® verify the performances of the proposed controller over all linear load conditions.

ACKNOWLEDGMENTS

This work was supported by grant No. R01-2003-000-11738 -0 from the Basic Research Program of the Korea Science & Engineering Foundation

REFERENCES

[1] M.J. Yazdanpanah, E. Semsar, and B. Siahkolah, "An H_∞ Robust Controller for Single Phase PWM Inverters," Proc. Of 15th IFAC World Congress, Barcelona, Spain, 2002.

[2] Y. C. Kim, L. H. Keel, and S. P. Bhattacharyya, "Transient Response Control via Characteristic Ratio Assignment," *IEEE Trans. on Automatic Control,* vol AC-48, No. 12 pp. 2238-2244, Dec. 2003.

[3] A.V. Lipatov and N.I. Sokolov, "Some sufficient conditions for stability and instability of continuous linear stationary systems," *Automation and Remote Control,* vol. 39, pp.1285-1291, 1979.

[3] G.C. Goodwin, S.F. Graebe and M.E. Salgado, *CONTROL SYSTEM DESIGN,* Prentice Hall PTR, Upper Saddle River, NJ, 2001.

[4] A. Datta, M.T. Ho, and S.P. Bhattacharyya, *Structure and Synthesis of PID Controllers,* London, U.K., Springer-Verlag, 2000.

[5] K. S. Kim, Y. C. Kim, L. H. Keel, and S. P. Bhattacharyya, "PID Controller Design with Time Response Specifications," *In Proceedings of the 2003 American Cont. Conf.*, pp. 5005-5010, Denver, 2003.

[6] G. F. Franklin, J. D. Powel, and A. Emani-Naeini, *Feedback Control of Dynamic Systems*, Prentice-Hall, Upper Saddle River, New Jersey, 2002.