Analysis of Carrier PWM Algorithms For Three Phase Four Wire Multi-level Inverter

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Abstract:

This paper presents a simple PWM method to control three phase four leg multilevel inverters, which have been developed for supplying electrical power to three phase unbalanced load and for related power active filters. The method is derived from a general correlation between space vector PWM (SVPWM) method and carrier based PWM (CPWM) method. As an advantage, the simplicity and flexibility of the proposed CPWM control can be obtained and the complicated calculations of the 3-D SVPWM concepts can be avoided.

The method has been mathematical formulated and demonstrated by simulation results.

1. Introduction

In recent years, study on a three phase four wire inverter, which supplies an three phase voltages for a unbalanced three phase load, has drawn a special attention from researchers. Different PWM methods have been introduced for three phase four wire inverters. Many of them are derived from 3-D SVPWM concepts, which are rather inconvenient for complicated calculations. There has not been many papers about CPWM methods in four leg multilevel inverter.

In this paper, a carrier PWM method, which is based on the vector correlation between SVPWM and CPWM will be proposed and applied to a four wire multilevel inverter. It can be seen that, the mathematical calculation of the method is simple and the algorithm is flexible for applications. The content of the paper will be presented as follows:

- to propose an equivalent voltage model of a four leg inverter.
- to present correlation between the SVPWM and CPWM in four leg inverter.
- to proposed a CPWM algorithm for controlling a four leg inverter .
- to implement simulation.

2. Carrier based PWM for three phase three leg VSI

2.1 The equivalent voltage model of three phase three leg inverter

Three phase voltages v_a, v_b and v_c of an unbalanced load in abc coordinates can be further decomposed into the active $v_{x12}, x = a,b,c$ and zero sequence $v0$ voltages as follows:

$$v_0 = \frac{1}{3}(v_a + v_b + v_c) \qquad (1)$$

$$\begin{bmatrix} v_{a12} \\ v_{b12} \\ v_{c12} \end{bmatrix} = \begin{bmatrix} v_a - v_0 \\ v_b - v_0 \\ v_c - v_0 \end{bmatrix} \qquad (2)$$

The active voltages are related to the reference space vector $\bar{v}_{ref} = V_{ref}.\exp(j\theta)$ in a vector hexagon and determined as follows:

$$v_{a12} = V_{ref}.\cos\theta \quad , \quad v_{b12} = V_{ref}.\cos(\theta - 2\pi/3) \quad ,$$
$$v_{c12} = V_{ref}.\cos(\theta - 4\pi/3) \qquad (3)$$

The voltage model of inverter will be derived under an assumption that the reference voltage vector in a hexagon area is modulated from the three nearest vectors up to four subsequent switching states voltage in a half sampling period, the switching sequence produces active voltages and zero sequence voltage. The phase to dc neutral point voltages v_{x0} as shown in fig.1a can be expressed as a summation of active v_{x12} and internal zero sequence component $v_{0,int}$ (fig.1d) as follows:

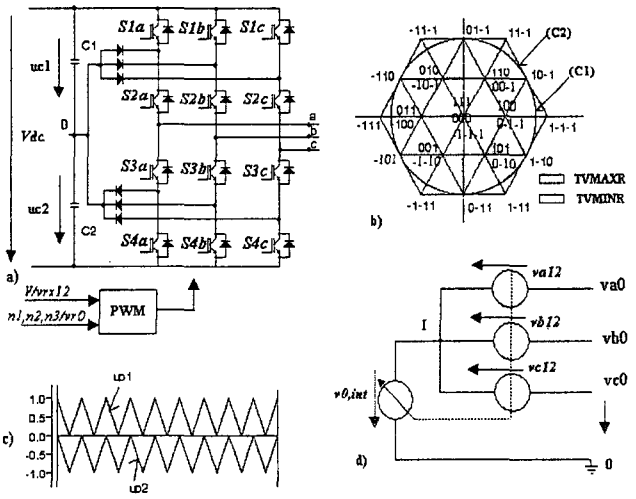

그림 1: Three level inverter: a) circuit and b) vector diagrams, c) carrier waves and d) equivalent phase to dc neutral point output voltages

$$v_{x0} = v_{x12} + v_{0,\text{int}}, x = a,b,c \qquad (4)$$

2.2 The SVPWM-CPWM correlation

For three-level inverter, two carrier waveforms are used, operating in ranges of (-1,0) and (0,1) as shown in fig.1c. The general correlation between the SVPWM and the CPWM in a multilevel inverter [5],[6] shows that a SVPWM can be implemented equivalently by a CPWM technique by adding a proper zero sequence function to active components.

The corresponding modulating signals consist of active modulating component v_{rx12} and zero sequence function $v_{r0,\text{int}}$, and can be described as follows:

$$v_{rx} = v_{rx12} + v_{r0,\text{int}},\ x = a,b,c \qquad (5)$$

For an n-level inverter, the active modulating components ($\vec{v}_{rx12} = [v_{ra12}, v_{rb12}, v_{rx12}]^T$) are related to the active voltages and the dc- source voltage V_{dc} v as

$$\vec{v}_{rx12} = [\frac{(n-1).v_{a12}}{V_{dc}}, \frac{(n-1).v_{b12}}{V_{dc}}, \frac{(n-1).v_{c12}}{V_{dc}}]^T \qquad (6)$$

Let's define functions max, mid and min as the maximum, the middle and the minimum values from among three active voltages as follows:

$$\max = \max[v_{ra12}, v_{rb12}, v_{rc12}] \qquad (7)$$
$$mid = mid[v_{ra12}, v_{rb12}, v_{rc12}]$$
$$\min = \min[v_{ra12}, v_{rb12}, v_{rc12}]$$

The zero sequence function $v_{r0,\text{int}}$ is related to the zero sequence voltage $v_{0,\text{int}}$ as

$$v_{0,\text{int}} = \frac{V_{dc}}{n-1}.v_{r0,\text{int}} \Rightarrow v_{r0,\text{int}} = \frac{(n-1).v_{0,\text{int}}}{V_{dc}} \qquad (8)$$

and can be determined as a function of vector redundancy [5],[6] as follows:

$$v_{r0,\text{int}} = p_{\min} - \min + \eta_1.K_1 + \eta_2.K_2 + \eta_3.K_3 \qquad (9)$$

At least two from among redundant factors are integer and the following constraints are met as

$$0 \le \eta_1 \le l_{r1}\ ,\quad 0 \le \eta_2 \le l_{r2}\ ,\quad 0 \le \eta_3 \le l_{r3}\ ,$$
$$0 \le \eta_3 \le \eta_2 \le \eta_1 \le (\eta_3 + 1) \qquad (10)$$

Parameters K_1, K_2 and K_3 are determined as

$$\left.\begin{aligned} K_1 &= 1 + \text{int}[\max - \min] - (\max - \min) \\ K_2 &= -\text{int}[\max - mid] + (\max - mid) \end{aligned}\right\} for\ \ l_{r1} > l_{r2} \qquad (11)$$

$$\left.\begin{aligned} K_1 &= 1 + \text{int}[mid - \min] - (mid - \min) \\ K_2 &= 1 + \text{int}[\max - mid] - (\max - mid) \end{aligned}\right\} for\ \ l_{r1} = l_{r2}$$

$$K_1 + K_2 + K_3 = 1$$

where the levels of redundancies l_{r1}, l_{r2} and l_{r3} are deduced as

$$l_{r1} = n - 1 - \text{int}[\max - \min] \qquad (12)$$
$$l_{r2} = n - 2 - \text{int}[mid - \min] - Int[\max - mid]$$
$$l_{r3} = l_{r1} - 1.$$

The limits of zero sequence function are determined substituting (η_1, η_2, η_3) by (0,0,0) and (l_{r1}, l_{r2}, l_{r3}). The results will be:

$$v_{r0,\text{int}\min} = P_{\min} - \min \qquad (13)$$
$$v_{r0,\text{int}\max} = P_{\min} + (n-1) - \max$$

From (8)-(11), the zero sequence function $v_{r0,\text{int}}$ can be derived in a useful form as follows:

$$n_0 = \text{int}[v_{r0,\text{int}} - P_{\min} + \min] \qquad (14)$$
$$v_{r1} = v_{r0,\text{int}} - P_{\min} + \min - n_0 \qquad (15)$$

$$v_{r0,\text{int}} = \begin{cases} P_{\min} - \min + n_0 + x_1.K_1 & if \quad 0 \le v_{r1} \le K_1 \\ P_{\min} - \min + n_0 + K_1 + x_2.K_2 & if \quad K_1 < v_{r1} \le K_1 + K_2 \\ P_{\min} - \min + n_0 + K_1 + K_2 + x_3.K_3 & if \quad K_1 + K_2 < v_{r1} < 1 \end{cases} \qquad (16)$$

where $(0 \le x_j < 1)$, $j = 1,2,3$.

If $0 < v_{r1} < K_1$, the active centered redundant vectors will appear at the pivot vector $\vec{U}_1$. Similarly, two remaining inequalities of (16) correspond to the active redundant vectors at the vectors $\vec{U}_2$ and $\vec{U}_3$.

2.3 Carrier based SVPWM and DPWM for three leg inverter

The correlation (9) or (16) could be used to perform PWM methods, which approximate inverter zero sequence function output to the reference zero sequence input. The principle is drawn in fig.2. There are two cases:

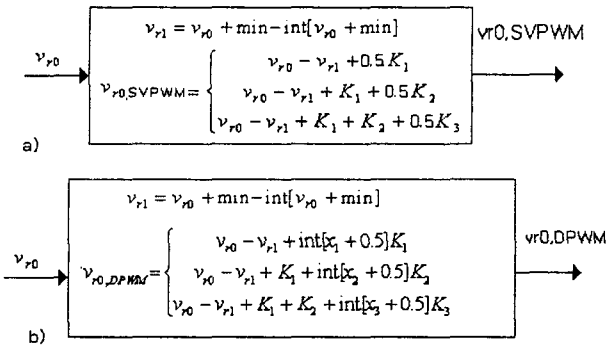

그림 2: Principle of zero sequence controlled PWM : Generation of zero sequence function for a) SVPWM and b) DPWM.

a) SVPWM: to deduce the zero sequence function $v_{r0,SVPWM}$, which realizes the SVPWM and approximates the required zero sequence function v_{r0}^*. This can be done by substituting $v_{r0,\text{int}} = v_{r0}^*$ into (14) and (15), and setting $x_j = 0.5$ into (16). The function $v_{r0,SVPWM}$ can be obtained as follows:

$$v_{r0,SVPWM} = \begin{cases} P_{\min} - \min + n_0 + 0.5xK_1 & if \quad 0 \le v_{r1} \le K_1 \\ P_{\min} - \min + n_0 + K_1 + 0.5xK_2 & if \quad K_1 < v_{r1} \le K_1 + K_2 \\ P_{\min} - \min + n_0 + K_1 + K_2 + 0.5xK_3 & if \quad K_1 + K_2 < v_{r1} < 1 \end{cases} \qquad (17)$$

b) DPWM: to deduce the zero sequence function $v_{r0,DPWM}$, which realizes discontinuous PWM and approximates the required zero sequence function v_{r0}^*. This can be done by substituting $v_{r0,\text{int}} = v_{r0}^*$ into (14) and (15) and setting $x_j.K_j \to \text{int}(x_j + 0.5).K_j$ into (16). The function $v_{r0,DPWM}$ can be obtained as follows:

$$v_{r0,DPWM}=\begin{cases} P_{\min}-\min+\eta_0+\text{int}[x_1+0.5]K_1 & if \quad 0\le v_{r1}\le K_1 \\ P_{\min}-\min+\eta_0+K_1+\text{int}[x_2+0.5]K_2 & if \quad K_1<v_{r1}\le K_1+K_2 \\ P_{\min}-\min+\eta_0+K_1+K_2+\text{int}[x_3+0.5]K_3 & if \quad K_1+K_2<v_{r1}<1 \end{cases} \tag{18}$$

For three leg inverter, by adding the zero sequence functions in (17), (18) to fundamental components, the obtained modulating signals will implement corresponding carrier based SVPWM and discontinuous PWM, respectively.

3. Three phase four leg inverter

3.1 The equivalent voltage model of three phase four leg inverter

The three phase four leg inverter can be considered as two circuits in series: three phase three-leg inverter, which generates active voltages v_{x12} , x=a,b,c and internal zero sequence voltage $v_{0,\text{int}}$, and single leg inverter, which generates only external zero sequence voltage $v_{0,ext}$. The active voltages of four leg inverter are performed independently on the switching states of single leg inverter. The external zero sequence voltage can be controlled separately and its output voltage varies in the range $\left(-\frac{V_{dc}}{2},+\frac{V_{dc}}{2}\right)$.

For three-level inverter, the modulating signal of the single leg $v_{r0,ext}$ for producing external zero sequence voltage $v_{0,ext}$ can be derived from its corresponding zero sequence voltage as

$$v_{0,ext}=v_{r0,ext}\cdot\frac{V_{dc}}{2},-1\le v_{r0,ext}\le 1 \tag{19}$$

If $v_{r0,ext}$=-1, the lower pair (S3f,S4f) in fig.3a is ON and $v_{0,ext}=-V_{dc}/2$; if $v_{r0,ext}$=1, the upper pair (S1f,S2f) is ON and $v_{0,ext}=V_{dc}/2$.

The output zero sequence voltage of a four leg inverter can be performed as a summation of the previously described internal and external voltage components [2] as

$$v_0=v_{0,\text{int}}-v_{0,ext}=v_{r0,\text{int}}\cdot\frac{V_{dc}}{n-1}-v_{r0,ext}\cdot\frac{V_{dc}}{n-1} \tag{20}$$

$$v_0=(p_{\min}-\min+\eta_1.K_1+\eta_2K_2.+\eta_3.K_3).\frac{V_{dc}}{n-1}-(P_{\min}+\eta_0)\frac{V_{dc}}{n-1} \tag{21}$$

where $\eta_0=v_{r0,ext}-P_{\min}$, and $0\le\eta_0\le(n-1)$.

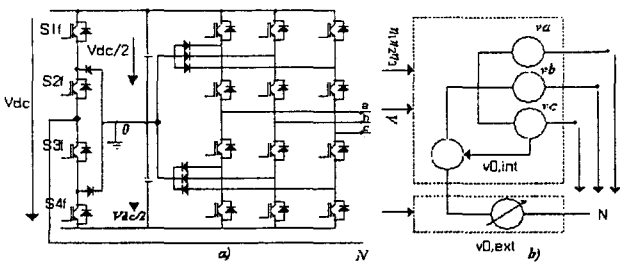

그림 3: *Three phase four leg inverter: a) circuit diagram and b) equivalent voltage model.*

From (21), there are two available possibilities of controlling the zero sequence voltage by varying either (η_1,η_2,η_3) (or $v_{r0,\text{int}}$) of three leg inverter or η_0 (or $v_{r0,ext}$) of the single leg inverter.

3. 2 The proposed carrier based SVPWM method for three phase four leg inverter

Since the active voltages depend only on the switching states of three leg inverter , for obtaining a high performance, the three leg inverter will be supposed to be implemented by the SVPWM, with two active redundant vectors equally centered. With the assumption that there is constant dc source voltages, this inverter will be proposed to compensate the main part of the reference zero sequence voltage and the single leg inverter will compensate the remaining part. The diagram illustrates the switching states of the described principle is drawn in fig.4.

The method can be explained using diagram in fig.5 From reference three phase unbalanced voltages $v_{ra}^*,v_{rb}^*,v_{rc}^*$, the active components $v_{ra12}^*,v_{rb12}^*,v_{rc12}^*$ and reference zero sequence components v_{r0}^* will be derived. The zero sequence function and as results, modulating signals of two inverters can be generated as follows:

a) Control of three leg inverter: The value of the internal zero sequence function $v_{r0,\text{int}}$ related to the internal zero sequence voltage will be set approximately as closest as possible to the reference. If the reference ZSF is out of the limited ranges ($v_{r0,\text{int min}}$, $v_{r0,\text{int max}}$), the inverter ZSF $v_{r0,\text{int}}$ will be set at its defined limit. Therefore, a PWM control of the three leg inverter can be described by its zero sequence function as follows:

$$v_{r0,\text{int}}=\begin{cases} v_{r0,\text{int}Cent\max} & if \quad v_{r0}>v_{r0,\text{int}\max} \\ v_{r0,\text{int}Cent} & if \quad v_{r0,\text{int}\min}\le v_{r0}\le v_{r0,\text{int}\max} \\ v_{r0,\text{int}Cent\min} & if \quad v_{r0}<v_{r0,\text{int}\min} \end{cases} \tag{23}$$

Determination of function $v_{r0,\text{int}Cent}$: if the required zero sequence function v_{r0} varies in the limits (13) $v_{r0,\text{int min}}\le v_{r0}\le v_{r0,\text{int max}}$, the carrier based PWM will be implemented as SVPWM. The corresponding zero sequence function can be obtained by (17) as

$$v_{r0,\text{int}Cent}=v_{r0,SVPWM} \tag{24}$$

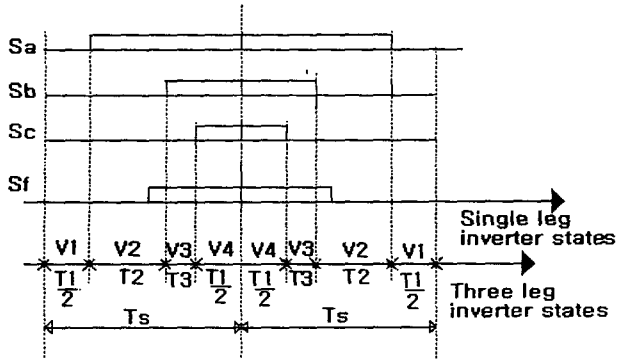

그림 4:Principle of separated PWM control of three leg inverter and single leg inverter.

Determination of function $v_{r0,\text{int }Cent\max}$. From the general form of the zero sequence function (9) and limits of the redundant factors (10), the maximum and minimum zero sequence functions of the SVPWM method can be determined as follows:

$$v_{r0,Cent\max} = \begin{cases} (n-1)/2 - \max - 0.5K_1 & if \quad l_{r1} > l_{r2} \\ (n-1)/2 - \max - 0.5K_2 & if \quad l_{r1} = l_{r2} \end{cases} \tag{25}$$

Determination of function $v_{r0,\text{int }Cent\min}$

$$v_{r0,\text{int}Cent\min} = -(n-1)/2 - \min + 0.5.K_1 \tag{26}$$

where (pmin=-(n-1)/2).

The diagrams of extreme internal zero sequence functions for three level inverter for modulation index m=1 are drawn in fig.***6a.*** For three level inverter two extreme internal zero sequence function values are equal each other $v_{r0,\text{int }Cent\max} = v_{r0,\text{int }Cent\min}$. The difference happens for higher level inverter.

b) Control of single leg inverter

The remaining part of the zero sequence voltage will be compensated by the single leg inverter, whose reference modulating signal can be determined as follows:

$$v_{r0,ext} = v_{r0,\text{int}} - v_{r0}\,;\; v_{r0} = \frac{v_0}{V_{dc}}.(n-1) \tag{27}$$

c) Limits of zero sequence voltages of four leg inverter

The total maximum and the minimum zero sequence voltages of four leg inverter, in which the three leg inverter is controlled by SVPWM method are determined using (20), (26), and (27) as

$$v_{0,4leg\max} = (v_{r0,\text{int }Cent\max} + \frac{n-1}{2}).\frac{V_{dc}}{n-1} \tag{28}$$

$$v_{0,4leg\min} = (v_{r0,\text{int }Cent\min} - \frac{n-1}{2}).\frac{V_{dc}}{n-1}$$

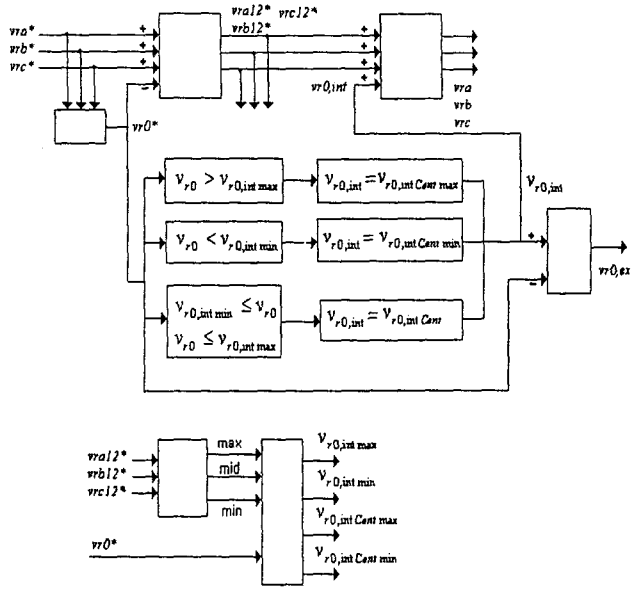

그림 5: Principle of the proposed CPWM method of four leg multilevel inverter.

The diagrams of total maximum and minimum of zero sequence components for m=1 are drawn in fig.6b. Operating range of zero sequence component will be larger for smaller modulation index.

In fig.7, there are shown diagrams of the generated internal zero sequence functions of three leg inverter from the required zero sequence signal and related limited signals of a three level three leg inverter

Advantages of the proposed carrier SVPWM

- analysis of zero sequence component of multilevel inverter using correlation between SVPWM and CPWM is simple. The calculation of modulating signals are less complicated in comparison with 3-D method [1]. The 3-D geometrical vector analysis is avoided. The method can be properly modified to apply for discontinuous PWM.
- the PWM method is simple for two zero sequence voltages are separately controlled.
-The proposed SVPWM method can obtain maximum range of zero sequence voltage output.

Flexible control of the internal zero sequence function by varying redundant factors could be utilized for controlling the neutral point voltage balancing. This will be investigated in further works.

4. Conclusions

The paper has presented a new method to analyze a four leg multilevel inverter by decomposing it into two simple inverters in series and introduced a simple SVPWM method to control this four leg inverter by varying redundant factors of the zero sequence function . The simple mathematical description, equivalent characters to the SVPWM and possible modifying for obtaining different PWM modes

present probably the advantageous characters in comparison with other 3-D methods.

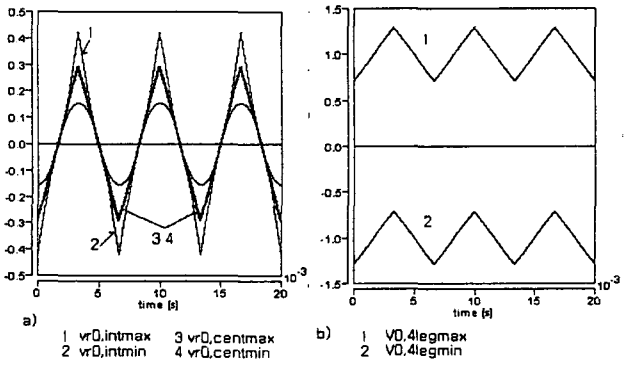

그림 6: Three- level inverter: diagrams of max and min zero sequence components for m=1.

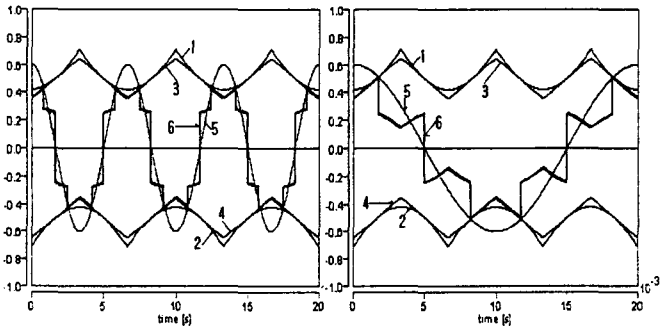

그림 7: Three level four leg inverter: the diagrams of zero sequence components for various referent zero sequence voltages

1-maximum zero sequence function $v_{r0,\text{int max}}$ *, 2-minimum zero sequence function* $v_{r0,\text{int min}}$ *, 3-maximum zero sequence function of SVPWM method* $v_{r0,\text{int Cent max}}$ *, 4-minimum zero sequence function of SVPWM method* $v_{r0,\text{int Cent min}}$ *, 5- the required zero sequence function* v_{ro}^{*} *, 6- the main part of zero sequence function generated by three leg inverter* $v_{r0,\text{int Cent}}$ *.*

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