전력전자학술대회 논문집 2004. 7.12 ~ 7.15

영 전위 중성점을 가진 새로운 3상 Three-Level 스위치 전압원 인버터

오원식, 한상규, 최성욱, 문건우
KAIST

Three Phase Three-Level Switched Voltage Source PWM Inverter with Zero Neutral Point Potential

Won-Sik Oh, Sang-Kyoo Han, Seong-Wook Choi, and Gun-Woo Moon
KAIST

ABSTRACT

A new three phase three-level Pulse Width Modulation (PWM) Switched Voltage Source (SVS) inverter with zero neutral point potential is proposed. The major advantage is that the peak value of the phase output voltage is twice as high as that of the conventional neutral-point-clamped (NPC) PWM inverter. Furthermore, three-level waveforms of the proposed inverter can be achieved without switch voltage unbalance problem. Since the average neutral point potential of the proposed inverter is zero, the common ground between input stage and output stage is possible. The proposed inverter is verified by experimental results based on a laboratory prototype.

1. 서 론

In recent years, industry has begun to demand higher power equipment and multi-level inverters have been attracting increasing attention for power conversion in high-power applications due to the lower harmonics, high efficiency, and lower voltage stress compared with two-level inverter. Numerous topologies to realize multi-level inverter have been introduced and widely studied[1-5]. The most important topologies of them are diode-clamped (neutral-point-clamped) inverter[6], capacitor-clamped (flying capacitor) inverter[7], and cascaded H-bridge inverter with separated DC sources[1,3]. In the diode-clamped inverter circuit proposed by Nabae et al in 1981. It is composed of a divided input source and several clamping diodes to make a neutral point at the output. Eventhough the NPC inverter can achieve higher power and lower harmonics by three-level operation, the static and dynamic sharing of the voltage across the switches is quite difficult[7]. Furthermore, diode-clamped inverter shows undesirable features such as fluctuation of the neutral point voltage due to difference of the switching characteristics and over voltage problems across the inner switching devices. Meynard et al proposed a multi-level structure where the device off state voltage clamping was achieved by using clamping capacitors rather than clamping diodes[7]. Although this topology solves the problem of static and dynamic sharing of the voltage across the switches, it still has the voltage unbalance problem of the diode-clamped inverter and DC offset voltage of the output. The cascaded H-bridge inverter is an alternative approach to achieve multi-level waveforms based on the series connection of full-bridge inverters with multiple isolated DC bus. Although the modular structure solves the voltage unbalance problem, this approach needs many isolated DC sources and link voltage controller.

To solve these all drawbacks of conventional multi-level inverter, a new three-level Switched Voltage Source (SVS) PWM inverter is proposed. Fig. 1 shows the circuit configuration of the proposed three-level SVS PWM inverter. It consists of three single-phase inverter modules and each module is composed of a main inverter stage and switched voltage source stage which includes two switches, one flying capacitor, one diode and a small size snubber inductor as shown in Fig. 2. It provides a three-level output across U and N, i.e., $v_{UN}=V_{dc}$, 0, or V_{dc}. Therefore, the peak value of phase voltage is V_{dc}, and the peak value of line to line voltage is $2V_{dc}$. Since the phase voltage of the SVS inverter is twice as high as that of the conventional NPC inverter, it is well suitable for the inverter with low input voltage such as a fuel cell, battery, and solar cell input. In addition, the SVS inverter does not have the voltage unbalance problem[4] which is often happened to the conventional three-level inverter with the divided input source. Furthermore, since the DC offset of the output phase voltage is zero, the neutral point of the output load stage can be connected to the ground, and the SVS inverter is safe without an electrical isolation. Therefore, it can be well applied to a transformer-less power conditioning system.

2. 본 론

2.1 Operational Principles

2.1.1 Circuit Operation

The circuit configuration of the three-level PWM SVS inverter consists of three single-phase inverter modules as shown in Fig. 1. Each module can be independently operated with a single input source. The basic operational modes of the SVS inverter are shown in Fig. 2 and Fig. 3. Since the flying capacitor C_1 is charged to input voltage V_{dc} when the switch M_1 turns on, voltage across C_1 can be assumed to be a constant voltage source V_{dc}, and snubber inductor L_1 can be ignored. As can be seen in Fig. 2, the voltage of node A can be changed to input voltage V_{dc} and 0V by switch M_1 and M_3, respectively. The difference between node A and Uis 0 and $-V_{dc}$ by switch M_2 and M_4, respectively, as shown in Fig. 3. Therefore, the SVS inverter has four different cases and three states of the output terminal voltage v_{UG}: V_{dc}, 0, and $-V_{dc}$ which are twice as those of the conventional NPC inverter. Furthermore, v_{UG} does not have DC component.

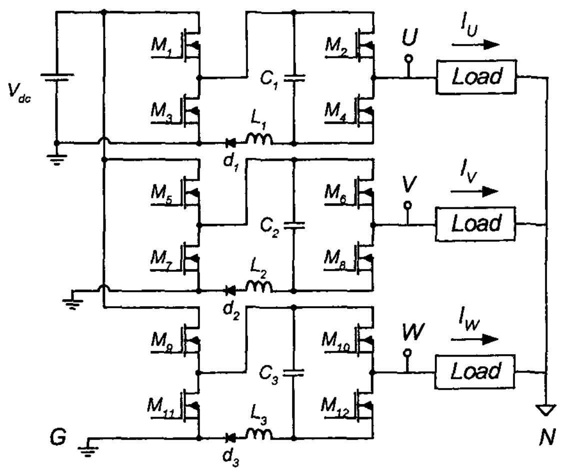

그림 1 제안된 SVS 인버터 회로도

Fig. 1 Circiut diagram of the proposed SVS inverter

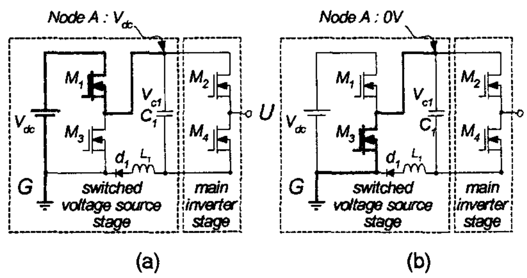

그림 2 스위치 전압원의 동작 원리

Fig. 2 Operational principles of switched voltage source

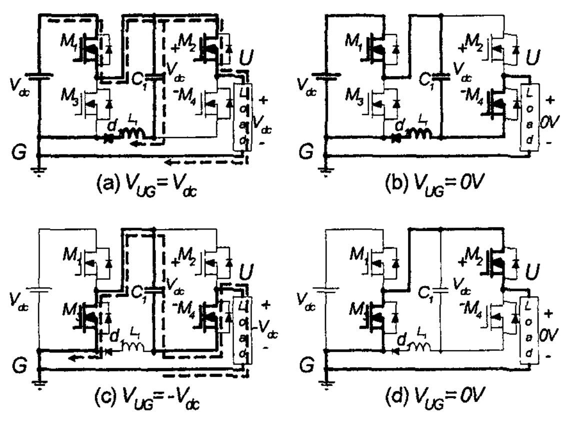

그림 3 SVS 인버터의 동작 모드

Fig. 3 Operational modes of SVS inverter

Case 1 (Fig 3. (a)): The output voltage v_{UN} is V_{dc} and C_1 is charged to V_{dc}, when switches M_1 and M_2 turn on. The snubber inductor limits the inrush current of M_1 when the voltage of C_1 is different from V_{dc}.

Case 2 (Fig 3. (b)): The output voltage v_{UN} is 0V when switches M_1 and M_4 turn on.

Case 3 (Fig 3. (c)): When switches M_3 and M_4 turn on, the diode $d_1$turns off. In addition, the output voltage v_{UN} is clamped to -V_{dc} and flying capacitor$C_1$is discharged.

Case 4 (Fig 3. (d)): The output voltage v_{UN} is 0 and diode d_1 is off, when switches M_3 and M_4 turn on.

The same analysis can also be applied to the other modules.

2.1.2 PWM Signal Generation

To generate the three-level PWM waveform, the sine-triangular PWM method[10, 11] is used. The sine-carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves. Three reference sinusoids are 120° apart to produce a balanced three-phase output, and the correspondingoutput signals for a three-level PWM can be expressed as

$$v_{xN} = \begin{cases} V_{dc} & \text{for } V_{ref,x} > V_{tri,1} \\ 0 & \text{for } V_{tri,1} > V_{ref,x} > V_{tri,2} \\ -V_{dc} & \text{for } V_{ref,x} < V_{tri,2} \end{cases} \quad (1)$$

where, $x = U, V, W$.

For the first module, the reference signal, two triangular carrier waves, and corresponding switch gate signals are shown in Fig. 4. When the reference signal is positive, switch M_1 turns on and switch M_3 turns off as shown in Fig. 3 (a) and (b). In this mode, switch M_2 turns on when the instantaneous value of the reference signal is larger than triangular carrier ($V_{tri,1}$), and switch M4turns on when the instantaneous value of the reference signal is less than carrier ($V_{tri,1}$). When the reference signal is negative, switch M_4 turns on and switch M_2 turns off as shown in Fig. 3 (c) and (d). In this mode, switch M_1 turns on when the instantaneous value of the reference signal is less than carrier ($V_{tri,2}$), and switch M_3 turns on when the instantaneous value of the reference signal is larger than carrier ($V_{tri,2}$).

2.2 Analysis of the Proposed Inverter

In the proceeding section, the voltage across capacitor C_1 of the switched voltage source (SVS) stage shown in Fig. 1 was assumed to be

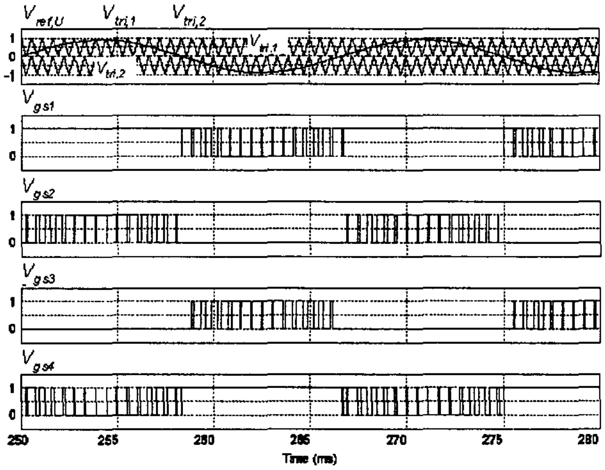

그림 4 한 모듈의 스위칭 파형
Fig. 4 Gate signals of one of three modules

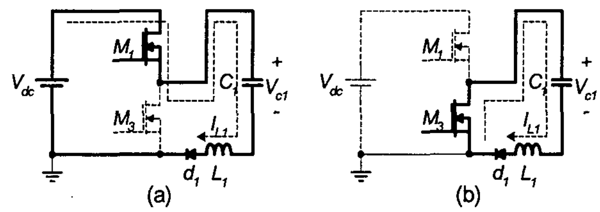

그림 5 SVS 인버터의 동작모드
(a)전력전달모드 (b) 환류 모드
Fig. 5 Operation of the SVS inverter
(a) powering mode (b) freewheeling mode

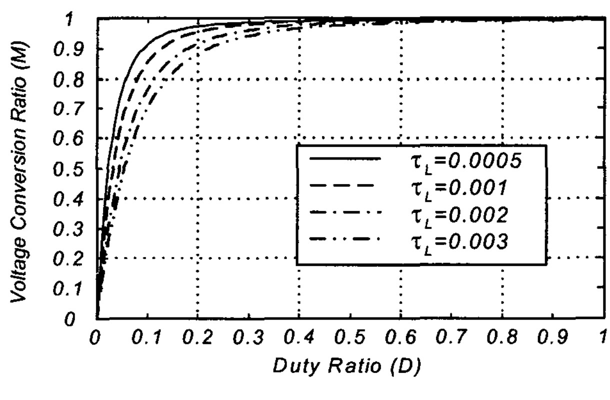

그림 6 DCM Buck 컨버터 입출력 비
Fig. 6 Voltage conversion ratio in the DCM buck converter

a constant voltage source V_{dc}. However, the voltage across the capacitor C_1, V_{C1} is slightly different from the input voltage source V_{dc}. The difference between the voltage across the capacitor C_1 and the input voltage source V_{dc} may cause the inrush current on the switch M_1 and diode d_1 when the switch M_1 turns on. To solve this problem, a small snubber inductor L_1 is inserted between the diode d_1 and capacitor C_1. However, this small snubber inductor does not affect the operation of the proposed SVS inverter. The effect of the small snubber inductor L_1 is considered in this section.

The SVS inverter is operated as buck converter , when $V_{ref,1}<V_{tri,2}$ as seen in Fig. 5. Therefore, to analyze the operation of the SVS stage according to the value of inductor, the simple buck converter can be considered. If the snubber inductor L_1 is small, the buck converter operates in Discontinuous Conduction Mode (DCM). When the buck converter is operated in DCM, its voltage conversion ratio is expressed as

$$M=\frac{V_o}{V_{dc}}=\frac{2}{1+\sqrt{1+\frac{8\cdot\tau_L}{D^2}}} \qquad (2)$$

where, $\tau_L=(L_o/R_o\cdot T_s)=L_o\cdot I_o/(V_o\cdot T_s)$

T_s=switching period, D=duty ratio

R_o=load resistance.

Based on this equation, the voltage conversion ratio M can be plotted as shown in Fig. 6. This figure shows that the less inductance can make voltage conversion ratio M close to the unity for wide range of the duty ratio. In case of the laboratory prototype, the modulation index ma is less than 0.8, and duty ratio of the switch M1 is greater than 0.2 as shown in Fig. 7. Also, the parameter τ_L is about 0.0005, and the voltage conversion ratio M at D=0.2 is 0.976. It means that the difference between the voltage across the capacitor C_1 and the input voltage source V_{dc} is 2.4%. Therefore, V_{C1} can be assumed to be voltage source charged with V_{dc}.

2.3 Experimental Results

The operational principles of the SVS inverter shown in Fig.1 have been investigated by experimental results. For three-level inverter drive, the sine-triangular wave modulation scheme is used to obtain three-level PWM pattern. The laboratory prototype with 200VDC of the input voltage, triangular carrier wave of 9kHz frequency is employed to the 50Ω resistive load with switching frequency LC filter. Fig. 7 shows the experimental results of the phase voltages, line to line voltages, and load currents of the three-level voltage source inverter, respectively. As can be seen in Fig. 7, the peak value of the phase voltages V_{dc} is 200V and the peak value of the line to line voltage $2V_{dc}$ is 400V. These are twice as high as those of the conventional NPC inverter. Therefore, the larger amplitude of the output voltage can be obtained compared with the conventional NPC inverter and it is well suitable for inverter with low input voltage source.

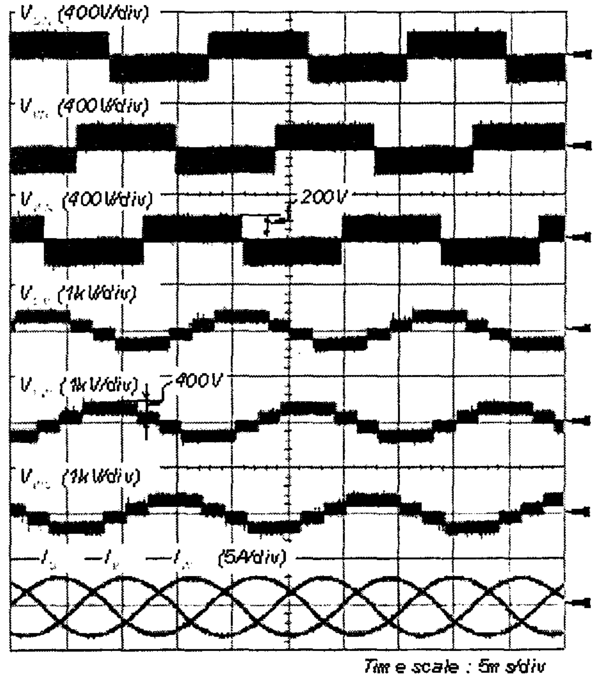

그림 7 SVS 인버터의 주요 실험 파형

Fig. 7 Experimental results of SVS inverter

Moreover, since the phase and line voltage show three and five levels, respectively, the multi-level waveform can be achieved by employing the interconnected modules without isolated DC sources and voltage unbalance problem. Furthermore, the proposed multi-level SVS inverter can considerably reduce the voltage harmonics and output filter size. In addition, since the average value of the phase voltages to the ground during one period is zero, the neutral point can be connected to the ground and it can be applied to transformer-less grid connected photovoltaic (PV) and fuel cell power conditioning system.

3. 결 론

A new three phase three-level SVS inverter with zero neutral point potential is proposed. Its phase voltage and line to line voltage is twice as high as those of the conventional neutral-point-clamped PWM inverter and three-level waveform can be achieved without switch voltage unbalance problem. Therefore, it is well suitable for inverter with low input voltage such as fuel cell, battery, and solar cell input. Furthermore, its average neutral point potential is zero. Therefore, the proposed SVS inverter can be widely applied to motor drive system and transformer-less grid connected power conditioning system.

이 논문은 IT research center project의 연구비 지원에 의하여 연구되었슴

참 고 문 헌

[1] Rodriguez, J., Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications", IEEE Transactions on Industrial Electronics, Vol. 49, pp. 724-738, 2002.

[2] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel converters-a new breed of power converters", IEEE Transactions on Industry Applications, Vol. 32, pp. 509-517, 1996.

[3] Fang Zheng Peng , "A generalized multilevel inverter topology with self voltage balancing", IEEE Transactions on Industry Applications, Vol. 37, pp. 611-618, 2001.

[4] Bor-Ren Lin, "Analysis and Implementation of a three-level PWM Rectifier/Inverter", IEEE Transactions on Aerospace and electronic systems, Vol. 36, No3, pp. 948-956, 2000.

[5] Hochgraf, C., Lasseter, R., Divan, D. and Lipo, T.A., "Comparison of multilevel inverters for static VAr compensation", IEEE Conference, Industry of Applications Society, vol. 2, pp. 921-928, 1994.

[6] Akira Nabae, Isao Takahashi and Hirofumi Akagi, "A New Neutral-Point-Clamped PWM Inverter", IEEE Transactions on Industrial Applications, Vol. IA-17, No5, pp. 518-523, 1981.

[7] Meynard, T.A. and Foch, H., "Multi-level conversion: high voltage choppers and voltage-source inverters", Power Electronics Specialists Conference, vol. 1, pp. 397-403, 1992.

[8] Carrer, P., Meynard, J. and Lavieville, P., "4000V 30A eight level IGBT inverter leg", Proceedings of European Power Electronics and Applications Conference, pp. 106-111, 1995.

[9] Lai, J. S. and Peng, F. Z., "Multilevel converters A new breed of power converters", IEEE Transactions on Industrial Applications, vol. 30, pp. 509-559, 1996.

[10] K. R. M. N. Ratnayake, Y. Murai, and T. Watanabe., "Novel PWM Scheme to Control Neutral Point voltage Variation in Three-Level Voltage Source Inverter", IEEE, Industry Applications Conference, vol. 3, pp. 1950-955, 1999.

[11] Rufer, A., "An aid in the teaching of multilevel inverters for high power applications", Proceedings of the Power Electronics Specialists Conference, pp. 347-352, 1995.