Multi-modulating Pattern- A Unified Carrier based PWM Method in Multi-level Inverter- Part 1

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Abstract:

This paper presents a systematical approach to study carrier based PWM techniques (CPWM) in diode-clamped and cascade multilevel inverters by using the proposed multi-modulating pattern method. This method is based on the vector correlation between CPWM and space vector PWM (SVPWM) and applicable to both multilevel inverter topologies. The CPWM technique can be described in a general mathematical equation, and obtain the same outputs similarly as of corresponding SVPWM. Control of the fundamental voltage, vector redundancies and phase redundancies in multilevel inverter can be formulated separately in the CPWM equation. The deduced CPWM can obtain a full vector redundancy control, and fully utilize phase redundancy in a cascade inverter.

In the paper, CPWM equations and corresponding algorithm for generating multi-modulating signals will be performed, in which SVPWM attributes will be presented by corresponding controllable factors.

1. Introduction

The two most common multilevel inverter topologies are diode-clamped and cascade inverters as shown in fig.1 and 2. For their controlling, carrier based PWM (CPWM) and space vector PWM (SVPWM) methods have been used the most in practice [1]-[3]. The SVPWM is implemented based on a vector diagram and highlight for its control flexibility. The implementation at higher level inverters still remains sophisticated.

The CPWM technique is realized using carrier waves and modulating signals. For diode-clamped inverter, multi-carrier phase disposition technique (PD) using a single modulating signal per phase- called single modulating system (SMS), shows be a proper solution. For cascade inverter, phase-shift carrier base modulation would give a similar performance [4]. Even if the previous PWM methods have been developing in practice for years, the correlation between them have been accepted based on somewhat heuristic investigations [3]. Vector redundancy control, which presents a high flexibility of SVPWM technique, has not been presented in the CPWM methods. The modulating pattern (MP) method, which is derived from the principle control between limit trajectories [5],[6], has appropriately clarified a vector character of the SVPWM-CPWM correlation [7],[8]. The vector redundancy control is presented by related redundant factors of the zero sequence function.

The recent studies [9],[10] have shown that if more active redundant vectors in the smallest triangle area are involved in the sampling period-see fig.3e, a better regulation of the dc neutral point voltage can be obtained. However, the SMS is not available for this purpose.

The cascade multilevel inverter has its phase redundancies. The problem is that, the phase redundancies are hidden out of the vector diagram and the SMS can not distinguish phase redundancies.

Several methods, which use modified modulating signals or modified multi carrier wave systems have been introduced [3],[4],[11]. However, a unified mathematical formulation would be needed to explain systematically the problems of vector redundancies and phase redundancies .

The previously described problems can be solved by CPWM with multi-modulating system (MMS), which has several modulating signals per phase and that is performed based on the CPWM-SVPWM correlation using multi-modulating patterns (MMP). The proposed MMS will show the possibility of implementing with maximum number of active redundant vectors and controlling the phase redundancies of cascade multilevel inverter.

The paper describes MMP, CPWM equations for MMS and introduces an algorithm to generate multi-modulating signals. Any CPWM method equivalent to the SVPWM method can be expressed in a unified mathematical formulation. From the previous discussion, there are three main features to characterize three phase multilevel inverter: the fundamental voltage, the vector redundancies and phase redundancies. In the proposed MMS, three mentioned quantities will be controlled separately in the CPWM modulator and this makes the control more flexible.

2. Basic Terminologies

In this section, the following results will be derived based on the vector analysis process and be valid to both types of multilevel inverters. The circuit diagrams of a five-level diode-clamped inverter and corresponding cascade type are drawn in fig.1a and fig.2, respectively. The multi-carrier phase disposition (PD) technique will be selected as a unified carrier wave system in the proposed method as shown in fig.4.

The vector analysis has been used effectively to study SVPWM control of multilevel inverter [2],[5],[7],[11]. In the abc coordinate system, the reference vector $\vec{V}^* = [v_a, v_b, v_c]^T$ can be analyzed as a linear combination of three pivot vectors $\vec{U}_1, \vec{U}_2$ and $\vec{U}_3$ as follows:

$$\vec{V}^* = K_1.\vec{U}_1 + K_2.\vec{U}_2 + K_3.\vec{U}_3 \quad (1)$$

$$K_1 + K_2 + K_3 = 1 ; 0 \le K_1, K_2, K_3 \le 1 \quad (2)$$

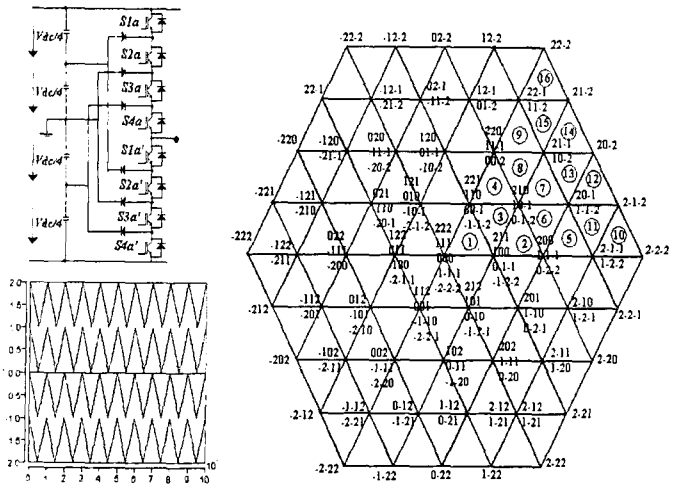

Figure 1:A-phase leg circuit , carrier waves and modulating pattern diagram of five-level diode-clamped inverter.

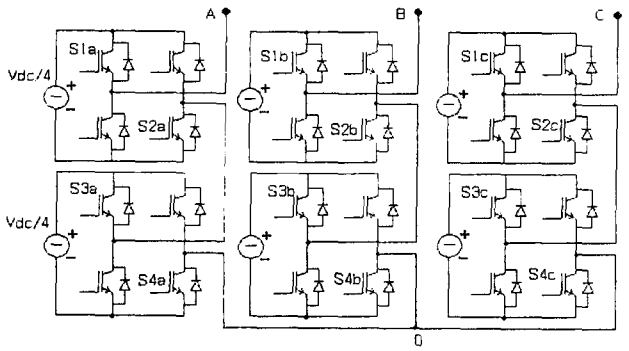

Figure 2: Circuit diagrams of five-level cascade inverter.

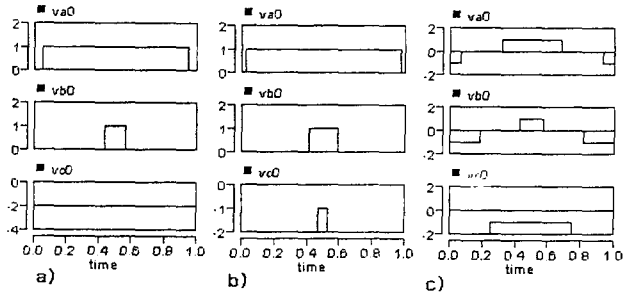

Figure 3: Different sequences of voltage states va0,vb0 and vc0 with a) three switching states, b) four switching states and c) six switching states.

The reference $\vec{V}^*$ consists of active component $\vec{V}_{12} = V_{12}.\exp(j\theta) = [v_{a12}, v_{b12}, v_{c12}]^T$ and zero sequence component $\vec{V}_0 = v_0[1,1,1]^T$. Let's define fundamental modulating function of the three signals $(v_{ra(1)}, v_{rb(1)}, v_{rc(1)})$ as $v_{ra(1)} = \dfrac{V_{12}}{V_{dc}/(n-1)}.\cos\theta$,

$$v_{rb(1)} = \frac{V_{12}}{V_{dc}/(n-1)}.\cos(\theta - 2\pi/3)$$

$$v_{rc(1)} = \frac{V_{12}}{V_{dc}/(n-1)}.\cos(\theta - 4\pi/3). \qquad (3)$$

Let's define functions max and min are the largest and smallest values from among $(v_{ra(1)}, v_{rb(1)}, v_{rc(1)})$ and function *mid* is equal to one between the max and min values. The parameters K_1 , K_2 and K_3 are proportional to switching time durations T_1, T_2 and T_3 of three pivot vectors and they can be calculated as follows [7],[8]:

$$\left.\begin{aligned} K_1 &= 1 + \text{int}[\max - \min] - (\max - \min) \\ K_2 &= -\text{int}[\max - mid] + (\max - mid) \end{aligned}\right\} \text{for } TVMINR - areas$$

$$\left.\begin{aligned} K_1 &= 1 + \text{int}[mid - \min] - (mid - \min) \\ K_2 &= 1 + \text{int}[\max - mid] - (\max - mid) \end{aligned}\right\} \text{for } TVMAXR - areas$$

$$K_3 = 1 - K_1 - K_2 \qquad (4)$$

where the conditions for TVMINR (two vectors with minimum level of redundancy) and TVMAXR (two vector with maximum level of redundancy) areas are:

$$S = Int[\max - \min] - Int[\max - mid] - Int[mid - \min]$$

$$S = \begin{cases} 0 & for \quad TVMINR \quad - areas \\ 1 & for \quad TVMAXR \quad - areas \end{cases} \qquad (5)$$

Under the consideration of the existing redundancies of three pivot voltage vectors, a complete expression of the reference vector can be performed as follows:

$$\begin{aligned} \vec{V} = K_1.&\left(\xi_{10}.\vec{U}_{10} + \xi_{11}\vec{U}_{11} + \xi_{12}\vec{U}_{12} + ... + \xi_{1,lr1}\vec{U}_{1,lr1}\right) + \\ K_2.&\left(\xi_{20}.\vec{U}_{20} + \xi_{21}\vec{U}_{21} + \xi_{22}\vec{U}_{22} + ... + \xi_{2,lr2}\vec{U}_{2,lr2}\right) + \\ K_3.&\left(\xi_{30}.\vec{U}_{30} + \xi_{31}\vec{U}_{31} + \xi_{32}\vec{U}_{32} + ... + \xi_{3,lr3}\vec{U}_{3,lr3}\right) \end{aligned} \qquad (6)$$

where the parameters l_{rj} , corresponding to the vectors $\vec{U}_j$, $j = 1,2,3$ termed as levels of vector redundancies are determined for an n-level inverter as follows:

$$l_{r1} = n - 1 - \text{int}[\max - \min]; \quad l_{r3} = l_{r1} - 1 \qquad (7)$$

$$l_{r2} = n - 1 - \text{int}[mid - \min] - Int[\max - mid] - 1$$

The distribution of the switching time durations of vector redundancies defined by the parameters ξ_{jk} , $j = 1,2,3$, $k = 0,1,2,..,l_{rj}$ will meet the following conditions as

$$\xi_{j0} + \xi_{j1} + \xi_{j2} + ... + \xi_{j,lrj} = 1 \;\; ; \;\; \xi_{jk} \geq 0 , \qquad (8)$$

The redundant vectors $\vec{U}_{j0}, \vec{U}_{j1}, ...\vec{U}_{jlrj}$, $j = 1,2,3$, which are related to the voltage vector $\vec{U}_j$ are arranged in an increasing sequence of their zero sequence voltages. It means:

$$U_{aj0} + U_{bj0} + U_{cj0} < U_{aj1} + U_{bj1} + U_{cj1} < .... < U_{aj,lrj} + U_{bj,lrj} + U_{cj,lrj} \qquad (9)$$

Three vectors $\vec{U}_{10}, \vec{U}_{20}$ and $\vec{U}_{30}$ with the lowest zero sequence voltages are termed as the lowest redundant vectors. In a triangle area, they are arranged in an increasing sequences of their zero sequence voltages as follows:

$$U_{a10}+U_{b10}+U_{c10}<U_{a20}+U_{b20}+U_{c20}<U_{a30}+U_{b30}+U_{c30} \quad (10)$$

Modulating pattern (MP) can be defined as a set of three phase small signals of a pivot voltage vector $\vec{U}_j$ and derived from the dc-voltage source V_{dc} as follows:

$$\vec{P}_j = \vec{U}.(n-1)/V_{dc} = [P_{aj}, P_{bj}, P_{cj}]^T. \quad (11)$$

Each component of the MP as P_{aj}, P_{bj} and P_{cj} is called *a phase modulating pattern (PMP)*. All the MPs are presented in a MP vector diagram (fig.1b). The MPs and the MP diagram are valid to both multilevel inverter topologies.

In triangle area , where the reference vector is located, three lowest MP (ZRC MP) can be determined as follows:

$$[P_{a10}, P_{b10}, P_{c10}]^T = [P_{\min}, P_{\min}, P_{\min}]^T +$$
$$+[Int[v_{ra(1)} - \min], Int[v_{rb(1)} - \min], Int[v_{rc(1)} - \min]]^T$$
$$[P_{a20}, P_{b20}, P_{c20}]^T = [P_{a10}, P_{b10}, P_{c10}]^T + [f_a, f_b, f_c]^T$$
$$[f_a, f_b, f_c]^T = \begin{cases} [f_{\max a}, f_{\max b}, f_{\max c}]^T & for \quad S=0 \\ [f_{mida}, f_{midb}, f_{midc}]^T & for \quad S=1 \end{cases}$$
$$[P_{a30}, P_{b30}, P_{c30}]^T = [P_{a10}, P_{b10}, P_{c10}]^T +$$
$$[f_{mida} + f_{\max a}, f_{midb} + f_{\max b}, f_{midc} + f_{\max c}]^T \quad (12)$$

The vector $[f_{\max}]$ *is described as follows:*

$$[f_{\max x}] = [f_{\max a}, f_{\max b}, f_{\max c}], \quad (13)$$

where its component is defined as

$$f_{\max x} = \begin{cases} 1 & for \quad v_{rx(1)} = \max \quad x = a,b,c \\ 0 & else \end{cases}. \quad (14)$$

Similarly, the vector $[f_{mid}]$ is described as follows:

$$[f_{midx}] = [f_{mida}, f_{midb}, f_{midc}] \quad (15)$$

where its component is defined as

$$f_{midx} = \begin{cases} 1 & for \quad v_{rx(1)} = mid \quad x = a,b,c \\ 0 & else \end{cases}. \quad (16)$$

The value $P_{\min}$ is the smallest value from among MP components in the MP diagram.

Any modulating pattern $\vec{P}_j$ can be determined from the corresponding ZRC MP as follows:

$$\vec{P}_j = \vec{P}_{j0} + \eta_j.\vec{I}\ ;\ 0 \le \eta_j \le l_{rj}, j = 1,2,3 \quad (17)$$

where $\vec{I} = [1,1,1]^T$ is a unit vector and the parameters l_{rj} ($j = 1,2,3$) defined in (7). For $\eta_j = 0 \Rightarrow \vec{P}_j = \vec{P}_{j0}$.

3. The correlation between the CPWM methods and the SVPWM method for multilevel inverter

3.1 The correlation between the multi-carrier single modulating system and the SVPWM

The multi-carrier SMS CPWM (or CPWM) technique has been used widely for its simplicity. For producing a pivot voltage vector, the modulating signals can be simply selected identical to the corresponding MP $\vec{P}_j$ defined in (11). For instance, the modulating pattern (-2,-1,0) corresponds to pivot vector with its three phase voltages $(-2.V_{dc}/n, -V_{dc}/n, 0)$. In the CPWM, three limit modulating signals with subsequent values equal to $(P_a = -2, P_b = -1, P_c = 0)$ are required for generating the previous voltage vector. Therefore, the MP represents a set of modulating signals for performing the corresponding voltage pivot vector. From (6) and (11), the CPWM equation which describes the reference modulating signals $\vec{v}_r = [v_{ra}, v_{rb}, v_{rc}]^T$ can be expressed as follows :

$$\vec{v}_r = \sum_{j=1}^{3} K_j.(\xi_{j0}.\vec{P}_{j0} + \xi_{j1}.\vec{P}_{j1} + \xi_{j2}.\vec{P}_{j2} + ... + \xi_{j,lrj}.\vec{P}_{j,lrj}) \quad (18)$$

The number of modulating patterns of each pivot vector $\vec{U}_j$ $j = 1,2,3$ is limited to a maximum value of two. At least four out of related coefficients $\xi_{j,Nj1}, \xi_{j,Nj2}$ are integer. Beside that the following conditions are satisfied as

$$\xi_{10} = \xi_{11} = ... = \xi_{1,N10} = 0 \ ;\ (\xi_{1,N11} + \xi_{1,N12}) = 1 \ ;$$
$$\xi_{1,N13} = ... = \xi_{1,lr1} = 0$$
$$\xi_{20} = \xi_{21} = ... = \xi_{2,N20} = 0 \ ;\ (\xi_{2,N21} + \xi_{2,N22}) = 1 \ ;$$
$$\xi_{2,N23} = ... = \xi_{2,lr2} = 0$$
$$\xi_{30} = \xi_{31} = ... = \xi_{3,N30} = 0 \ ;\ (\xi_{3,N31} + \xi_{3,N32}) = 1 \ ;$$
$$\xi_{3,N33} = ... = \xi_{3,lr3} = 0 \quad (19)$$

where $N_{11}, N_{12}, ..., N_{32}$ are integer numbers.

Substituting (17) and (19) into (18), we can obtain CPWM equation of the SMS as follows:

$$\vec{v}_r = K_1.[\vec{P}_{10} + (N_{11} + \xi_{1,N12}).\vec{I}] + K_2.[\vec{P}_{20} + (N_{21} + \xi_{2,N32}).\vec{I}]$$
$$+ K_3.[\vec{P}_{30} + (N_{31} + \xi_{3,N32}).\vec{I}] \quad (20)$$

or in a simple form as

$$\vec{v}_r = K_1.\vec{P}_{10} + K_2.\vec{P}_{20} + K_3.\vec{P}_{30} + (\eta_1.K_1 + \eta_2.K_2 + \eta_3.K_3).\vec{I} \quad (21)$$

where for the redundant parameters η_1, η_2 and η_3 , the conditions are satisfied as

$$N_{j1} = Int[\eta_j]\ ;\ \xi_{j,Nj2} = \eta_j - N_{j1}\ ,\ \xi_{j,Nj1} = 1 - \xi_{j,Nj2}\ ;$$
$$(\eta_3 + 1) \ge \eta_1 \ge \eta_2 \ge \eta_3 \ge 0\ ;\ j = 1,2,3 \quad (22)$$

From (21), the correlation between the SVPWM and the CPWM represented by a general zero sequence function can be determined as follows [7],[8]:

$$v_{r0} = P_{\min} - \min + \eta_1.K_1 + \eta_2.K_2 + \eta_3.K_3 \quad (23)$$

The minimum and maximum values of the function v_{r0} can be determined substituting ($\eta_1 = \eta_2 = \eta_3 = 0$) and ($\eta_1 = l_{r1}$, $\eta_2 = l_{r2}$ and $\eta_3 = l_{r3}$), respectively. The obtained results are expressed as follows:

$$v_{r0\min} = P_{\min} - \min \text{ and } v_{r0\max} = n - 1 + P_{\min} - \max \quad (24)$$

In (23), the parameter $P_{\min}$ presents a lower limit of the carrier system and the parameters max, mid and min introduce the influence of the fundamental voltages. The SMS CPWM performance will depend on the defined redundant factors η_1, η_2 and η_3.

3.2. The correlation between the multi-carrier multi-modulating system and the SVPWM

a) **Multi-modulating pattern**

In a multi-modulating system (MMS), each phase voltage is controlled by a set of p-modulating signals , p>1. Each modulating signal is used to control s switching pairs. If s=1, there are p=(n-1) signals per phase. This system is defined as a full modulating system. For 1<p<(n-1), the system is simpler, however its redundant capability will appropriately decrease. In the SMS, for producing a MP, each modulating signal is set equal to the value of corresponding MP component. In the MMS, a p-modulating signal set will produce a modulating pattern (MP). Each standard p-modulating signal set determines a phase voltage output and called as a phase MMP (PMMP). A combination of three phase MMP performs multi-modulating pattern (MMP), which can be derived from the circuit diagram and related switching rules.

The MMP can be considered as an extension of the MP, where the vector elements in CPWM equation are replaced by corresponding matrix elements. For a full MMS, each MMP has a [3x(n-1)]-dimension and fully determines switching characters of multilevel inverter.

The mathematical description of the matrix MMP $[\dot{Q}_j]$ is as follows:

$$[\dot{Q}_{jk}]=\begin{bmatrix} Q_{ajk1} & Q_{ajk2} & Q_{ajkp} \\ Q_{bjk1} & Q_{bjk2} & \cdots Q_{bjkp} \\ Q_{cjk1} & Q_{cjk2} & Q_{cjkp} \end{bmatrix} ; \quad \begin{matrix} 1 \le p \le (n-1) \\ k = 0,1,2,\ldots l_{r1}, l_{r2}, l_{r3} \end{matrix}$$

$$j = 1,2,3 . \qquad (25)$$

where (Q_{ajk1}, Q_{ajk2}, ..., Q_{ajkp}), (Q_{bjk1}, Q_{bjk2}, ..., Q_{bjkp}) and (Q_{cjk1}, Q_{cjk2}, ..., Q_{cjkp}) are three *PMMP* sets, corresponding to three *PMP*s as P_{aj}, P_{bj} and P_{cj}.

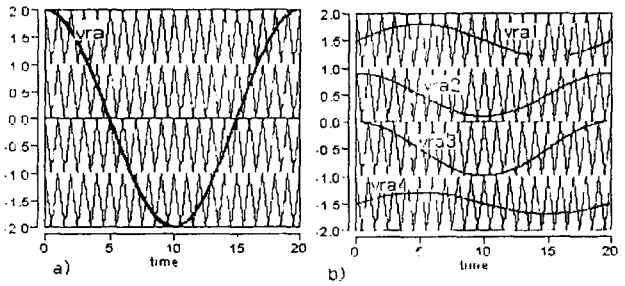

Figure 4: Five-level inverter: the diagrams of carrier waves and A-phase modulating signals of a) the multi-carrier SMS, b) the full multi-carrier MMS.

Full modulating system –in five-level inverter, a full MMS requires four modulating signals per phase for instance A-phase signals v_{ra1}, v_{ra2}, v_{ra3} and v_{ra4} as shown in fig.4b, which vary in the corresponding ranges of (1,2),(0,1),(-1,0), and (-2,-1), respectively. Intersections between these signals with the carrier waves u_{p1} ($1 \le u_{p1} \le 2$), u_{p2} ($0 \le u_{p2} \le 1$) , u_{p3} ($-1 \le u_{p3} \le 0$), and u_{p4} ($-2 \le u_{p4} \le -1$) will determine switching states of the corresponding switching pairs S1a,S2a,S3a, and S4a, respectively. For instance, to obtain the A-phase output equal to $V_{dc}/2$ (PMP=2), the states of switching pairs will be $S_{1a} = S_{2a} = S_{3a} = S_{4a} = ON$. This can be satisfied by *PMMP* set consisting of 4 signals as $v_{ra1} = 2, v_{ra2} = 1, v_{ra3} = 0$ and $v_{ra4} = -1$, or in short PMMP (2,1,0,-1). Similarly, the other *PMMP* s can be deduced and filled in table 4.

Table 4. Phase multi-modulating pattern (*PMMP*) of five-*level diode-clamped inverter with full MMS*

PMP	-2	-1	0	1	2
PMMP	(1,0,-1,-2)	(1,0,-1,-1)	(1,0,0,-1)	1,1,0,-1	(2,1,0,-1)

Table 5. Phase multi-modulating pattern (*PMMP*) o f five-level cascade inverter with full MMS

PMP	-2	-1	0	1	2
PM MP	1,0,-1,-2)	(2,0,-1,-2) (1,1,-1,-2) (1,0,0,-2) (1,0,-1,-1)	(1,1,-1,-1 (2,0,0,-2) (2,0,-1,-1 (2,1,-1,-2 (1,1,0,-2) (1,0,0,-1)	(2,0,0,-1) (2,1,-1,-1 (2,1,0,-2) (1,1,0,-1)	(2,1,0,-1)
Set 1	1,0,-1,-2)	(1,0,-1,-1)	(1,0,0,-1)	(1,1,0,-1)	(2,1,0,-1)
Set 2	(1,0,-1,-2)	(2,0,-1,-2)	(2,0,-1,-1)	(2,0,0,-1)	(2,1,0,-1)
Set 3	(1,0,-1,-2)	(1,1,-1,-2)	(1,1,-1,-1)	(2,1,-1,-1)	(2,1,0,-1)
Set 4	(1,0,-1,-2)	(1,0,0,-2)	(2,0,0,-2)	(2,1,0,-2)	(2,1,0,-1)
.....	There are total 4!=24 sets				

For diode clamped inverter, there is only one set of PMMP. For a cascade inverter, in a similar process, all the *PMMP*s can be described in table 5. There is only one *PMMP* for generating the *PMP* -2 , *PMP* 2, four *PMMP*s for generating the *PMP* -1, *PMP* 1 and six *PMMP*s for generating the *PMP* zero. Any *MP* can be implemented by several *MMP* s. For instance, the MP (-2,1,2) can be generated by one of four *MMP*s described as follows :

$$\begin{bmatrix} 1,0,-1,-2 \\ 2,0,0,-1 \\ 2,1,0,-1 \end{bmatrix} \begin{bmatrix} 1,0,-1,-2 \\ 2,1,-1,-1 \\ 2,1,0,-1 \end{bmatrix} \begin{bmatrix} 1,0,-1,-2 \\ 2,1,0,-2 \\ 2,1,0,-1 \end{bmatrix} \begin{bmatrix} 1,0,-1,-2 \\ 1,1,0,-1 \\ 2,1,0,-1 \end{bmatrix}.$$

The set of the *PMMP*s would be selected so that two following patterns, which correspond to two subsequent *PMP*s, differ only one switching state. For instance, four sets from 1 to 4 in table 5 are applicable, since each modulating signal changes only once while the *PMP* varies from -2 to 2. In contrary, the *PMMP* set of (1,0,-1,-2), (2,0,-1,-2), (1,0,0,-1),(2,1,-1,-1) and (2,1,0,-1) will not valid.

b) The correlation between SVPWM and CPWM for a multi-carrier multi-modulating system

A general formulation of CPWM in a MMS with p modulating signals per phase can be expressed as follows:

$$[\bar{V}_r] = \sum_{j=1}^{3} K_j \left(\xi_{j0} [\dot{Q}_{j0}] + \xi_{j1} [\dot{Q}_{j1}] + \ldots + \xi_{jlrj} [\dot{Q}_{jlrj}] \right) \qquad (26)$$

where

$$[\vec{v}_r]=\begin{bmatrix} v_{ra1}\, v_{ra2}\cdots v_{rap} \\ v_{rb1}\, v_{rb2}\cdots v_{rbp} \\ v_{rc1}\, v_{rc2}\cdots v_{rcp} \end{bmatrix};[\vec{Q}_{jk}]=\begin{bmatrix} Q_{ajk,1}\, Q_{ajk,2}\cdots Q_{ajkp} \\ Q_{bjk,1}\, Q_{bjk,2}\cdots Q_{bjkp} \\ Q_{cjk,1}\, Q_{cjk,2}\cdots Q_{cjkp} \end{bmatrix};$$

$$j=1,2,3 \qquad k=0,1,2,..,l_{r1}/l_{r2}/l_{r3} \qquad (27)$$

The combinations $(v_{ra1}, v_{ra2}...v_{rap})$, $(v_{rb1}, v_{rb2}...v_{rbp})$ and $(v_{rc1}, v_{rc2}...v_{rcp})$ are three p-modulating signal sets, corresponding to A-,B- and C- phase voltages. A maximum number of switching states, which can be possibly implemented, will depend on the proposed MMS. For a full modulating system, a maximum of $(l_{r1}+l_{r2}+l_{r3}+3)$ states can be involved in a switching sequence. The meaning of the (26) is that: if a set of the reference modulating signals is generated by (26), the output voltage vector will be implemented by a sequence of the related redundant vectors as $\vec{U}_{10}, \vec{U}_{20}, \vec{U}_{30}, \vec{U}_{11}, \vec{U}_{21}.....\vec{U}_{1,lr1}, \vec{U}_{2,lr2}, \vec{U}_{3,lr3}$, their switching time durations are proportional to the corresponding coefficients as $K_1\xi_{10}, K_2\xi_{20}, K_3\xi_{30}, K_1\xi_{11}, K_2\xi_{21}.....K_1\xi_{1,lr1}$, $K_2\xi_{2,lr2}, K_3\xi_{3,lr3}$, respectively.

Each *MMP* in (26) will be derived from its corresponding MP, which for instance can be determined from the vector redundant factors. The method to determine a MP and its coefficients will depend on the individual required application.

For the demonstration, the first *PMMP* set in table 5 can be applied to both inverter topologies, consisting of the following *PMMP* s as (1,0,-1,-2),(1,-1,-1),(1,0,0,-1),(1,1,0,-1) and (2,1,0,-1). The three remaining sets can be applied only for cascade inverter.

The reference modulating signals in the following figures are derived for the fundamental voltages equal to $\frac{\sqrt{3}Vdc}{4\sqrt{3}}$. In fig.5, the redundant parameters are selected as $\xi_{10}=\xi_{11}=0.5$ and $\xi_{20}=\xi_{30}=1$, corresponding to a switching sequence of the vectors $\vec{U}_{10}, \vec{U}_{20}, \vec{U}_{30}$ and $\vec{U}_{11}$. Two active redundant vectors $\vec{U}_{10}$ and $\vec{U}_{11}$ are centered in a half sampling period. In fig.6, the redundant parameters are set as $\xi_{10}=\xi_{11}=\xi_{20}=\xi_{21}=0.5$ and $\xi_{30}=1$, corresponding to a switching sequence of the vectors $\vec{U}_{10}, \vec{U}_{11}, \vec{U}_{20}, \vec{U}_{21}$ and $\vec{U}_{30}$. From among them, there are two pairs of active redundant vectors as $\vec{U}_{10}, \vec{U}_{11}$ and $\vec{U}_{20}, \vec{U}_{21}$

In fig.7, the diagrams illustrate a phase redundancy control by substituting subsequently four *PMMP* sets from table 5 into CPWM equation (26). Discontinuous PWM mode using three vectors $\vec{U}_{10}, \vec{U}_{20}, \vec{U}_{30}$ $(\xi_{10}=\xi_{20}=\xi_{30}=1)$ occurs. With different *PMMP* sets, the phase redundant control alternates switching pairs and redistributes the switching losses among them.

As can be seen from the diagrams in fig.5 and fig.7, that the described "modular" PWM method or PD discontinuous PWM in cascade inverter [3],[4] is just a special case of the full MMS.

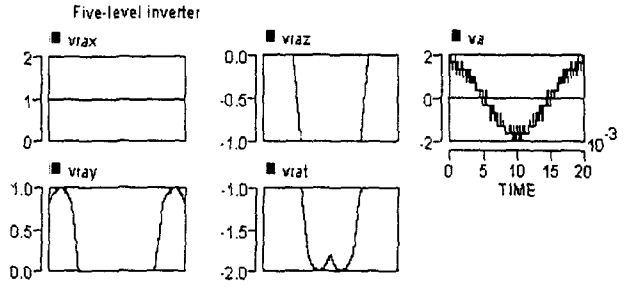

Figure 5: Five-level inverter- Equally-centered PWM with four switching states: Diagrams of modulating signal set of the A-phase and output phase voltage for m=0.75.

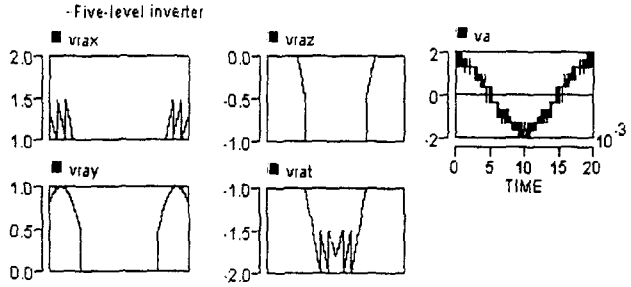

Figure 6: Five-level inverter- Equally-centered PWM with five switching states: Diagrams of modulating signal set of the A-phase and output phase voltage for m=0.75..

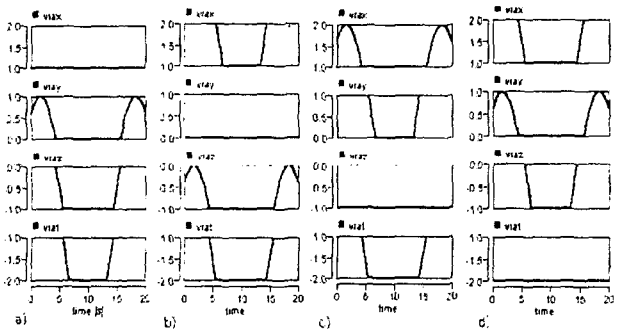

Figure 7: Five-level inverter Discontinuous PWM: Diagrams of the A-phase modulating signal sets for various selected PMMP modulating patterns, m=0.75.

Conclusions:

In this part, it has been introduced a generalized correlation between SVPWM and CPWM methods. It has been shown that the SVPWM can be equivalently implemented by the corresponding CPWM. The multi-modulating patterns have been presented as basic elements for the multi-modulating CPWM methods. The multi-modulating system gives rise to a maximum number of switching states and utilizes phase redundancies by alternating modulating pattern sets. These advantages can be applicable for improving the PWM performances of multi-level inverters.

References (see the continued paper of the same title–Part2)