High Efficiency and Low Device Stress Voltage and Current Clamping ZVS PWM Asymmetrical Half Bridge Converter

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Abstract—**A high efficiency and low device stress voltage and current clamping ZVS PWM asymmetrical half bridge converter is proposed in this paper. To achieve the ZVS of power switches along the wide load range, the transformer leakage inductor L_{lkg} is increased. Then, to solve the problem related to ringing in the secondary rectifier caused by the resonance between L_{lkg} and rectifier junction capacitors, the proposed converter employs a voltage and current clamping cell, which helps voltages and currents of rectifier diodes to be clamped at the output voltage and output current, respectively. Therefore, no RC-snubber for rectifier diodes is needed and a high efficiency as well as low noise output voltage can be realized. In addition, since all energy stored in L_{lkg} is transferred to the output side, the circulating energy problem can be effectively solved and duty loss does not exist. The operational principle, theoretical analysis, and design considerations are presented. To confirm the operation, validity, and features of the proposed circuit, experimental results from a 425W, 385-170Vdc prototype are presented.**

1. Introduction

A plasma display panel (PDP) is now expected as the most leading candidate for the large area wall-hanging color TVs, since it has advantages over conventional display devices by its large screen over 40-inch, wide view angle, lightness, thinness, long life time, and high contrast [1-3].

The operation of the PDP is divided into three periods of resetting, addressing, and sustaining periods. During the resetting period, all of PDP cells are erased and prepared to carry out addressing. Then, selective write-discharges to form a required image are ignited by applying the data and scanning pulses to the addressing and scanning electrodes, respectively. Since the addressing discharge itself emits an insufficient visible light, high voltage AC square pulses are continuously applied between sustaining and scanning electrodes for the strong light emission of selective cells during the sustaining period. Therefore, to carry out these operations successfully, the PDP must be equipped with the various kinds of power modules for sustaining, erasing, addressing, and scanning operations, etc [1-3].

Meanwhile, since most of the power required to drive the PDP is consumed during the sustaining period, that for sustaining operation among abovementioned power modules are mainly responsible for the overall system efficiency and size. In addition, since the recent wall hanging PDP color TV tends to require the smaller size, lighter weight, and fan-less system for the lower acoustic noise and vibration, the high power density, high performance, and high efficiency become the hot issue of the PDP power module [1-3]. Among various ZVS-PWM DC/DC converters hitherto developed, a half bridge converter suitable for the mid power (about 400W~500W) application like the PDP power module has been proposed to reduce the component current/voltage stress and switching losses. However, since this converter is required to have the large leakage inductor to achieve the ZVS of power switches for the wide load range, it has several serious problems such as a large circulating energy, low system efficiency, serious parasitic ringing in the secondary rectifier, considerable heating, bulky cooling system, and noisy output voltage. Especially, in the case of the high output voltage applications like the PDP sustaining power module, the resistor-capacitor (RC) snubber to absorb the serious ringing voltage across the secondary rectifier degrades the overall system efficiency, since the energy stored in the snubber capacitor is not only very large but also all dissipated through the snubber resistor [4, 5].

Therefore, to overcome these problems, a new high efficiency and low device stress voltage and current clamping ZVS PWM asymmetrical half bridge converter well suited to the PDP Sustaining Power Module (PSPM) is proposed in this paper as shown in Fig. 1. It can effectively overcome the abovementioned all problems of the prior circuit and realize the high power density, high performance, and high efficiency. More detailed features and operational principles of the proposed converter will be described in following chapters.

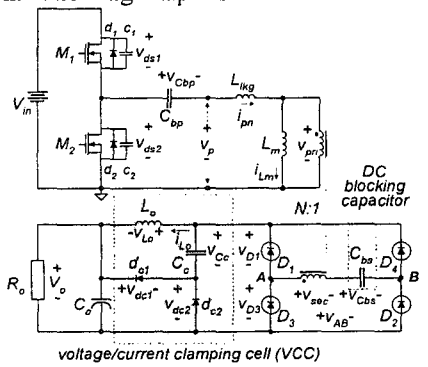


Fig. 1. ZVS PWM half bridge converter

2. Structure and features of proposed converter

To achieve the ZVS of power switches for the wide load range, a somewhat large inductor is required like the prior ZVS PWM half bridge converter.

However, same abovementioned problems as the prior circuit caused by the large inductor are inevitable. To solve the problem related to the serious ringing in the secondary rectifier, the voltages across the output rectifier diodes has

to be clamped at any voltage source, which can be effectively accomplished by adding the proposed voltage current clamping cell (VCC) between the output rectifier and output inductor as shown in Fig. 1. Therefore, an RC snubber to absorb the ringing voltage is not necessary and the high efficiency as well as low noise output voltage can be realized.

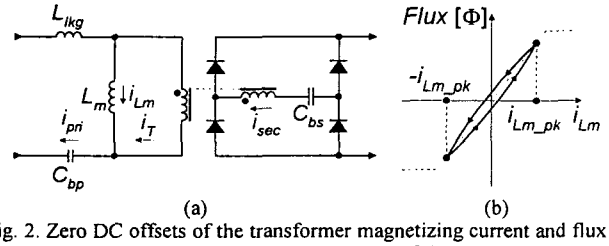


Fig. 2. Zero DC offsets of the transformer magnetizing current and flux (a) transformer magnetizing current (b) B-H curve of the magnetic core

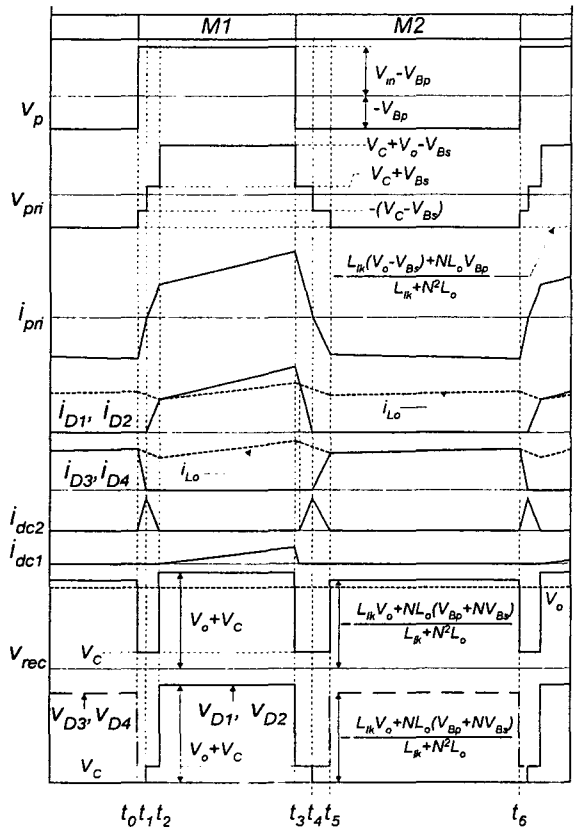


Fig. 3 Operational key waveforms of the proposed circuit

Moreover, since all energy stored in L_{lkg} is transferred to the output side until the current flowing through L_{lkg} becomes 0A, the circulating energy problem, which could be more increased according to the larger leakage inductor in the prior approach, can be effectively solved.

Fig. 2 shows the zero DC offset characteristics of the transformer magnetizing current in the proposed converter. From the fact that the DC value of the current through the capacitor is 0A, the DC values of i_{pri} and i_{sec} (i. e. $<i_{pri}>$ and $<i_{sec}>$, respectively) are all 0A, where $<\bullet>$ means the DC value of '•'. Since i_T is equal to i_{sec}/N, $<i_T>=<i_{sec}/N>=0A$. And, since i_{Lm} is equal to $i_{pri}-i_T$, $<i_{Lm}>=<i_{pri}>-<i_T>=0A$, which means that the DC offsets of the transformer magnetizing current and flux can be completely blocked. Therefore, the RMS (root mean square) value of the primary currents can be minimized and the transformer magnetic core fully utilized compared with the prior circuit as shown in Fig. 2, and thus, its power density can be considerably increased.

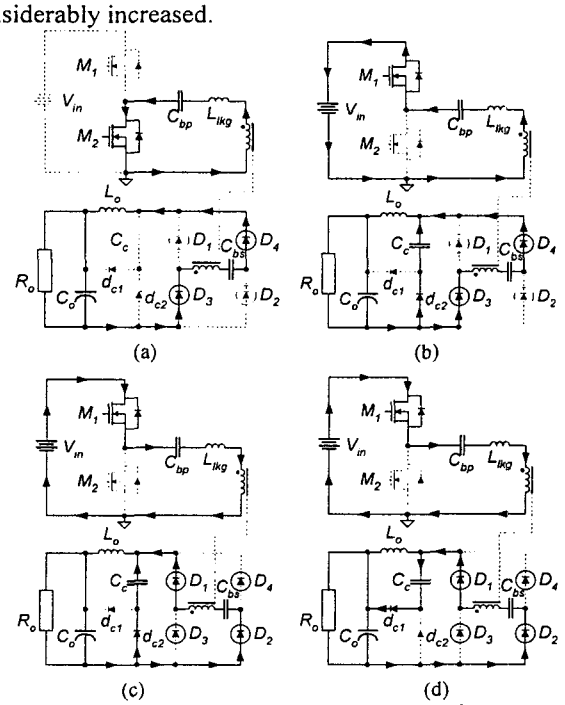


Fig. 4 Operation modes of the proposed converter, (a) Before t_0 (b) Mode 1 (t_0~t_1) (c) Mode 2 (t_1~t_2) (d) Mode 3 (t_2~t_3)

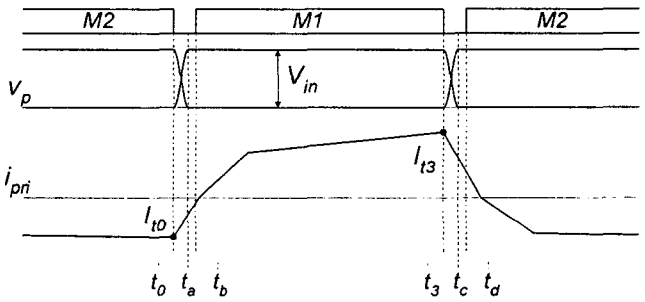


Fig. 5 ZVS transition of power switches

3. Operational principles of proposed circuit

Fig. 3 shows the key waveforms of the proposed converter. One cycle period of the proposed circuit is divided into two half cycles, t_0~t_3 and t_3~t_6. Since the operational principles of two half cycles are symmetric, only the first half cycle is explained. The driving method of the proposed circuit is the same as that of the conventional asymmetrical half bridge converter. The switches M_1 and M_2 are turned on and off in a complementary way to each other. And, M_1 is driven with the duty ratio D, which is less than 0.5. To illustrate the steady-state operation, all parasitic components except for those specified in Fig. 1 are assumed to be neglected, where c_1, c_2, d_1 and d_2 are not additional components but parasitic capacitors and anti-parallel diodes of MOSFETs and L_{lkg} represents the transformer leakage component. The switch M_2 is assumed to be initially in turn-on states before t_0. Therefore, the energy stored in C_{bp} is powered to the output stage as shown in Fig 4 (a). The analysis of the proposed circuit begins when the switch M_2 is turned off and M_1 is turned on.

Mode 1 (t_0~t_1): When M_2 is turned off at t_0, mode 1 begins. With the initial conditions of $i_{pri}(t_0)=-I_{t0}$, $v_{ds1}(t_0)=V_{in}$, and $v_{ds2}(t_0)=0$, the current i_{pri} flowing through L_{lkg} charges C_2 and discharges C_1 as $v_{ds1}(t)=V_{in}-I_{to}/(2C_{oss})(t-t_0)$ and $v_{ds2}(t)=I_{to}/(2C_{oss})(t-t_0)$ where C_1 and C_2 are equal to C_{oss} and L_{lkg} acts as a current source with the value of I_{t0} in this interval. After the voltage across C_1 is decreased to 0V, d_1 starts conducting at t_a as shown in Fig. 5. Therefore, the voltage across M_1 is maintained at 0V. Since d_1 is conducting before t_a, M1 can be turned on with the ZVS at t_b. Since the primary current i_{pri} is still flowing in the same direction, the secondary current i_{sec} is also flowing in the same direction as that of the previous mode and output rectifier diodes D_3 and D_4 are on the conductive state as shown in Fig. 4 (b). Meanwhile, since the current i_{sec} through D_3 and D_4 becomes smaller than I_{Lo}, d_{c2} starts conducting and the energy stored in capacitor C_c being transferred to the load side.

Mode 2 (t_1~t_2): When the primary current i_{pri} becomes 0A, mode 2 begins at t_1. Since the direction of the primary current i_{pri} is reversed, the current i_{sec} starts flowing through D_1 and D_2 instead of D_3 and D_4 and the input power being transferred to the input side as shown in Fig. 4 (c).

Mode 3 (t_2~t_3): When the secondary current i_{sec} is equal to the output inductor current i_{Lo}, d_{c2} is blocked at t_2 as shown in Fig. 4(d). At the same time, since the current i_{sec} through D_1 and D_2 is larger than I_{Lo}, C_c is charged through d_{c1} and the input energy is transferred to the load side.

The circuit operation of t_3~t_6 is similar to that of t_0~t_3. Subsequently, the operation from t_0 to t_6 is repeated.

4. Analysis of the proposed converter

4.1. Voltage conversion ratios

For the convenience of the analysis of the steady-state operation, several assumptions are made as follows:

- The proposed converter is operating in the continuous conduction mode (CCM).
- All parasitic components except for the leakage inductor are neglected
- The dead time between M_1 and M_2 is discarded.
- The conductive period DT_s of M_1 is less than $0.5T_s$.
- The commutation time between two pairs of output diodes is discarded.
- The capacitors C_{bp}, C_{bs}, C_c, and C_o are large enough to be considered as a constant voltage source V_{Cbp}, V_{Cbs}, V_{Cc}, and V_o, respectively.
- Since time intervals t_0~t_2 and t_3~t_4 in Fig. 3 are much smaller than the switching period T_s, they can be discarded.
- The magnetizing inductor L_m is much larger than L_{lkg}.
- The magnetizing inductor L_m is so large that $i_{Lm}=0$.
- The output inductor L_o is much larger than L_{lkg} and thus, L_o is considered to be constant current source I_o.

Based on abovementioned assumptions, the key waveforms of V_{AB}, i_{pri}, and V_{Lo} can be simplified as shown in Fig. 6.

By imposing the voltage-second balance rule on the magnetizing inductor L_m in the transformer primary side, the voltage V_{Cbp} can be obtained as

$$V_{Cbp} = DV_{in}. \quad (1)$$

Since the volt-second balance rule for the transformer secondary side must be satisfied, the steady state equation can be obtained from the waveform V_{AB} of Fig. 6 as

$$V_{Cbs} = DV_o - (1-2D)V_{Cc}. \quad (2)$$

Since the current-second balance rule for the primary DC blocking capacitor C_{bp} must be satisfied, the area S1 should be equal to the area S2 in the primary current i_{pri} of Fig. 6. Therefore, the following equation can be obtained.

$$-NV_o + 2NV_{Cbs} + (1-2D)V_{in} = 0. \quad (3)$$

Also, by imposing the voltage-second balance rule for the output inductor L_o in Fig. 6, the relationship between V_{Cc} and V_o can be obtained as

$$V_{Cc} = (1-D)V_o. \quad (4)$$

From equations (2) and (4), V_{Cbs} can be simply expressed as following:

$$V_{Cbs} = (4D-2D^2-1)V_o. \quad (5)$$

From equations (3) and (5), the steady state voltage conversion ratio between input and output voltages can be derived as following:

$$\frac{V_o}{V_{in}} = \frac{1}{N(3-2D)}. \quad (6)$$

From equations (4), (5), and (6), each capacitor voltage can be expressed as followings:

$$V_{Cc} = \frac{1-D}{N(3-2D)}V_{in} \quad (7)$$

$$V_{Cbs} = \frac{4D-2D^2-1}{N(3-2D)}V_{in}. \quad (8)$$

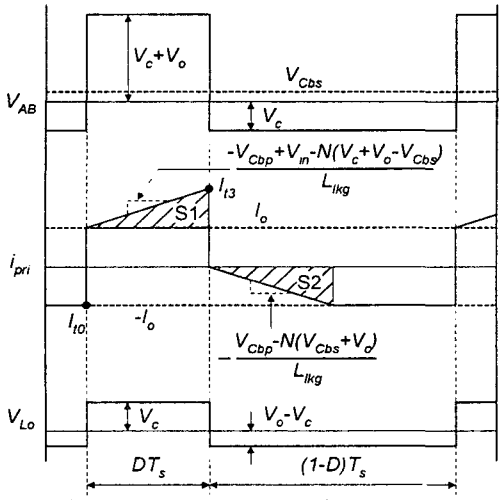


Fig. 6 Simplified voltage and current waveforms

4.2. Zero-voltage switching

From Fig. 5, to achieve the ZVS of switches, the energy E_{lkg_t0} stored in the leakage inductor L_{lkg} at t_0 must be large enough to fully charge C_2 and discharge C_1 before the switch M_1 is turned on. Similarly, the energy E_{lkg_t3} stored in the leakage inductor at t_3 must fully charge C_1 and discharge C_2 before the switch M_2 is turned on. Therefore,

to assure the ZVS of switches M_1 and M_2, the following equation must be satisfied.

$$E_{lkg\_t3} = \frac{1}{2} L_{lkg} I_{t_3}^2 \geq E_{lkg\_t_0} = \frac{1}{2} L_{lkg} I_{t_0}^2 \geq \frac{1}{2} 2C_{oss} V_{in}^2 \quad (9)$$

where C_1 and C_2 are assumed to be equal to C_{oss} and I_{t0} and I_{t3} are the peak currents through the leakage inductor at t_0 and t_3, respectively. From the simplified current waveforms shown in Fig. 6, I_{t0} and I_{t3} can be easily obtained as followings:

$$I_{t_0} \cong I_o \quad (10)$$

$$I_{t_3} \cong I_o + \frac{V_{in} - V_{Cbp} - N(V_c + V_o - V_{Cbs})}{L_{lkg}} DT_s . \quad (11)$$

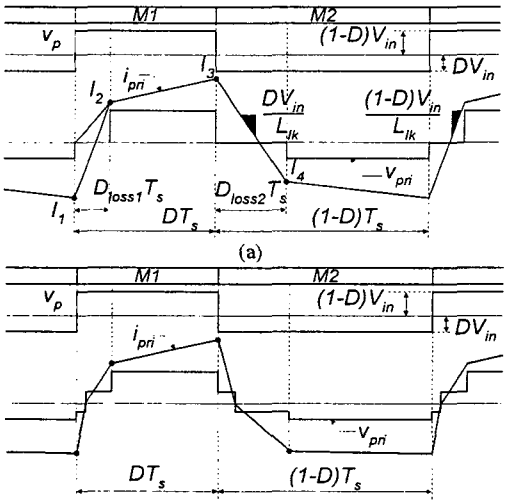


Fig. 7 Comparison of primary voltage and current waveforms, (a) Conventional half bridge converter (b) Proposed converter

4.3. Duty cycle loss and circulating current

The typical waveforms of the conventional half bridge converter and the proposed converter are compared as shown in Fig. 7. The operating duty cycle of the conventional circuit can be expressed as $D=D_{eff1}+D_{loss1}$ and $1-D=D_{eff2}+D_{loss2}$, where D_{eff1} and D_{eff2} mean the effective duty cycle and D_{loss1} and D_{loss2} mean the losses of the duty cycle.

The D_{loss1} and D_{loss2} can be expressed as

$$D_{loss1} = \frac{L_{lk}(I_1 + I_2)}{(1-D)T_s V_{in}}, \quad D_{loss2} = \frac{L_{lk}(I_3 + I_4)}{DT_s V_{in}} \quad (12)$$

where I_1, I_2, I_3, and I_4 are defined in Fig. 7 (a).

For the conventional half bridge converter, the leakage inductance should be large enough to provide a reasonable ZVS range. So, the loss of the duty cycle D_{loss1} and D_{loss2} are very large from the equation (12) and therefore, the effective powering period is decreased as shown in Fig. 7 (a), resulting in the increased circulating current and subsequent serious conduction loss. On the other hand, the proposed converter does not have any duty cycle loss and all energy stored in L_{lkg} is transferred to the output side until the current flowing through L_{lkg} becomes 0A as shown in Fig. 7 (b). Consequently, the circulating energy problem can be effectively solved.

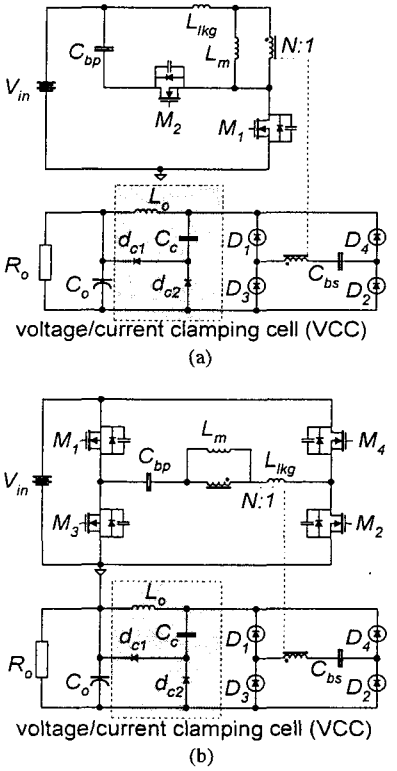


Fig. 8 Topological extension of the proposed circuit, (a) Active clamp forward converter (b) Full bridge converter

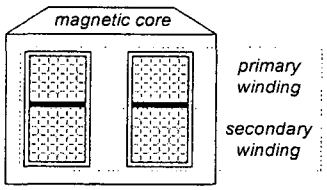
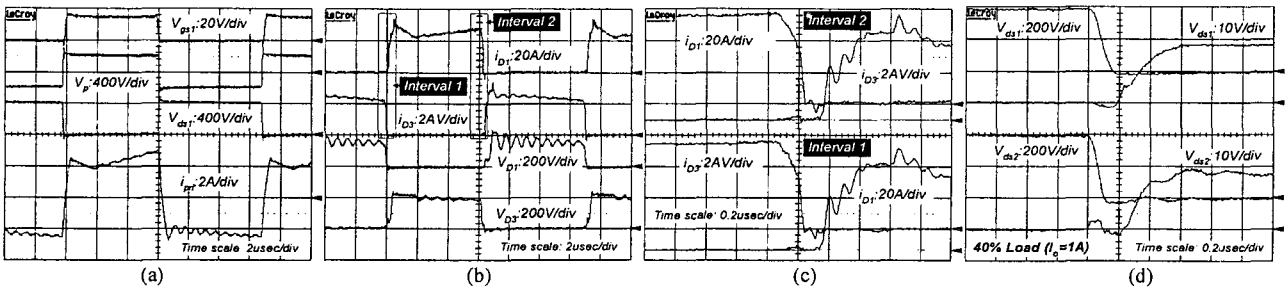


Fig. 10 The sectional view of the transformer having the large leakage inductance



(a) (b) (c) (d)

Fig. 9 Experimental waveforms, (a) Key waveforms of v_{gs1}, v_p, v_{ds1}, and i_{pri} (b) Key waveforms of i_{D1}, i_{D3}, v_{D1}, and v_{D3} (c) Transition intervals of i_{D1} and i_{D3} (d) ZVS turn on at 40% load

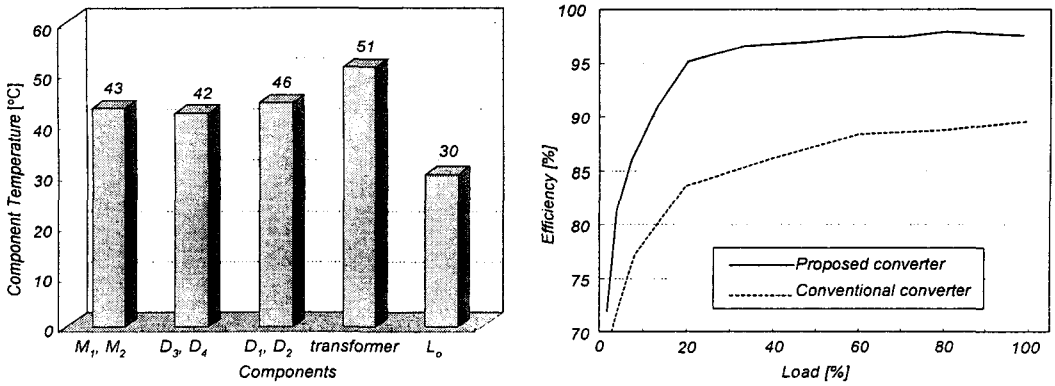


Fig. 11 Measured data from the prototype: (a) Component temperatures in operating the proposed converter for an hour, (b) Experimentally measured efficiency

5. Topological extensions of the proposed circuit

The concept presented to the proposed circuit in the previous section can be extended to any bridge-type DC/DC converter. Two kinds of bridge-type ZVS PWM DC/DC converters equipped with the proposed voltage/ current clamping cell are shown in Fig. 8. One is the active clamp forward converter and the other the asymmetrical full-bridge converter. The operational principles, features, and soft switching procedures of these converters are similar to that of the proposed circuit presented in section III.

6. Experimental results

The prototype of the proposed circuit is implemented with specifications of V_{in}=385V, V_o=170V, rated power P_o=425W, L_{lkg}=16uH, C_{bp}=C_{bs}=C_c=2.2uF, C_o=560uF/ 250V, transformer turns ratio N_1:N_2=21:23, M_1 and M_2= FQP13N50 (C_{oss}=245pF), d_1~d_4=15ETH03, and switching frequency=72kHz. To acquire the large leakage inductance, the transformer is manufactured as shown in Fig. 10. Therefore, no additional inductor is not needed and the system size and cost can be somewhat reduced. Fig. 9 (a) and (b) shows the experimental key waveforms at the full load. From these figures, since the voltages across D_1 and D_3 are clamped to V_o+V_{Cc} and turned off under zero current switching (ZCS) conditions, there is no serious voltage ringing in those diodes. Moreover, since the current overlap in each output diode, which is always observed in the conventional circuit, does not exit as shown in Fig. 9 (c), all energy stored in L_{lkg} is transferred to the output side and no circulating energy exists. Fig. 9 (d) shows that the ZVS of M_1 and M_2 can be achieved even at the 40% load condition. Fig. 11 (a) shows the component temperatures in operating the proposed converter for an hour, which is very important factor to determine the suitability of the developed converter to the commercial scale product. The temperatures of all components are below about 50°C except for the transformer (51°C). Fig. 11 (b) shows the measured efficiency. The maximum efficiency comes up to 97.3% and the efficiency along a wide load range is as high as above 95%.

7. Conclusion

A high efficiency and low device stress voltage and current clamping ZVS PWM asymmetrical half bridge converter for PSPM is proposed in this paper. The large leakage inductor can achieve the ZVS of all power switches along the wide load range. The problem related to ringing in the secondary rectifier caused by the large inductor can also be completely solved by employing a newly proposed VCC. Therefore, no RC-snubber for rectifier diodes is needed and a high efficiency as well as low noise output voltage can be realized. Moreover, since all energy stored in the additional inductor is transferred to the output side, the circulating energy problem can be effectively solved and the overall system efficiency along a wide load range is as high as above 95% (Maximum efficiency: 97.3%). The measured temperatures of all components are below about 50°C except for the transformer (51°C). These results mean that the proposed converter features the high efficiency, low device stress, high reliability, and small size due to the reduced heat sink. The proposed PSPM is expected to be well suited to the wall hanging color PDP TV.

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