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Low Power Memory-based FFT Processor with a Novel Coefficient Ordering

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Abstract

This paper presents a new memory-addressing scheme for the realization of low power FFT processors. The scheme is based on the minimization of the coefficient access and reduction of switching activity by modifying the butterfly sequence. Therefore, the power consumption in complex multiplier and memory is significantly saved.

I. Introduction

High performance fast Fourier Transform (FFT) processors are widely used in different areas of application such as communications, radars, imaging, etc. Previously, the major concern for researchers was the enhancement of the processing speed; however, with the advent of portable computations, area and power consumption have become of particular interest. For the FFT processor, a variety of algorithms exist depending on the method used to store the intermediate results and carry out computation. These algorithms determine the architecture of FFT processors: their memory requirements, the complexity of their control unit, the structure of each processor and their interconnections. Therefore, in order to obtain a design that occupies a small area, the selected algorithm should mainly seek to minimize the memory size, the number of communication lines, and the control unit area.

In-place algorithms minimize memory requirements by writing the intermediate results over the data used for their calculation. The architecture of the memory-based FFT processor using an in-place algorithm basically consists of a unique butterfly unit that performs all the operations of the FFT, a two port RAM to store the intermediate data, a memory with twiddle factors, address generators and control logic. For large transforms, the area required for this architecture is considerably smaller than for the others. In this architecture, if the butterfly unit has parallel inputs and outputs, the memory for intermediate results needs to be divided into separate banks in order to access inputs and outputs in one cycle.

Several addressing schemes for an in-place algorithm have been proposed so far. Pease [1] observed that the addresses of the two inputs differ in their parity. It is possible to divide the memory into two separate banks; one bank with even address parity and the other with odd parity. Based on this property, Cohen [2] proposed a simplified control unit for radix-2 FFT processors. Johnson [3] arranged the memory module in his radix-r FFT processor in a similar way. In all schemes mentioned above, the bank partition is completed with parity.

For a low power implementation of FFT processors, a number of researchers have investigated. In [4][6], the authors realized low power architecture by effectively minimizing the number of complex multiplications. In [5], Ma modified butterfly order to reduce the number of coefficient access such that the power consumption in memory is saved. Hasan [7] proposed low power FFT processor based on the algorithm that decreases switching activity of successive coefficient feeding into complex multiplier.

In this paper, we propose a new addressing scheme, which minimizes the number of coefficient access with reduced switching activity. A new addressing scheme can be applied to radix-r in-place FFT algorithms, where r is power of two. We demonstrate that the proposed scheme can be implemented more efficiently with much reduced hardware than the ones mentioned earlier.

II. BANK PARTITION

The N-point discrete Fourier Transform (DFT) is defined by

$$X_k = \sum_{m=0}^{N-1} x_m \cdot W_N^{mk}$$

where WN = exp(-j2π/N) and k=0, 1, ···, N-1.