Image Data Processing System for Satellite

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Abstract: The SRI (Super Resolution Imager) uses the CCD (Charge coupled device) detector that is used to convert the light into electronic data. The purpose of the SRI is to obtain data for high resolution images by converting incoming light into digital stream of pixel data.
The SRI has a high resolution, so this electronic system needs more fast imaging data processing, detector control and data transmission systems.
This report describes the required system specification and manufactured electronic system for satellite.

Keyword: CCD, Camera, Satellite, Image, High resolution, transmission

1. Introduction

The purpose of the SRI EOS (Electro-Optic System) is to obtain data for high-resolution images by converting incoming light (analog data) into digital data.
The OM (Optical Module) of EOS includes an optical objective, in order to image the objects on its detectors. The objective consists of two optical channels, a Panchromatic channel (PAN) and a Multi-Spectral channel (MS).
Each detector has four output modes. Every output from CCD port has a separate video-processing channel that incorporates CDS (correlated double sample), PGA (programmable gain amplifier) and a 10 bits A/D (analog to digital converter). The outputs of the A/Ds are digitally driven out using differential line drivers, converted to 8 bit bytes, serialized and transmitted to the NUC (Non-Uniformity Correction) module for pre-processing to correct for non-uniformity. The single band pixel rate is about 60Mpps. Each detector's band shall be configured to up to four output ports (each output pixel rate is about 15Mpps).

2. EOS system

The SRI system is a space-borne Electro-Optical system. The OM of SRI includes an optical objective, in order to image the objects on its detectors. The objective consists of two optical channels, a PAN and a MS. The two channels have catoptric common mirrors.
The PAN channel has a high-resolution image and produces a black-white picture at the spectral region of 500nm-900nm. The MS channel consists of four spectral bands and its resolution is four times greater in comparison to the PAN channel. The PAN channel has up to 1m ground resolution and the MS channel has up to 4m ground resolution in each of the 4 spectral bands.
The detector consists of 5200 active elements with 32 TDI stages. The number of TDI stages is externally selectable in predefined stages. This control module shall be included in the FPE (Focal Plane Electronics) of CEU The FPE board receives operating voltages from an external source. The FPE board supplies voltages (required power) as well as clocks (timing) to the CCD detector. Precise timing is supplied to the detector to ensure optimal operation in each operational mode (Fig.1).

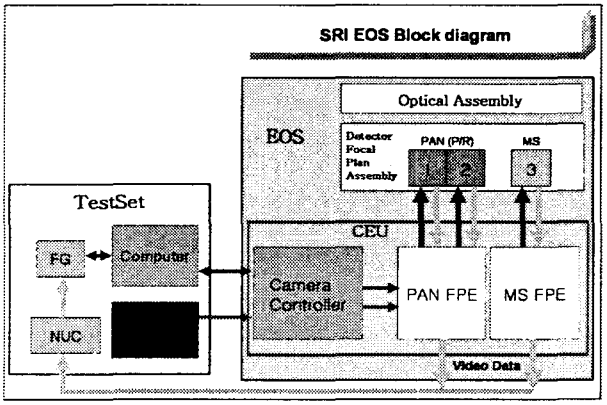

Fig.1. EOS Block diagram.

3. Data Acquisition system

The incoming light is converted to electronic analog signals by the detectors in the DFPA. The analog signals are amplified, biased and converted into digital signals (pixel data stream) in the FPE.

Every output from CCD port has a separate video-processing channel that incorporates CDS, PGA and 10 bits A/D. In this paper, the TDA8787 is used by video processor. The TDA8787 has the sampling frequency up to 30MHz, PGA gain range of 3dB, and low power consumption. The outputs of the A/Ds are digitally multiplexed and driven out using differential line drivers. Each of the detectors is supported separately with the required timing and power supply circuitry

The fig.2 is the CEU block diagram. As the fig.2, the CC (Camera Controller) controls the PAN FPE and MS FPE.

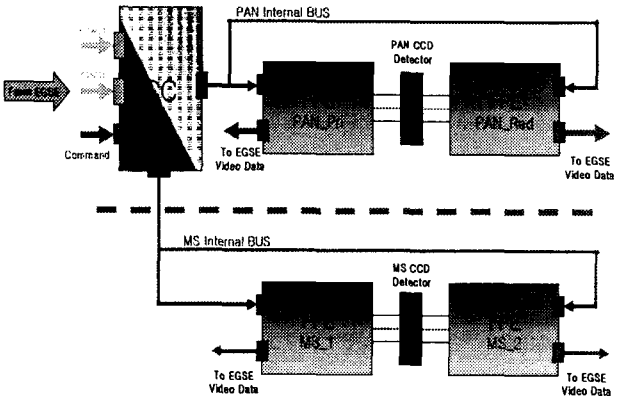

Fig.2. CEU Block diagram.

The digital data is transmitted to the NUC (Non-Uniformity Correction) for pre-processing to correct for non-uniformity, to partially reorder the pixel stream (in the MS channel only) and to add header data for identification and synchronization.

The EOS is slave to the EGSE and fully controlled by the EGSE. The EOS receives the required power supplies from the Power Supply Module of the EGSE.

The FPE assembly shall support the detector with the required power and timing. It shall process the analog signals, which come out of the detector and convert them to digital form. The FPE assembly shall consist of a single detector, up to six video channels, clock drivers, voltage regulators and control lines.

The fig.3 shows the manufactured CEU system.

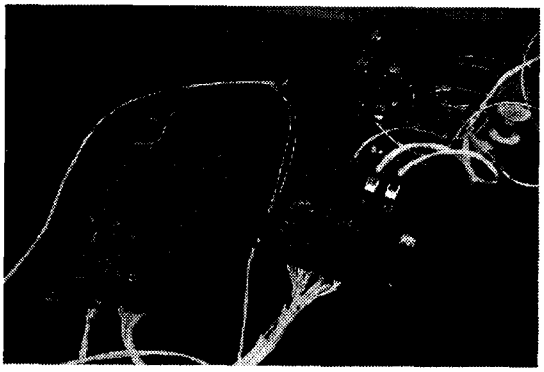

Fig.3. CEU system.

4. Data Processing & Transmission

The fig.4 is the PAN FPE data output block diagram. As the fig.4, the acquisition video signals from the detector (four-output, each mode Primary and Redundant) are amplified, converted, mixed, and transmitted. The fig.5 is the MS FPE data output block diagram. In the MS mode, the video data output mode has only one channel, because of the slower video data rate for MS channel.

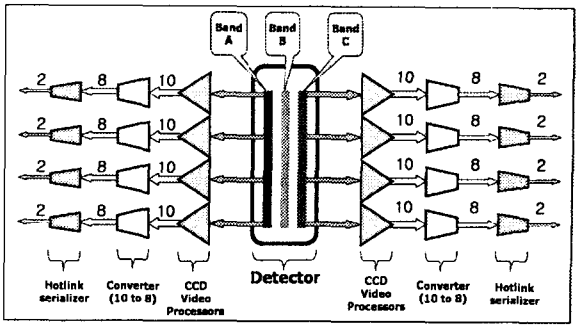

Fig.4. PAN FPE Data Output Block diagram.

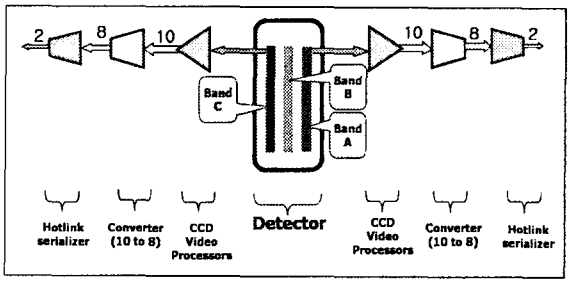

Fig.5. MS FPE Data Output Block diagram.

The fig.6 is the NUC block diagram. As the fig.6, the NUC board is an image-processing unit that receives video data from the FPE boards via a hotlink. Five FPGAs are implemented within the NUC board, each device takes charge of two video channels. The handling video data in the NUC is transmitted to the EGSE for displaying. The main functions of the NUC board's FPGAs are to perform NUC procedures on pixel values using gain and offset words, load the NUC tables value from the SRAM according to control commands.

The fig.7 shows the manufactured NUC system.

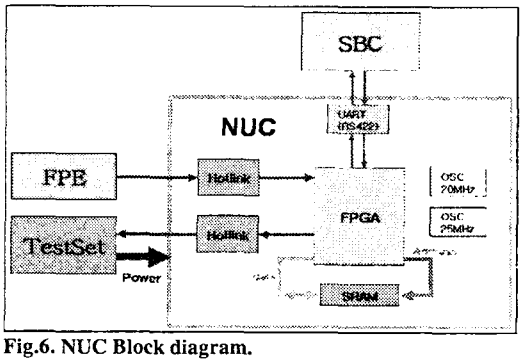

Fig.6. NUC Block diagram.

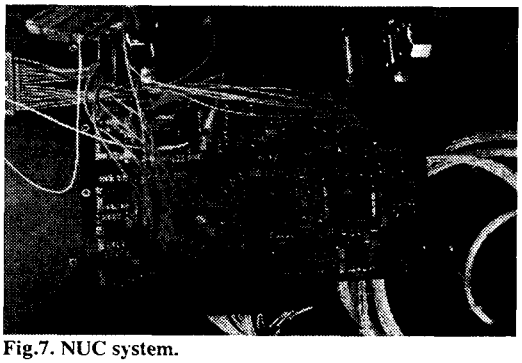

Fig.7. NUC system.

5. Data Display

The EGSE designed to conduct the testing of the SRI EOS and the NUC, shall be used for checking and verifying the functionality and performance of the EOS unit tests and the NUC. Also, it's used for supporting SRI system testing by providing display services for the image data that is collected from the SRI output and providing simulated image data at the input of the NUC under test and acquiring image data at the output of the EOS under test. For operating in the EOS test mode and testing the EOS, the EGSE shall supply the power, command and control, telemetry and thermal control, image data acquisition.

In image data acquisition mode, it acquires image data at the output of the EOS under test while (Fig. 8).

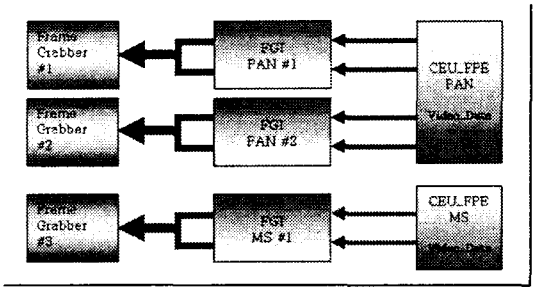

Fig.8. Video Data Stream In EGSE system.

The fig.9 is the FGI system that is controlled by EGSE. It is used for image data acquisition from NUC via hot-link method. The FGI board (for Frame Grabber Interface) is the board that accepts the stream of imagery data from the EOS and prepares it for the Frame Grabbers for capture and storage in the EGSE memory. The objectives of the FGI boards are to perform some electrical conversions, to identify and synchronize of lines of the imagery data using a synchronization patterns in the stream of data from EOS, to generate synchronization signals for the frame grabbers, to inject predefined patterns of data for testing purposes, and to track the movement of the translator axes.

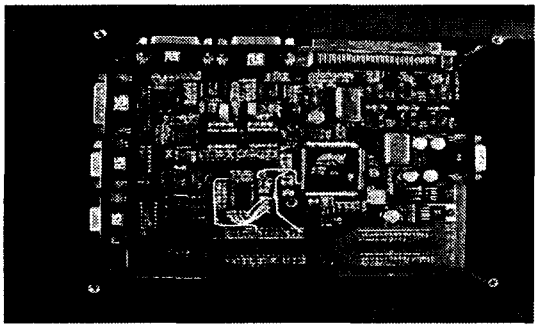

Fig.9. FGI system.

The fig.10 is the simulated data in CEU FPE board. It's used for verification of the video data transmission system. The EGSE receives the simulated data and displays it (fig.11).

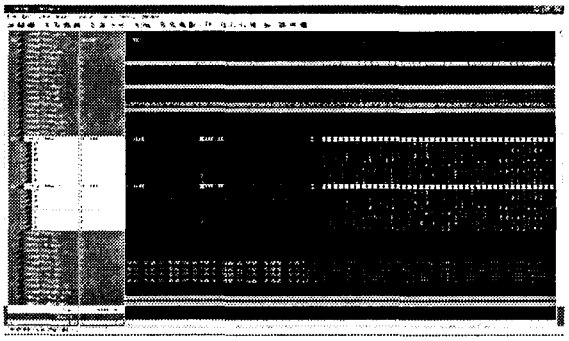

Fig.10. Simulated video data.

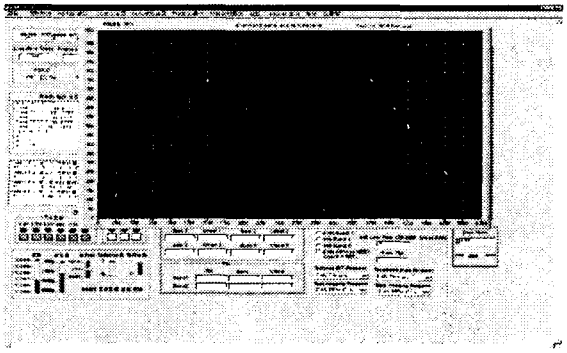

Fig.11. EGSE video data output.

6. Conclusions

The purpose of the SRI EOS is to obtain data for high-resolution images by converting incoming light into digital stream of pixel data. In this paper, the design concept of a video data output system which is described in terms of H/W (video data stream and processing).

Every output from the CCD detector port has a separate video-processing channel that incorporates CDS, PGA and 10 bits A/D. Each detector's band shall be configured to up to four output ports. Each output pixel rate is about 15Mpps.

In the future, it is needed that the multi-purpose satellite camera has fast speed, high confidence, low power consumption, and small size. This image data processing system will be used successfully.

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