Electronic System Design of SRI (Super Resolution Imager) for satellite

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Abstract: The SRI (Super Resolution Imager) is the development project for the next generation satellite camera. This camera has more high resolution than the present satellite camera. It's used by very accurate observation and other multi-purposes. In this paper, the SRI electronic system is described in terms of H/W (Configuration and Function operation).

Keyword: Imager, Camera, Satellite, Electronic System, Observation, Configuration

1. Introduction

The SRI consists of two Electro-optical channels: Panchromatic (PAN) and Multi-Spectral (MS) sharing the same mirror telescope. A single internally CC (Camera Controller), that performs the communication and control functions, serves both the PAN-CEU and the MS-CEU. The incoming light is converted to electronic analog signals by the detectors. The analog signals are amplified, biased and converted into digital signals (pixel data stream) in the FPEs. The digital data is transmitted to the NUC (Non-Uniformity Correction) for pre-processing to correct for non-uniformity and to add header data for identification and synchronization. The SRI fully controlled by the EGSE (Electronic Ground Support Equipment). The EOS (Electro-Optics System) is received the required power supplies from the EGSE. The EGSE performs the management, control and power supply of the SRI operation.

2. SRI system

The SRI consists of the EOS (Electro-Optical Subsystem), the NUC and the EGSE (Testset). The EOS is to obtain data for high-resolution images by converting incoming light into digital stream of pixel data. The NUC performs data processing, to correct and to add the header file. The EOS consists of the PAN camera, the MS camera and the CC. The EGSE comprises of the Computer, Power Supply Module, FG (Flame Grabber), FGI(Flame Grabber Interface), and the Monitor.

The fig.1 shows the MSC block diagram.

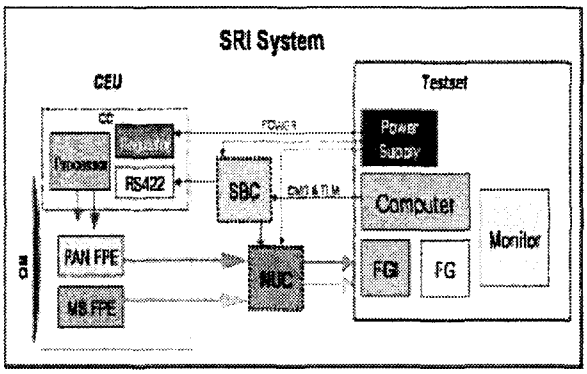

Fig.1. SRI electronic system block diagram.

As depicted in the fig.1, the EGSE computer controls all the SRI CEU units via serial communication channel such as RS-422. The NUC is in charge of non-uniformity correction of image data from FPE. The EGSE storages and displays in monitor, the receiving image data from NUC. The fig.2 shows the manufactured SRI CEU system.

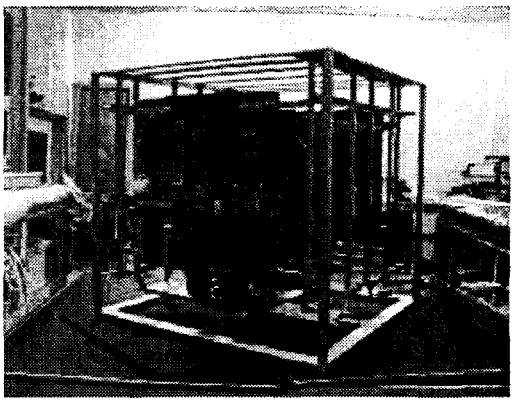

Fig.2. Manufactured SRI electronic system.

3. CEU System

The CEU contains camera control hardware for either the panchromatic or the multi-spectral camera. The CC consists of FPGA, MUX & A/D, 8032 CPU, Memory

devices (Flash, Ram), and Logic device(Fig.3). The main objectives of the CC are to manage the various system operation modes, to handle communication with the master via the serial communications link, to control camera operation, to execute the Built-In Test (BIT), and to collect and report telemetry data to the EGSE.

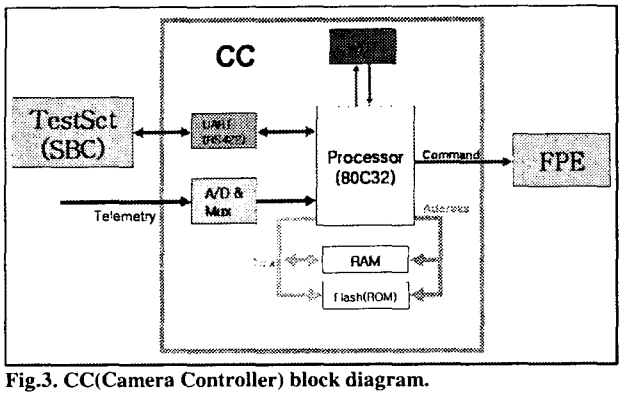

Fig.3. CC(Camera Controller) block diagram.

The CEU-PAN is based on the CCD detector having three linear arrays of pixels (three bands). Each band has 5,200 active photo-elements (pixels), and has selectable TDI levels (1, 4, 8, 16 or 32 rows).
During normal imaging one band is operational and the second one is not as redundant. The output from each band in a detector is implemented through 4 outputs. The operating voltages are supplied by the power supply module of the EGSE to the FPE (Focal Plane Electronics) of the detector to ensure proper operation. Precise timing is supplied to the detector to ensure optimal operation in each operational mode. The analog video data is sampled, amplified, converted to digital form and transmitted out to the NUC module.

The CEU-MS is based on the CCD detector each having three linear arrays (A, B, C) of pixels. In CEU-MS only A and C are operational bands. Each band has 5,200 active photo-elements (pixels), and has selectable TDI levels (1, 4, 8, 16 or 32 rows). The output from each band is through 1 output. The operating voltages and command are supplied by the EGSE.

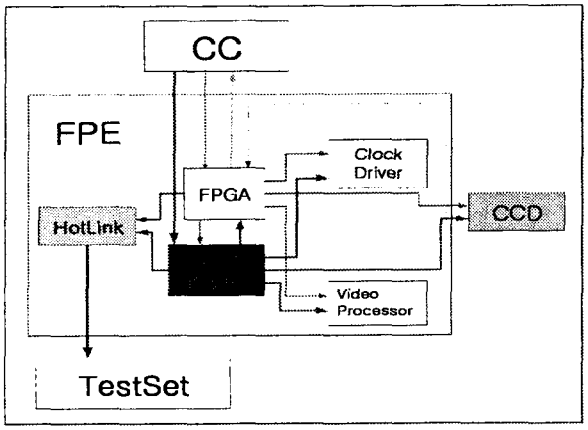

Fig.4. FPE (Focal Plane Electronic) block diagram.

The FPE assembly shall support the detector with the required power and timing (Fig.4). It shall process the analog signals, which come out of the detector and convert them to digital form.

The fig.5 shows simulated data result that is the supplied to FPE from CC for camera electronic controls and operations.

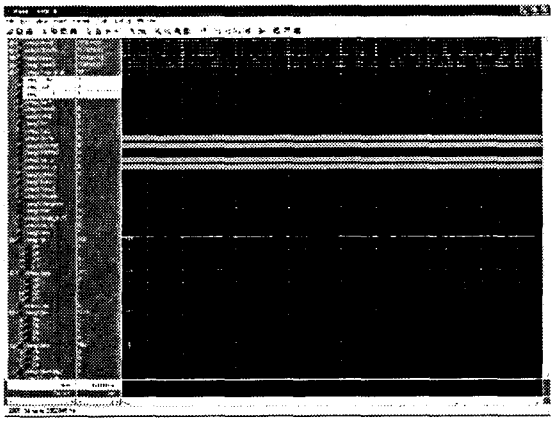

Fig.5. FPE Control Signal from EGSE.

4. SBC & NUC System

The SBC is an on-board computer for the management, control and power supply of the SRI operation.
The SBC shall handle the communication with the EGSE for command and telemetry.
The SBC consists of three FPGAs. One of these is designated for handling commands received from the CPU (Intel-486 processor). This FPGA receives commands from the CPU and handles these commands. The other two FPGAs handle the communication (external/internal) functions of the SBC PCB. The SBC contains six UARTs. Four of these are controlled by the first FPGA and the other two are controlled by the second FPGA.
The SBC FPGA makes use of the following buses: An 8-bit data bus for communicating with external components, A 32-bit data bus, Buses for writing and reading the on-board memory components.
The fig.6 shows the manufactured SBC system.

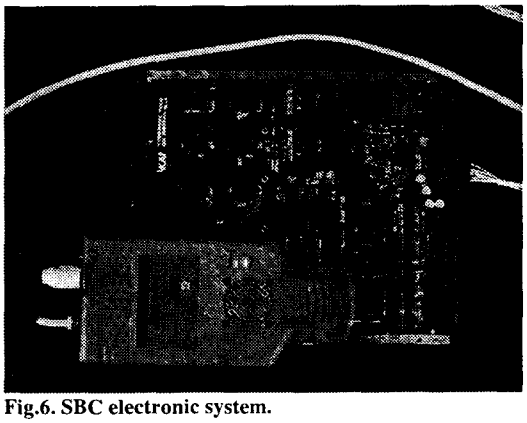

Fig.6. SBC electronic system.

The NUC board is an image-processing unit that receives video data from the FPE boards via a hotlink and performs non-uniformity corrections upon the pixels. The NUC may operate in several different configurations. The video data that is processed by the NUC is transmitted to the EGSE.

The each logical device implemented in the NUC is identified that handles panchromatic video channels and multi-spectral video channels. The main functions of the NUC board's FPGAs are to perform NUC procedures on pixel values using gain and offset words and to load the on-board SRAM with the NUC tables.

5. EGSE System

The EGSE is a computerized testset designed to conduct the testing of the SRI EOS and the NUC. For this purpose, EGSE shall have the capability of connecting with the SRI EOS external interfaces on a one-to one basis.

The following block diagram (Fig.7) displays EGSE's connectivity with the SRI system.

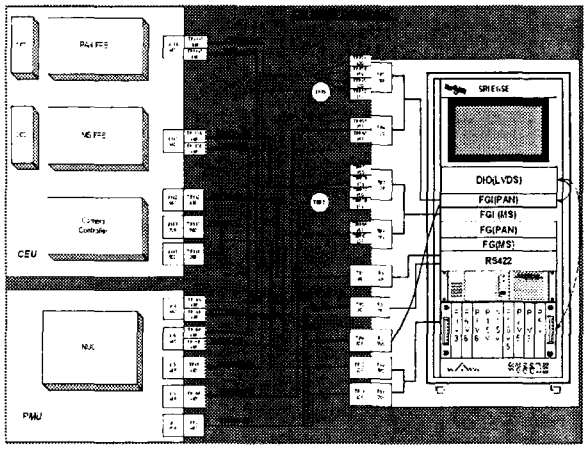

Fig.7. EGSE block diagram.

EOS EGSE shall be used for checking and verifying the functionality and performance of SRI during EOS unit tests, checking and verifying the functionality and performance of NUC, supporting SRI integration by checking the functionality and the performance of SRI system. Therefore, the EGSE shall be capable of operating, controlling and monitoring the EOS under test by providing the input power, establishing communication, implementing thermal control and monitoring the status reports and analog signals, providing simulated image data at the input of the NUC under test and acquiring image data at the output of the EOS under test or the output of the NUC under test. EOS EGSE shall use all the above capabilities for testing the EOS functionality and performance

The fig.8 shows the manufactured EGSE system. As depicted in the fig.8, EGSE system is very important to control and to test the SRI EOS system.

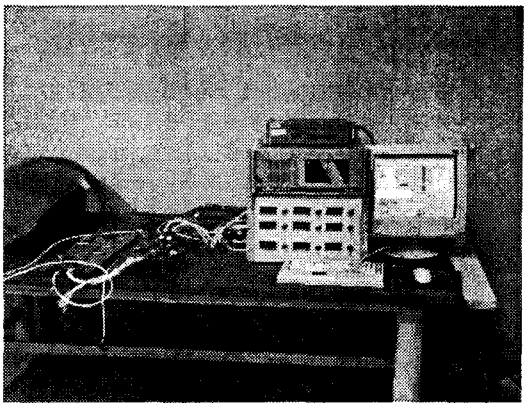

Fig.8. FPE Control Signal from EGSE.

6. Conclusions

In this paper, the SRI electronic system is described in terms of H/W (Configuration and Function operation). The SRI consists of panchromatic and multi-spectral channel. The CC performs the communication and control functions, serves both the PAN and the MS channel. The detector converts incoming light to electronic analog signals. These data are amplified, biased, converted into digital signals, and transmitted to NUC in the FPEs. The NUC performs pre-processing to correct for non-uniformity and adding header data for identification and synchronization. The EGSE fully controls the total SRI system by supplying the power and the control commands.

This camera has more high resolution than other satellite camera. It's used by very accurate observation and other multi-purposes. The development of the SRI system will be based on advanced design methods and tools, and will make use of novel advanced components and technology, in order to reduce size, power consumption and weight and enhance performance

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