FOS improvement through the growth speed increase of A-Si layer in TFT process

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Abstract

As time goes by, the market demand increases and each LCD panel manufacturing company makes every effort to produce more panels in a limited time. It is necessary to reduce the cost and time of production for the improvement of productivity in manufacturing companies.

The increased speed of thin films growth used in the TFT process brings improvement of productivity but it is also accompanied by a drop in display quality due to a characteristic change of the thin film. So in our dissertation, we deal with the increased speed of a-Si layer growth and the proportioned a drop in characteristic quality.

We discuss a drop in display quality by a characteristic change of a-Si layer and we propose a counter-plan through panel design improvement. We have already applied our plan to the 15" XGA panel and confirmed the improved result.

1. Objectives and Background

Amorphous silicon (a-Si), TFT layer of semiconductor, has different structure from the forbidden gap of crystalline silicon (c-Si) because it does not have the regularity of long range. There are energy band tails and deep state in the center of the forbidden gap due to a disorderly combination of a-Si. Fig 1 shows the energy band structure of a-Si:H [1,2].

The energy band tails that came out from the edge of the bands make the localized state and the mobility in the a-Si:H very weak in comparison with c-Si due to the defective state made by the localized state and the dangling bond.

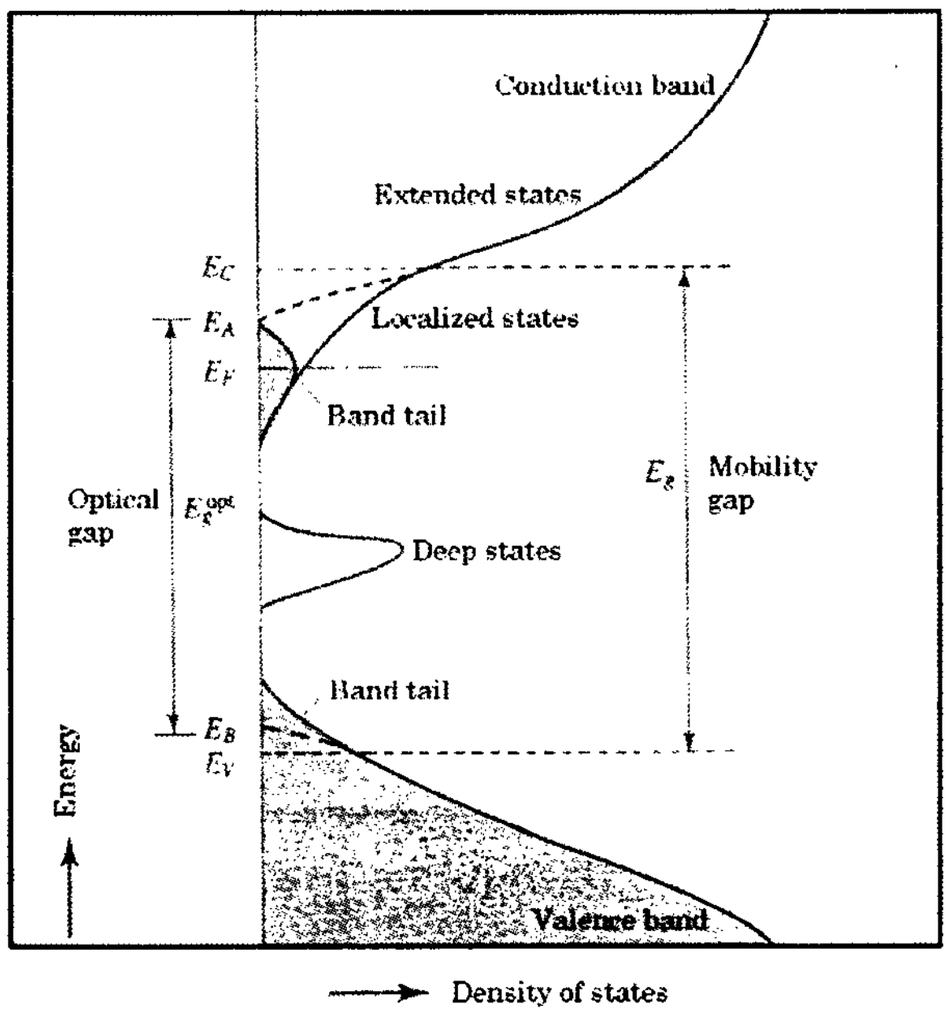

Figure 1: Schematic representation of the density of states and the electron distribution of n-type a-Si:H. The mobility gap of a-Si:H is 1.9eV and the optically defined band gap is about 1.7eV.[2]

The characteristic of a-Si:H layer depends on the condition of deposition (the flux rate of H_2 and SiH_4), the electrode spacing of CVD and RF Power etc. The objective of LCD panel manufacturing companies is to study how to increase the production capacity of TFT with good quality in a limited time. Regretfully, the more the RF power of CVD is raised to shorten the time of making the layer of a-Si:H , the more the layer characteristic of a-Si:H decreases.

In case of TFT of BCE (Back Channel Etch) structure, the steps making the layer of a-Si divides into roughly two steps. The first step is to make a-Si:H layer with RF low power and the characteristic of a-Si:H layer controls the one of TFT element. The second step is to make a-Si:H layer with RF high power.

Although the characteristic of a-Si:H layer decreases a little bit due to rapid deposition, the characteristic finally controls the one of TFT element and the second step plays a role to protect the layer made by the first step from BCE.

Generally, the thickness of the second layer is 2.5~3.5times thicker than one of the first step. So the process time of the second step is longer in comparison with 1st step. The more RF power is raised, the more the layer is made rapidly when the layer of the second step is made. As for controlling RF power, we can increase the capacity of TFT. The important prerequisite is that the entire TFT characteristic does not change.

2. Results

When forming the semiconductor layer of thickness 2000Å a-Si:H on 590×670 ㎜ mother glass, the total time required is 271sec (The first step takes 74sec and the second step takes 197sec). At this time, CVD RF power is 200W in the first step and is 550W in the second step. For reducing the time required in the second step, we can increase RF power up to 900 W without changing the TFT characteristic, and the required time in the second step is 180sec. Fig 2 shows the TFT Transference Characteristic Curve from 550W and 900W of RF power each other. We know that there is not a big difference between them.(refer to of table 1.) However, low temperature irregular mura occurred from LCD module with TFT elements made by 900W. This occurs because the Ion current decreases as a result of the drop in kinetic energy of many carriers in a-Si:H in a low temperature[3,4,5].

The fig. 4 is the actual measurement result of TFT characteristic in the high temperature and in the low temperature and we know that On-current is about 50~60%w in the low temperature.

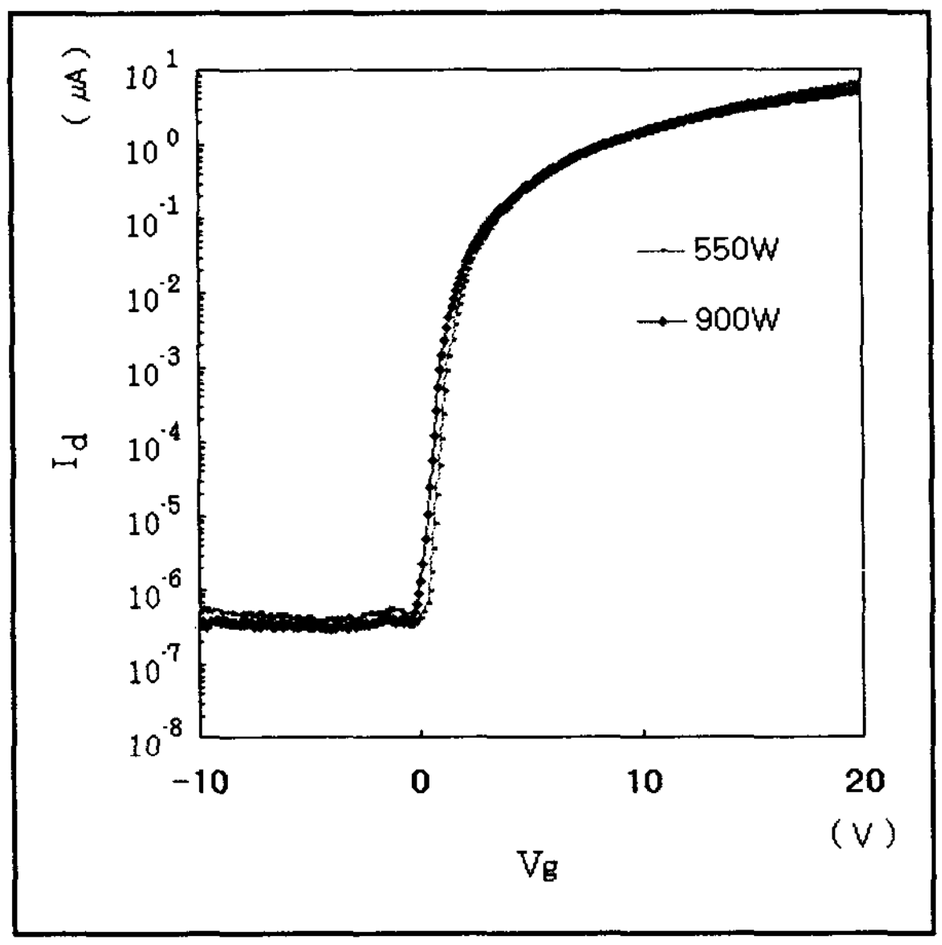

Figure 2: TFT transference characteristic curve (RF power 550W vs 900W)

Table 1

2nd Step condition	I off (pA)	I on (μA)	Vth (V)	Mobility (㎠/Volt-sec)
550W	0.39	1.43	1.19	0.29
900W	0.32	1.42	0.88	0.24

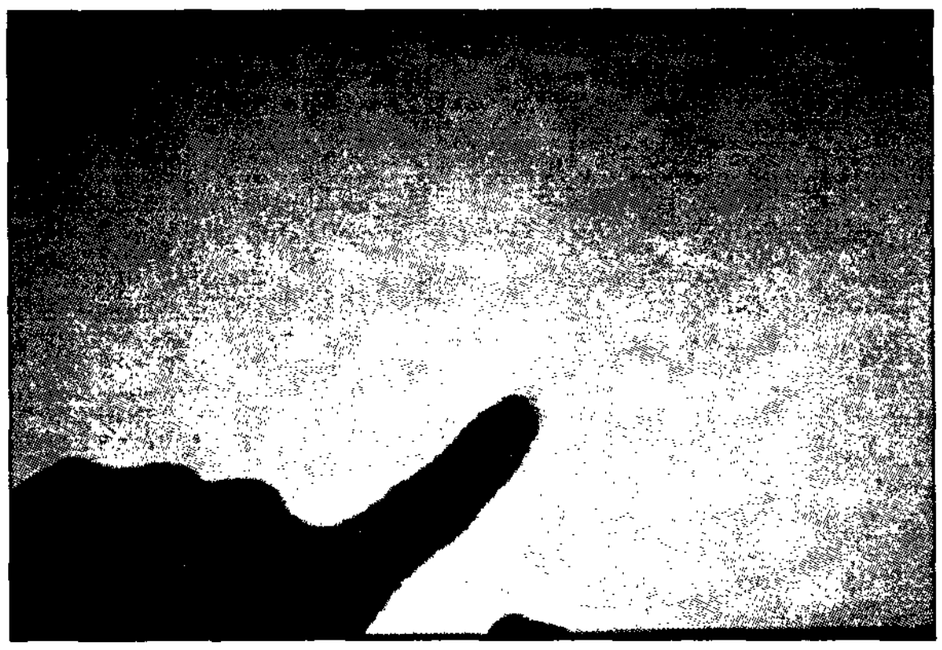

Figure 3: The irregular mura that can occur in the low temperature test in a LCD module.

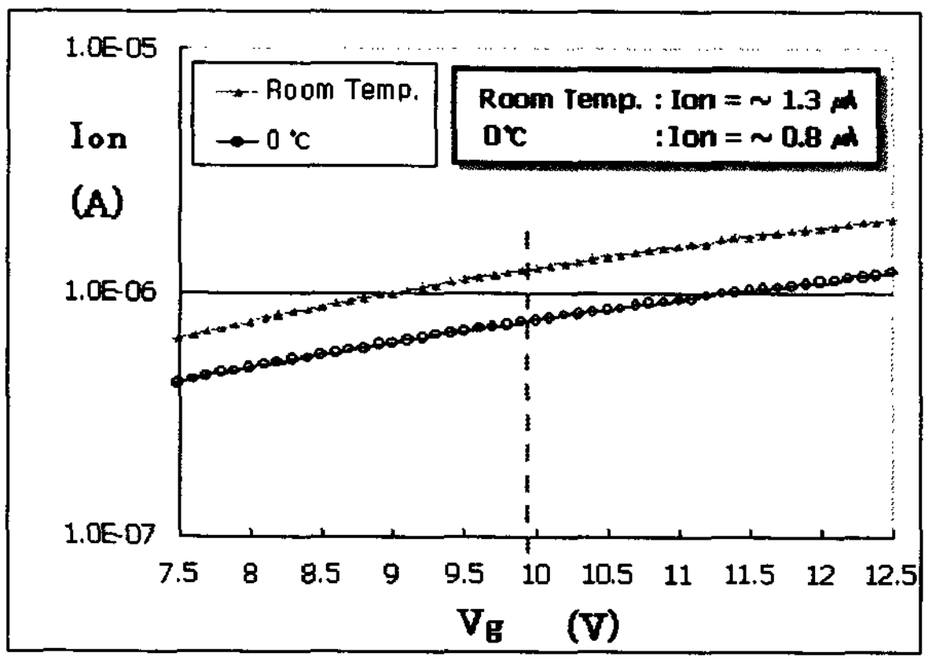

Figure 4: The current at 0℃ shows a decrease of 40%~50% compared with that of room temperature.

The most effective method for improving low temperature irregular mura is to increase current gain K [1,6].

The current gain is defined as

$$K = 1/2 \times W/L \times \mu \times Cg$$

W ; the width of TFT channel
L ; the length of TFT channel
μ ; the mobility of transistor carrier
C_g ; the parasitic capacitance in Gate insulator between a-Si:H layer and Gate layer when the current flows.

In case of increasing the W/L parameter (unique design factor), C_{gs} increases together. Therefore, the Pixel charging can be retarded or current clouding can occur.

In case of increasing W/L from 7 to 9 in 15.0" XGA panel, C_{gs} increased from 651 pF to 774 pF. So we decreased C_{st} (pixel storage capacitance) from 230fF to 200fF to complement it. The Fig 5 shows the relation between the increase of C_{st} and the charging of pixel.

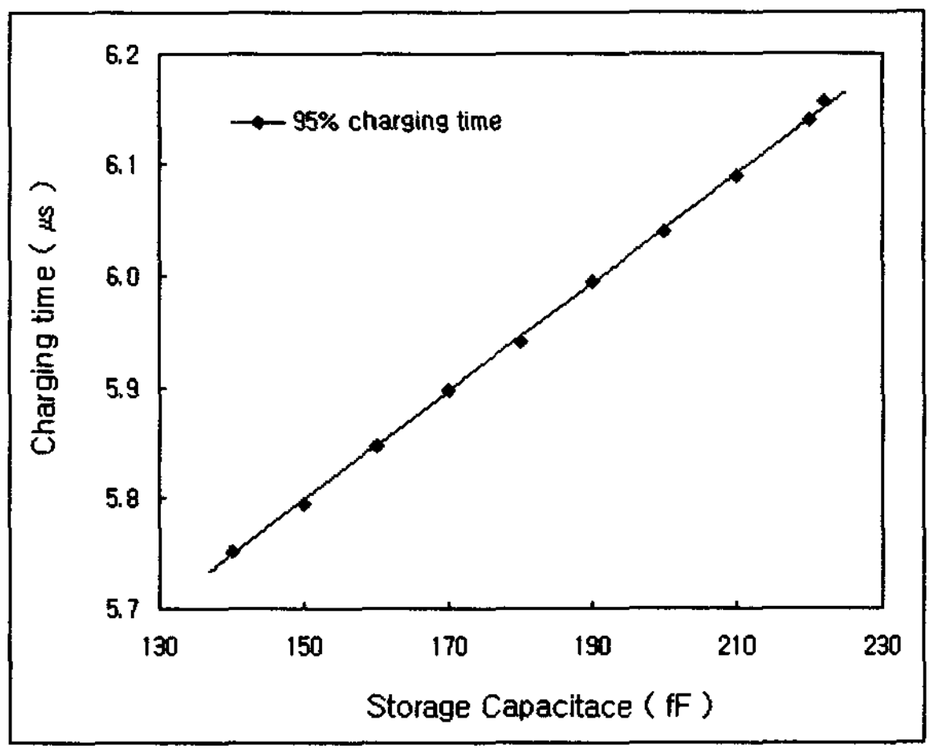

Figure 5: The relationship between C_{st} and pixel charging

In short, we increased RF power from 550W to 900W in the second step to reduce the growth time of a-Si:H layer, increased W/L of TFT from 7 to 9, and decreased C_{st} from 230fF to 200fF. As a result of the tuning of the process condition according to the variation of parameters, the low temperature irregular mura disappeared and the charging ability of TFT improved a little bit. Table 1 shows the characteristic of TFT between completed sample through design tuning and the uncompleted one when RF power is increased 900W.

Table 2

Condition	I off (pA)	I on (㎂)	Vth (V)	Mobility (㎠/Volt-sec)
rf = 900W, W/L = 7, & Cst = 230fF	0.32	1.42	0.88	0.24
rf = 900W, W/L = 9, & Cst = 200fF	0.23	1.73	1.03	0.25

3.Impact

We increased RF Power to reduce the growth time of a-Si layer. So we saved 17sec for layer growth and the production capacity of

15.0" XGA TFT increased 6000ea/month with 590×670 ㎜ mother glass.
When process tuning is needed for improving production capacity, the counter-plan has to precede for completing it.

4 References

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