Development of New LTPS Process

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Abstract

We have developed the five mask PMOS[1] and the six mask CMOS process architecture for poly-Si TFT. In order to have a competitive process with that for a-Si TFT, the simple co-planar electrode structure whose data line electrode and pixel electrode are on the same plane was adopted. In addition, RGB + White four color technology[2] were applied to achieve high aperture ratio and transmittance. Using the aforementioned process architecture and four color technology, 2.0 inch qCIF transmissive micro-reflectance (TMR) device was successfully fabricated.

1. Introduction

Low-temperature poly-silicon thin-film-transistor liquid-crystal-display (LTPS TFT-LCD) has gained much attentions in the area of mobile applications, since compact and high resolution TFT-LCD panel can be fabricated and, thus, less number of driving IC are required by integrating the driver circuitry on the peripheral area of the panel. However, in general, the fabrication cost is relatively higher than that of a-Si TFT-LCD due to the increased number of process steps and masks. In order to achieve the cost competitiveness, the fabrication process of LTPS TFT-LCD needs to be simplified, comparable to a-Si TFT-LCD.

In addition to the PMOS five mask (or CMOS six mask) process architecture, the four color technology using RGB + White is introduced in order to both improve optical properties of panel and make the integration of peripheral circuitry easy.

In this paper, we report the five mask PMOS and six mask CMOS process architecture adopting the pixel-data electrode co-planar structure and the RGB + White four color technology was successfully developed and applied to the 2.0 inch qCIF TMR device.

2. Results

2.1 TFT Process

Table 1 shows the PMOS five mask and CMOS six mask process architecture used in 2.0 inch qCIF. In case of five mask PMOS device, comparing with normal seven mask CMOS architecture, Gate-N process and via (or passivation) process are not necessary by introducing PMOS process architecture and co-planar structure, respectively. The cross-section view of TFT fabricated using the less mask process architecture is shown in Fig. 1. To realize five mask PMOS and six mask CMOS process architecture, the etching selectivity of data metal against pixel electrode is required since the data metal should not be damaged while patterning the pixel electrode.

Process \ Gate driving type	CMOS (7 mask)	CMOS (6 mask)	PMOS (5 mask)
Active	0	0	0
Gate P	0 (P+)	0 (P+)	0 (P+/P-)
Gate N	0 (N+/N-)	0 (N+/N-)	
ILD	0	0	0
S/D electrode	0	0	0
Passivation	0	0	0
Pixel electrode	0		

Table 1. Comparison of each LTPS-TFT fabrication process flow.

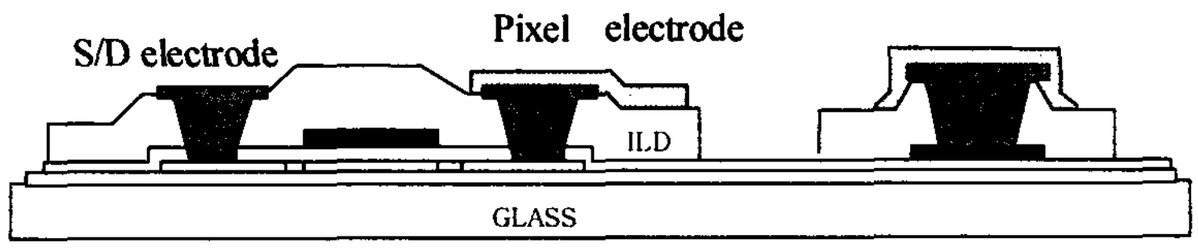

Fig. 1. Schematics of cross sectional view of coplanar S/D and pixel electrodes structure.

2.2 Crystallization

SLS is a new crystallization technique using laser.[4] The procedure consists of repeatedly irradiating the film to induce complete melting of the exposed areas of the film. Crystal grows from the side of the masked regions into the molten region as the film cools. Then the sample is translated over a distance less than the exposed area so that part of the crystallized region overlaps and acts as seed for next crystallization, and is irradiated again. Once more, this results in complete melting of the exposed areas.

Lateral growth recommences from the edge of the completely molten region. In this study, SLS poly-silicon is crystallized with a two shot process. The two-shot implementation method is especially well suited for formation of poly-silicon films as it can have a high throughput with relatively high quality silicon. The grain propagation direction is arranged parallel to the TFT channel direction on the gate driver circuits. The structure of the active layer is monitored by scanning electron microscope (SEM) as shown in Figure 2.

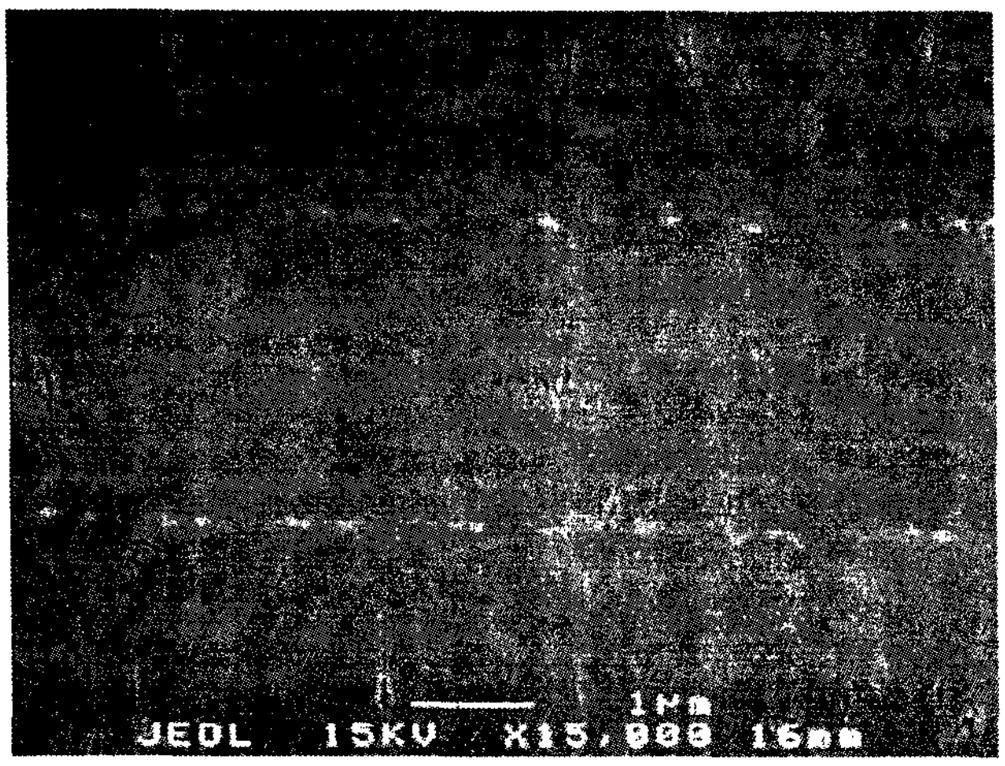

Fig 2. SEM micrograph of SLS polysilicon.

2.3 Four Color Technology

In addition to the less mask process architecture, RGB + White four color technology is introduced. An RGBW system is an addition of white color to the conventional RGB system. The addition of the white sub-pixel greatly enhances the light efficiency. The RGB to RGBW mapping algorithm is designed to keep the original color intact and improve the luminance at the same time with no aid of extra backlights. The sub-pixels of RGBW and normal RGB systems are depicted in Figure 3. There is no loss in the aperture since it has two lines running within a pixel just as the RGB system. Consequently, the channel number of gate driver is doubled, but the channel number of source driver is reduced by 1/3. An RGB system, there are 3 sub-pixels, each occupying 1/3 of a pixel and transmitting 1/3 of light. As a result, only 3 x 1/3 x 1/3 = 33% of light is transmitted. In an RGBW system, there are 3 colored sub-pixels, each occupying 1/4 of a pixel, and one white sub-pixel transmitting all of light. The result is transmission ratio of 3 x 1/4 x 1/3 + 1 x 1/4 x 1 = 50%. This results in an increase of the luminance by 50% in an RGBW system.

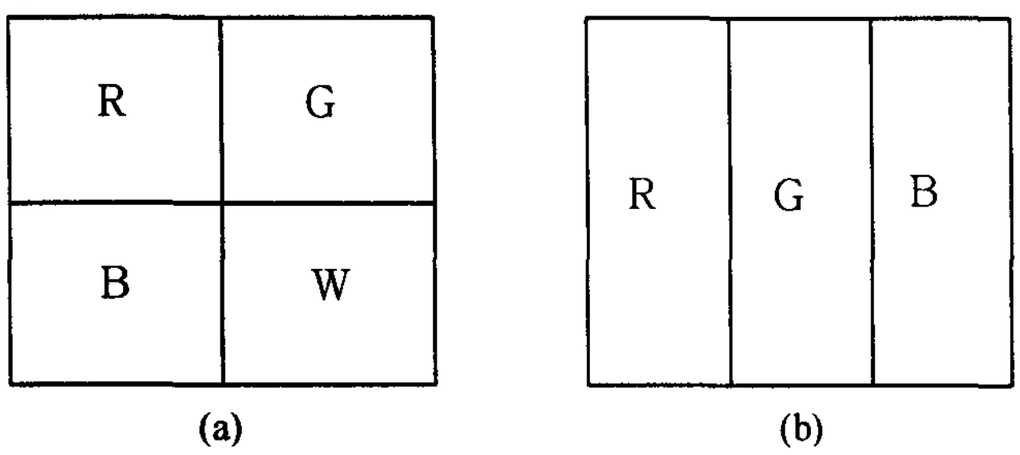

Fig. 3. Sub-Pixels of RGBW(a) and RGB(b) system

RGB + White four color technology not only improves the luminance of panel by increasing aperture ratio and transmittance, but also makes the integration of peripheral circuitry easy which can be the great merit for LTPS TFT-LCD.

Fig. 4 shows the simplified pixel structure of less mask poly-Si TFT. In case of properly integrated devices, we can use 5 mask PMOS architecture[3,4], however, for the highly integrated devices, we have to use 6 mask CMOS process.

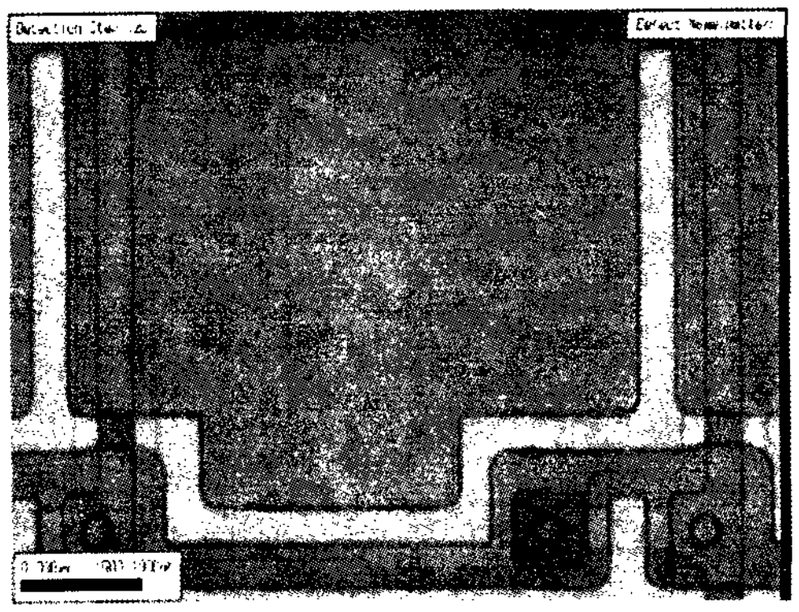

Fig. 4. Top view of simplified pixel structure of 2.0" qCIF less mask poly-Si TFT

3. TFT Characteristics of PMOS LDD Structure

In order to reduce the leakage current, we optimized the LDD condition using the single gate structure.[3] This effect is shown in Figure 5. Using the PMOS architecture, we could reduce the off current level stably and it shows the similar on current value to that of CMOS process.

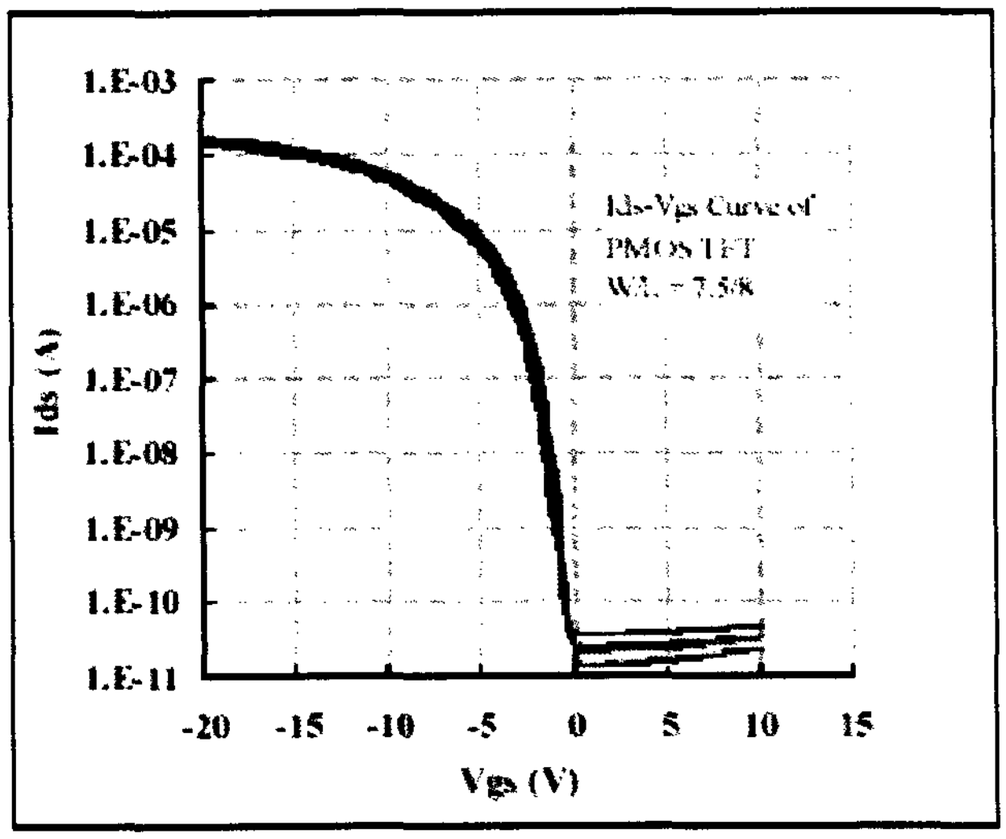

Figure 5. Transfer characteristics of 7.5/8 (W/L) TFT.

3. Conclusion

We have developed the five mask PMOS and six mask CMOS process architecture of LTPS TFT, which takes the advantage of less process steps, resulting in saving the fabrication cost. This process architecture would be expected to improve the competitiveness of LTPS TFT.

4. Acknowledgements

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5. References

[1] P.M Choi, etal, Korea Patent Applied (in process)

[2] S.D. Lee and C.Y.Kim, Korea Patent Applied (in process)

Fig. 7. Variation of TFT transfer characteristics after 20000sec hot carrier stress.

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