P.116:A New DC-DC Converter for Gate Driver Circuit Using Low Temperature Poly-Si TFT

Jin-Young Choi, Byoung-Chul Cho, Hyun-Sook Shim and Oh-Kyong Kwon
Division of Electrical and Computer Engineering Hanyang University
17 Haengdang-dong, Seongdong-gu, Seoul, Korea
Phone : +82-2-2297-0139, E-mail : okwon7@chol.com

Abstract

In this paper, we present a new DC-DC converter for gate driver circuit in low temperature poly-Si TFT technology. It is composed of a newly developed charge pump circuit and a regulator circuit. When the input voltage is 5V, the efficiency of a positive charge pump used in the DC-DC converter and that of a negative charge pump is 69.0% and 57.1%, respectively. The output voltage of DC-DC converter varies 200mV when the target voltages of DC-DC converter are 9V, -6V and the threshold voltage of TFTs varies ± 0.5V.

1. Introduction

Recently the market for portable devices such as PDA or hand-held phone has grown. These devices require display systems with compact size, high quality image, low power consumption and low cost. Low Temperature Polycrystalline Silicon(LTPS) technology attracts attention for its potential to integrate the driver circuits and the power management circuits with pixel array on a glass panel. But power management circuits which are integrated in LTPS panel suffer from low efficiency and difficulty in integrating analog circuit such as regulation; LPTS TFT has some inferior electrical characteristics to single crystal Si transistor, which have characteristic of low mobility, high threshold voltage and non-uniformity of the electrical properties.

To address this issue, we developed a novel DC-DC converter composed of new charge pump and regulator. It has higher efficiency by adding just two more circuit components and can be integrated in a glass substrate by using improved comparator because it has immunity to threshold voltage variation.

2. Limit of conventional charge pump circuit

Dickson's charge pump circuit, shown in Fig. 1, is one of the conventional positive charge pump circuit[1]. It converts a low voltage to a high voltage.

The output voltage of Dickson's charge pump which has N stages is represented in Equation (1).

$$V_{OUT} = (N+1)\cdot VDD - (N+1)\cdot V_{th} \qquad (1)$$

And the voltage gained at jth stage, V(j), is given by

$$V(j) = \frac{C \times VDD}{C + Cp} - V_{th} \qquad (2)$$

where C and Cp are clock coupling capacitance and parasitic capacitance at the input node of each unit stage, respectively. VDD is the clock amplitude equal to the power supply voltage, and V_{th} represents the threshold voltage of the nTFT transistor. Equation (2) implies that the voltage gain per unit stage suffers from the threshold voltage drop. To obtain high output voltage in poly-Si TFT technology which has a larger threshold voltage, many stages are needed. Many schemes are proposed to compensate for the threshold voltage drop[2, 3]. But those configurations needed additional control pulses or complex circuits.

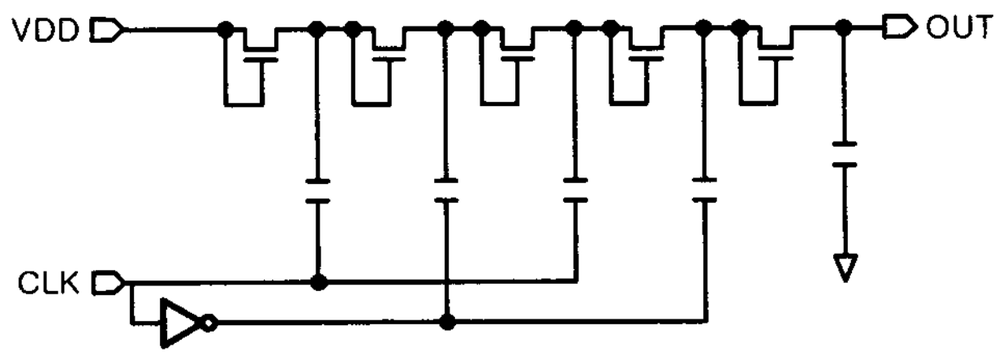

Fig. 1. The conventional 4-stage charge pump circuit.

3. DC-DC converter

Fig. 2 shows a block diagram of DC-DC converter. DC-DC converter is comprised of a charge pump and a regulator. The charge pump circuit makes output voltage which is higher than the input voltage. The regulator compares the output voltage with the reference voltage. If the output voltage exceeds the reference voltage, the regulator turns off the switch. Thus, the charge pump circuit is turned off. Otherwise the regulator turns on the charge pump circuit.

I. Proposed charge pump circuit

Proposed positive charge pump circuit is shown in Fig. 3. Proposed circuit improves its efficiency by adding two more circuit components. As shown in Fig. 3, one pTFT and one capacitor are added. These two additional components prevent threshold voltage drop in the 1st stage. The followings are the operation principle of proposed circuit.

CLK is initially high and CLKB is initially low. In this case, the gate of P1 is applied to low, and P1 is turned on. Therefore Node 0 is charged to VDD. When CLK is changed to low, the gate of P1 is applied to high, and P1 is turned off. Since Node 0 is a floating node, the gate of N1 is charge to 2VDD by clock coupling capacitor, C1. And N1 is fully turned on. The first stage, therefore, transmits the input voltage to the next stage without threshold voltage drop.

The output voltage of proposed positive charge pump with N stages is represented in Equation (3).

$$V_{OUT} = (N+1)\cdot VDD - N\cdot V_{th} \quad (3)$$

Proposed negative charge pump circuit is shown in Fig. 4 and its operation is the same as the proposed positive charge pump. The output voltage of proposed charge pump which has N stages is represented in Equation (4).

$$V_{OUT} = N\cdot V_{th} - N\cdot VDD \quad (4)$$

II. Regulator

The regulator is shown in Fig. 5. It maintains the output voltage constant by comparing the output voltage to the reference voltage. The regulator uses a comparator to compare the two voltages. Due to the large threshold voltage variation in poly-Si TFT, however, conventional comparator which uses differential input stage cannot be used. Proposed DC-DC converter which is integrated in poly-Si TFT panel uses a comparator with single-ended input stage as shown in Fig. 6. And Fig. 7 is its timing diagram.

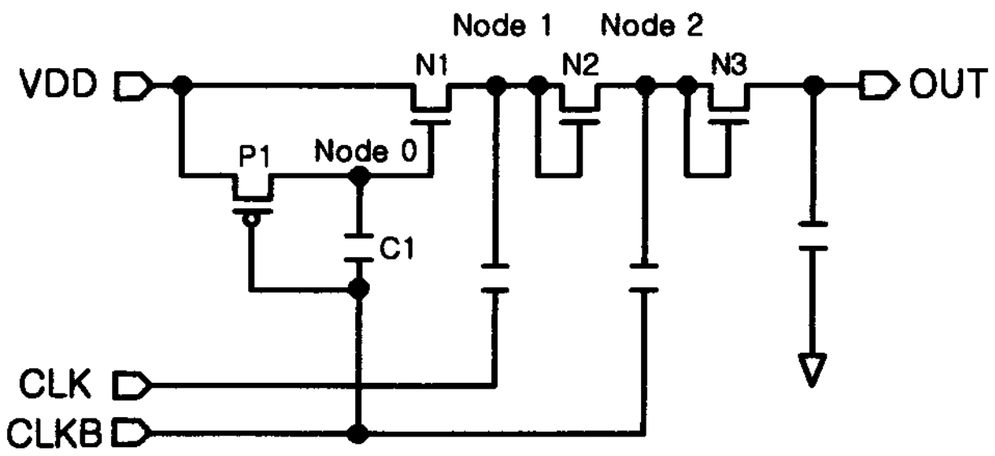

Fig. 3. The proposed 2-stage positive charge pump circuit.

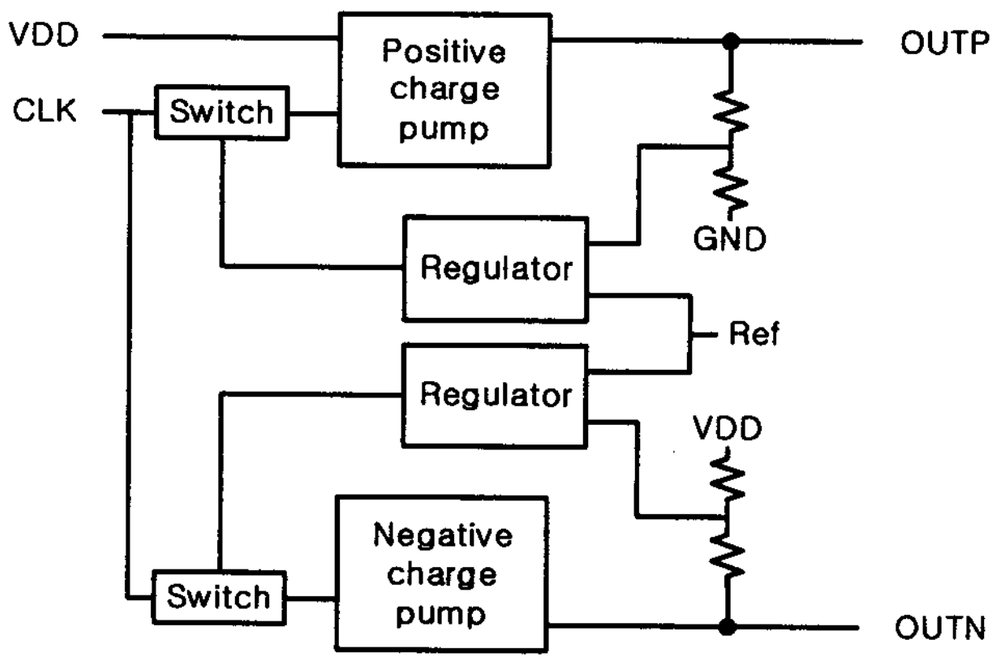

Fig. 2. Block diagram of DC-DC converter.

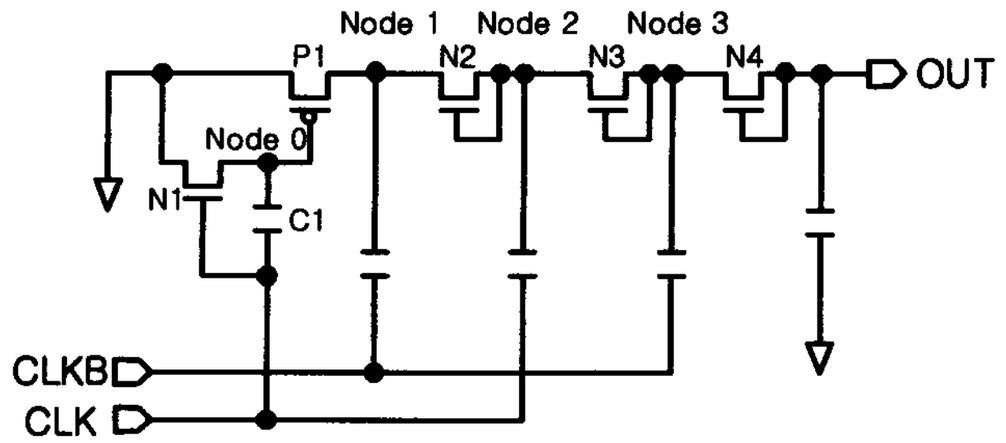

Fig. 4. The proposed 3-stage negative charge pump circuit.

In T1 period, the comparator saves the value of in1 to cap1, and two inverters are in logic threshold state. In T2 period, the value of in2 is applied to C1. If the value of in2 is lower than that of in1, the voltage of Node1 is lower than the logic threshold voltage. Then two inverters amplify the difference between in1 and in2. Output has VV or GND according to the difference between in1 and in2. This structure has immunity to threshold voltage variation.

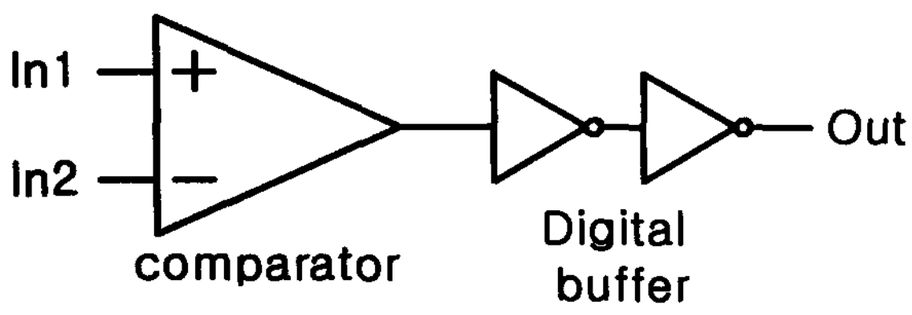

Fig. 5. Block diagram of regulator.

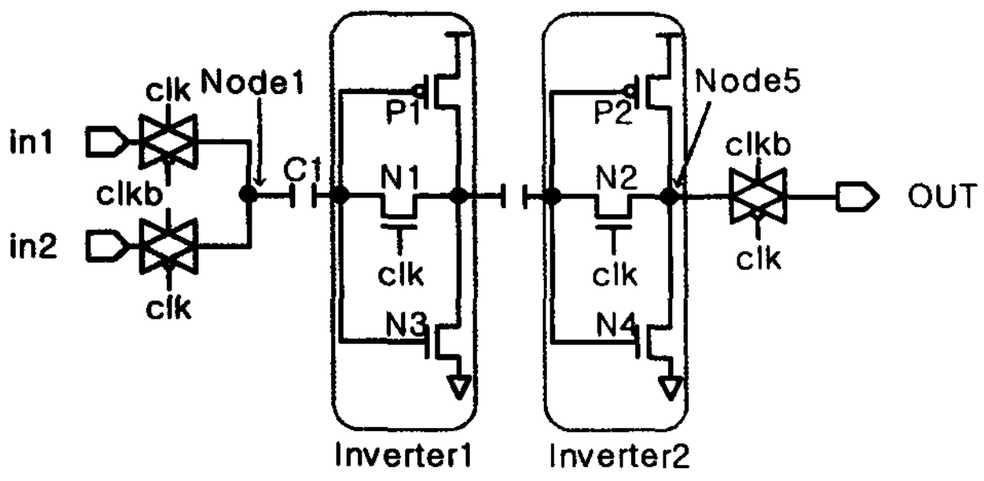

Fig. 6. Single-ended input type comparator.

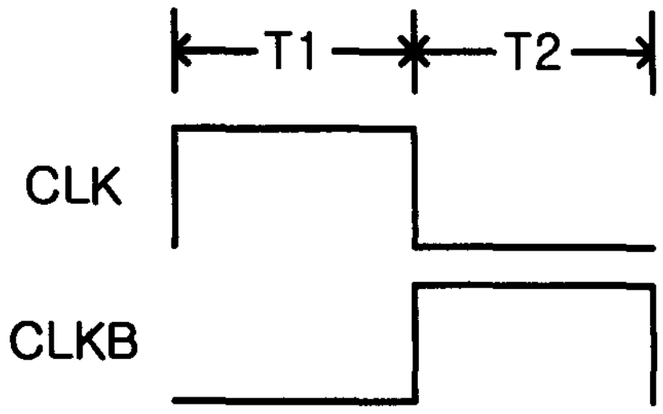

Fig. 7. Timing diagram of comparator

4. Simulation results

We simulated the performance of the proposed circuit by HSPICE. We assume that the input voltage is 5V, and that a display system is 2-inch QVGA poly-Si TFT LCD panel in which driver circuits and power circuits are integrated and that the supplied power voltages of gate driver are 9V and -6V. To know output voltage variation of the output voltage according to the number of stage, we simulated the conventional circuit and the proposed positive charge pump circuit with varying the number of stage. Fig. 8 shows the results of simulation. To obtain 9V the proposed charge pump circuit uses 2-stage but the conventional charge pump circuit uses 3-stage. Thus, the proposed charge pump occupies smaller area and it has higher efficiency than the conventional charge pump circuit.

Since the supplied power voltages of a gate driver are 9V and -6V, the output voltage of positive charge pump circuit must be higher than 9V and the output voltage of negative charge pump circuits must be lower than -6V. When the output voltage of positive charge pump circuit is higher than 9V, the conventional charge pump has 3-stage and its efficiency is 59.1%. But proposed charge pump uses 2-stage and its efficiency is 69.0%. And when the output voltage of negative charge pump circuit is lower than -6V, the conventional charge pump has 4-stage and its efficiency is 46.7%. But proposed charge pump uses 3-stage and its efficiency is 57.1%.

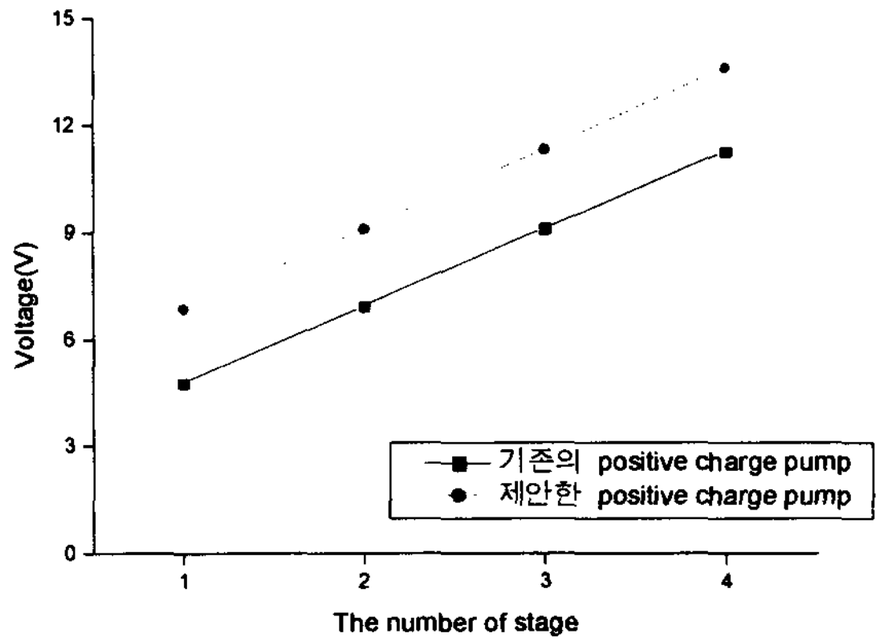

Fig. 8. Simulation results (Output voltage)

The simulated output waveform of DC-DC converter is shown in Fig. 9. In this simulation when time is 100μsec, the load current, 120μA, is turned on. The average output voltages of DC-DC converter are 8.99V and -5.96V. Positive output voltage has 80mV ripple voltage and negative output voltage has 100mV ripple voltage. And the output of DC-DC converter varies 200mV when the threshold voltage of TFTs varies ±0.5V.

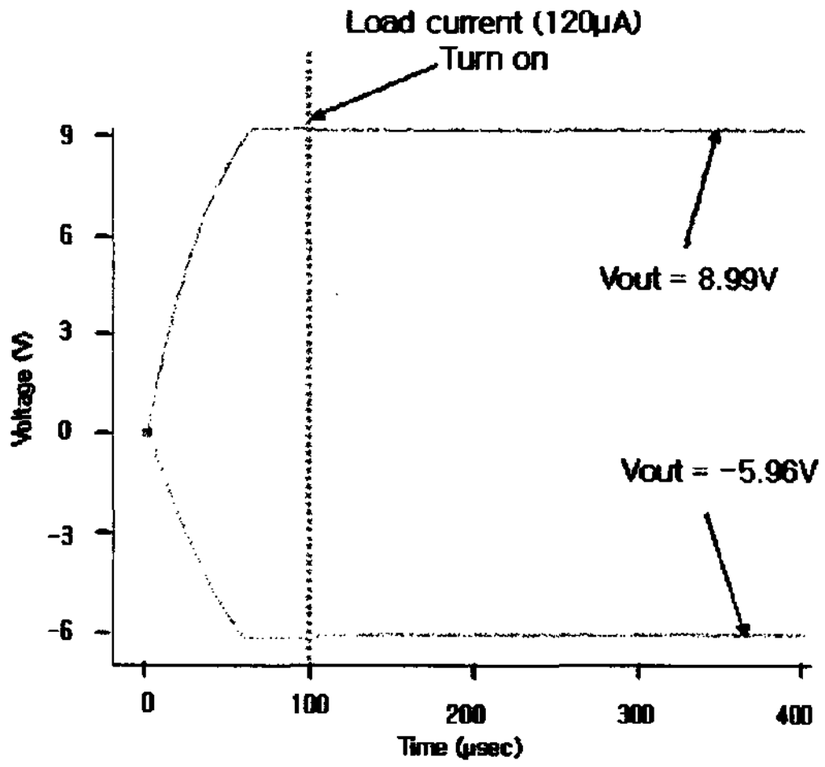

Fig. 9. The result of simulation

5. Conclusions

A DC-DC converter used in gate driver which is integrated in 2-inch LTPS TFT-LCD panel has been developed. The average output voltages of DC-DC converter are 8.99V and -5.96V when the load current is 120μA. The efficiency of positive charge pump used in this DC-DC converter is 69.0%, and the efficiency of negative charge pump circuit is 57.1%. When the threshold voltage varies in ± 0.5V, the output of DC-DC converter varies 200mV.

6. References

[1] John F. Dickson, *el al.*, IEEE J. Solid-State Circuit, June 1976, pp.374-378 (1976)

[2] Jieh-Tsorng Wu, *el al.* , IEEE J. Solid-State Circuit, April 1998, pp.592-597 (1998)

[3] M. Hirata, *el al.* , The 2000 IEEE Asia Pacific Conference on ASICs, pp.17-19 (2000)