

28.5: High Performance Bottom Contact Organic TFTs on Plastic for Flexible AMLCD

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Abstract

We developed a high performance bottom contact, organic thin-film transistor (OTFT) array on plastic using a self-organized process. The effect of OTS treatment on the PVP gate insulator for the performance of OTFT on plastic has been studied. The OTFT without OTS exhibited a field-effect mobility of $0.1 \text{ cm}^2/\text{Vs}$ on/off current ratio of $> 10^7$. On the other hand, OTFT with OTS, exhibited a field-effect mobility of $1.3 \text{ cm}^2/\text{Vs}$ and on/off current ratio of $> 10^8$.

1. Introduction

Organic semiconductor has been studied intensively because they have potential to make large-area devices at low cost on flexible substrate [1]. The TFT performance was improved significantly during the last several years, so that the performance of OTFT is similar to or better than that of amorphous silicon (a-Si) TFT. Among many organic semiconductors, pentacene is the best material for TFT in terms of mobility [2, 3].

We used an organic vapor phase deposition, OVPD, to grow the pentacene thin-film on plastic and optimized the growth conditions to grow a big grain pentacene. We achieved the condition of self-organized pentacene growth [4]. We developed the self-organized process using hydrophobic surface formed by surface treatment and achieved an active-matrix array on flexible polyethersulphone (PES) substrate [5]. In this work we studied the effect of OTS treatment on the PVP gate insulator for the OTFT using a pentacene grown by organic vapor phase deposition. The field effect mobility increases from $0.1 \text{ cm}^2/\text{Vs}$ to $1.3 \text{ cm}^2/\text{Vs}$ by OTS treatment, this is due to the enlargement of grain size.

For active-matrix displays and integrated circuits using pentacene TFTs, patterning with high-resolution are the most important issue. In addition the mobility is related with the grain size and it is attempted to increase its size. So far the inverted staggered structure using a shadow mask technique is widely used because shadow mask process is possible to make the shape of the pentacene active island and the source and drain as well. This is the top contact structure, and this gives better TFT performance. Note that the contact between the organic semiconductor and the metal is better on the organic semiconductor, top contact structure. [6]. But this is not a practical structure for the manufacturing of high resolution displays.

On the other hand, an inverted coplanar structure has inferior TFT performance, but has advantage of high resolution display with a short channel TFT. Therefore, we studied a bottom contact structure for high resolution display.

2. Experimental

2.1 Deposition of Pentacene Thin-Film

Pentacene thin-films are deposited onto plastic substrate using OVPD. The source material, pentacene, was evaporated at the temperature of about $285 \text{ }^\circ\text{C}$, and the deposition temperature was $\sim 180 \text{ }^\circ\text{C}$. The pressure of the reactor was kept to be around 2 Torr using N_2 [7]. The 450 nm thick cross-linked poly-4-vinylphenol (PVP) was deposited onto the PES by spin coating from solution and cured at $180 \text{ }^\circ\text{C}$ in vacuum oven. Before pentacene deposition, the sample was dipped in diluted octadecyltrichlorosilane (OTS) with toluene to allow a monolayer of OTS to be self-assembled on the surface [4].

2.2 Fabrication of Pentacene OTFT

The p-channel pentacene OTFT with a bottom contact, bottom gate structure was fabricated on plastic. Al and Au deposited by magnetron sputtering were used for the gate and source/drain, respectively. A 450 nm thick cross-linked PVP was deposited onto the patterned gate as a polymer gate insulator. Before pentacene deposition, a monolayer of OTS was self-assembled on the PVP surface. Treating the surface with an OTS monolayer has been shown to noticeably improve the performance of pentacene TFT [8]. Pentacene thin-film was deposited onto the substrate by OVPD.

2.3 Fabrication of OTFT Array

Figure 1 shows the cross-sectional view of the OTFT array on PES substrate. A 4 inch array was designed with a 50 ppi (pixel per inch) resolution.

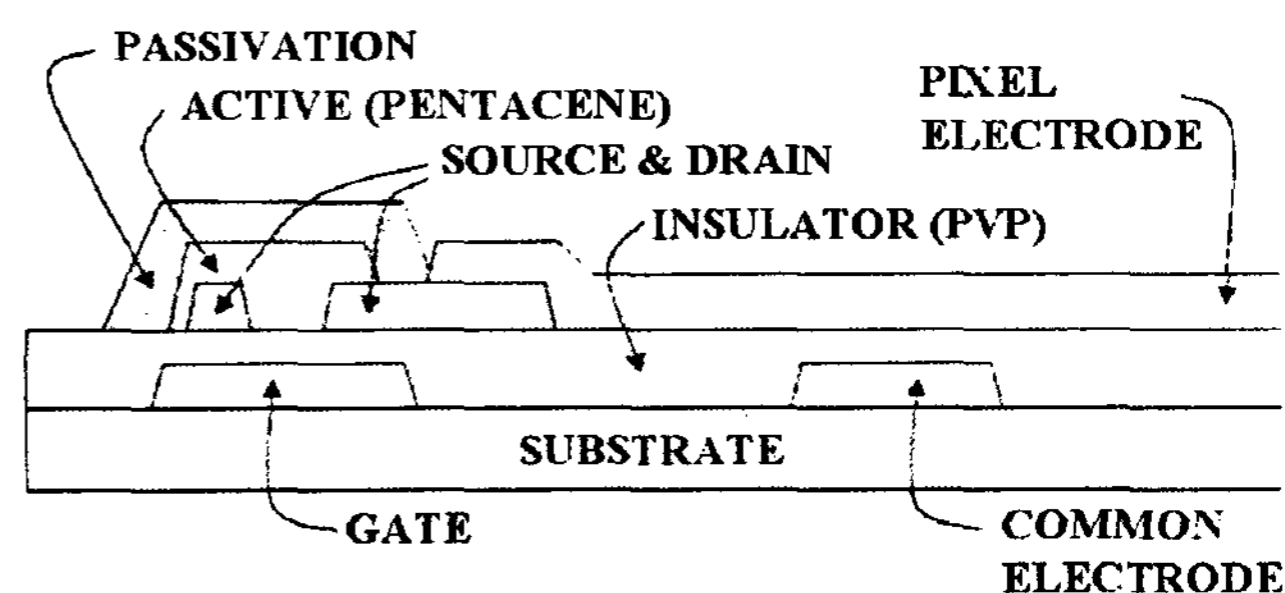


Figure 1. A cross-sectional view of an OTFT array.

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Before pentacene deposition, IZO pixel electrodes were formed and then the surface was treated by O₂ plasma and OTS as well. O₂ plasma was used for making hydrophilic surface and OTS for hydrophobic surface. Therefore, the hydrophobic surface on the TFT area, formed by OTS treatment, helps the selective deposition on the TFT region. On the top of the pentacene, photoacryl was coated by spin coating and formed the island on the TFT using photo-definable process.

3. Results and Discussion

Figure 2 shows the scanning electron microscope (SEM) image of pentacene deposited on the cross-linked PVP with OTS treated on the PES. Thickness of pentacene is about 600 nm and its morphology depends on the substrates; the PVP and OTS treated PVP. Note that the left-hand side, pentacene on the PVP, shows grains of ~ 10 μm. On the other hand, the pentacene on the right-hand side, on the OTS treated PVP, has grains of ~ 20 μm.

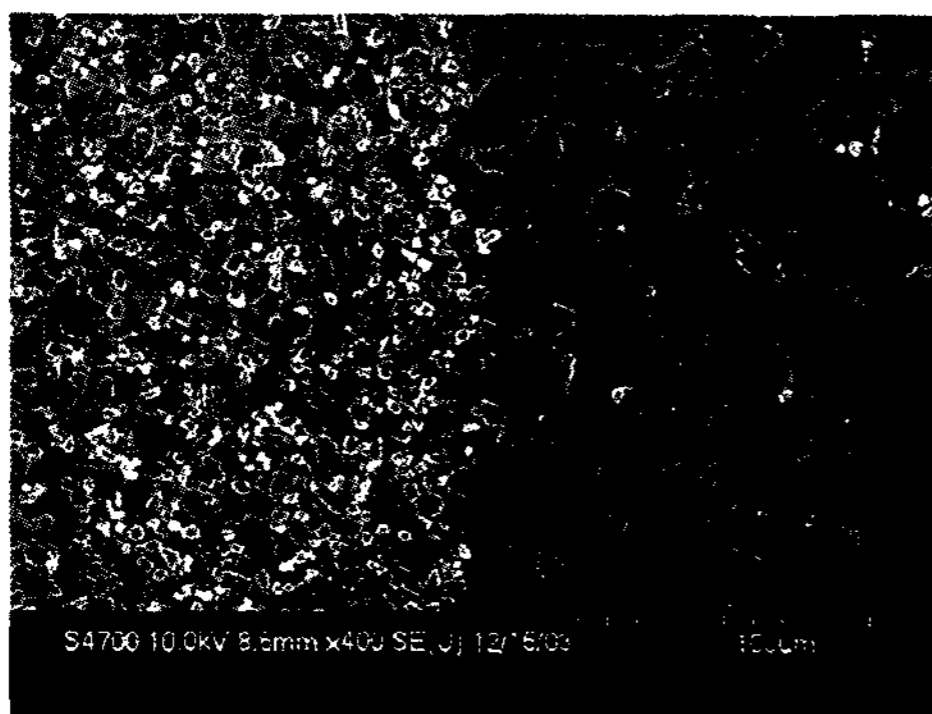


Figure 2. The SEM image of pentacene thin-film on the cross-linked PVP on PES. The images on the as-coated PVP (left-side) and OTS treated PVP (right-side).

Figure 3 shows the X-ray diffraction (XRD) peaks for the pentacene film on the cross-linked PVP with OTS treated on the PES. The films are highly (001) oriented and the full-width-at-half-maximum (FWHM) of the XRD (001) peak is 0.08 which shows good crystalline quality.

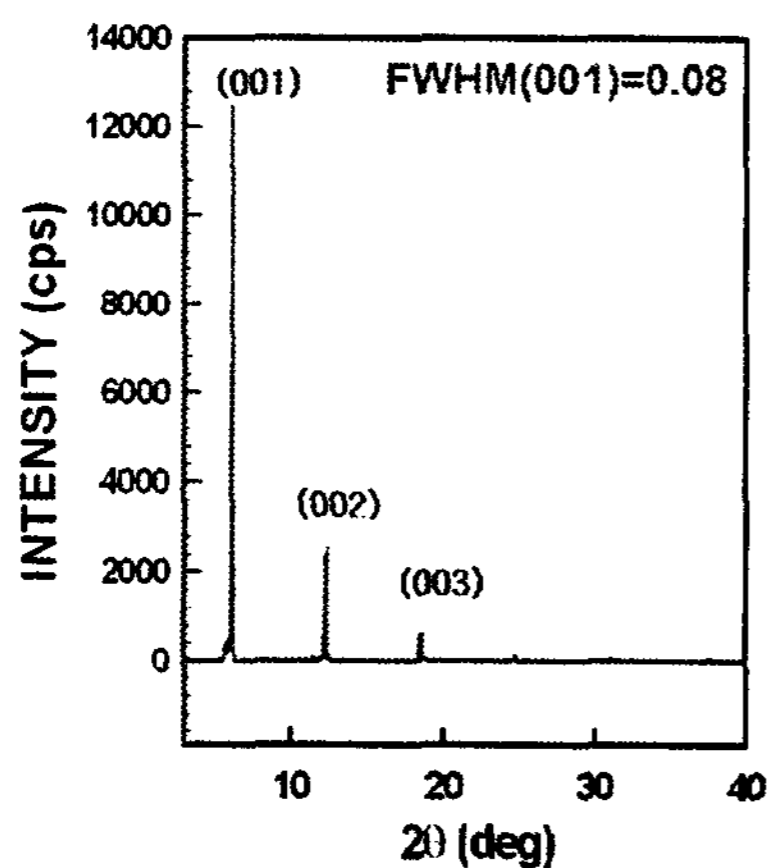
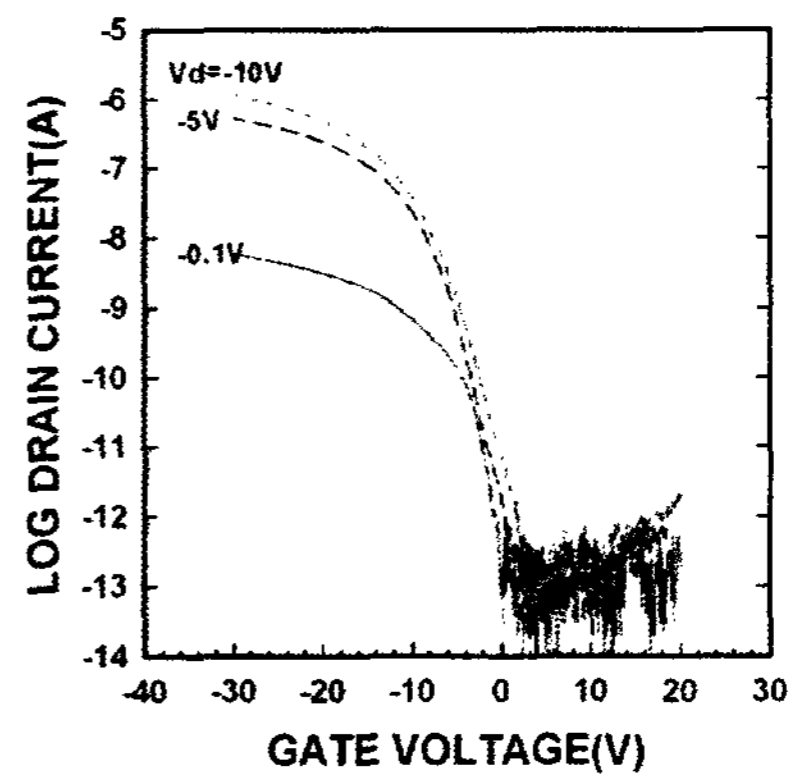
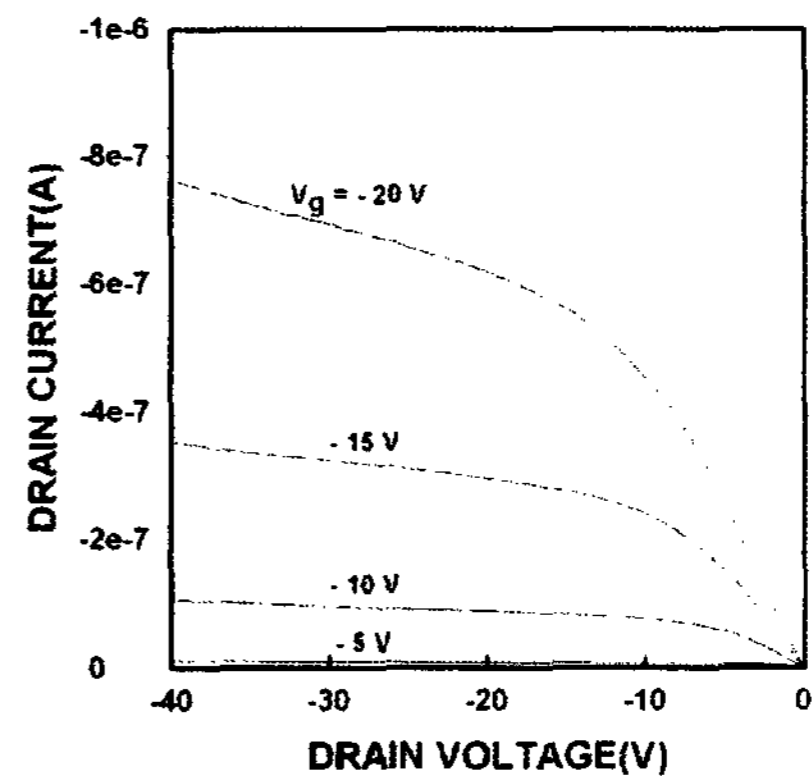


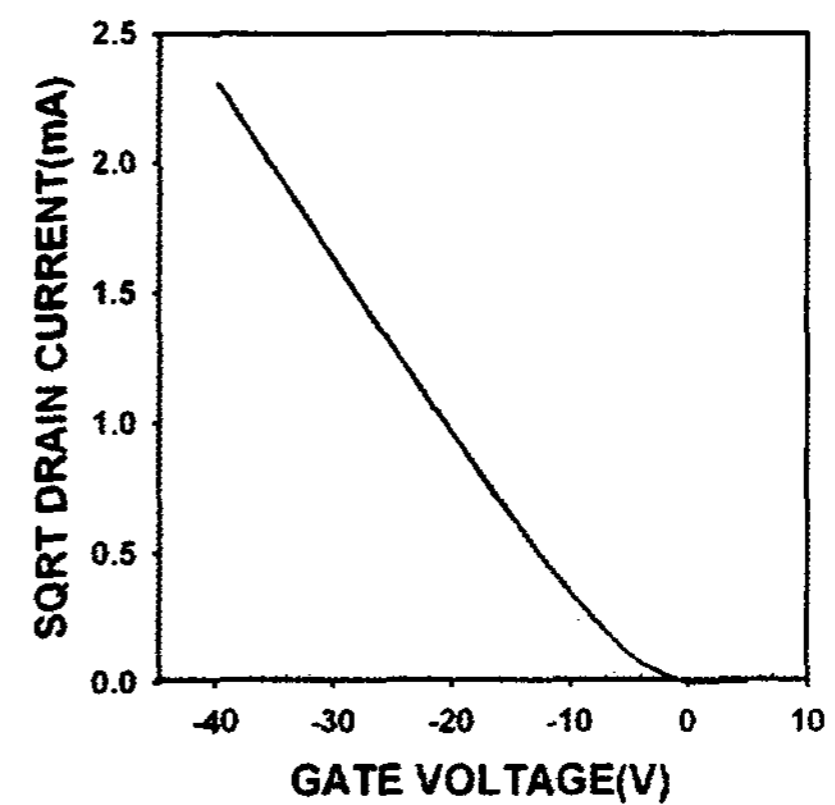
Figure 3. The XRD intensity for the pentacene on the OTS treated PVP/PES.



(a)



(b)



(c)

Figure 4. Transfer (a), output (b) and $I_D^{1/2} - V_G$ characteristics (c) of a pentacene OTFT without OTS treatment. Device parameters for this sample were $\mu_{FE} = 0.1 \text{ cm}^2/\text{Vs}$, $V_{TH} = -6 \text{ V}$ and $I_{ON}/I_{OFF} = 10^7$.

Table 2. Device parameters of the pentacene OTFTs grown with and without OTS treatment on PVP.

Device	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	V_{TH}	μ_{FE}
No treated	1.10 μA	0.10 pA	10^7	-6 V	0.1 cm ² /Vs
OTS treated	24.6 μA	0.23 pA	10^8	-9 V	1.3 cm ² /Vs

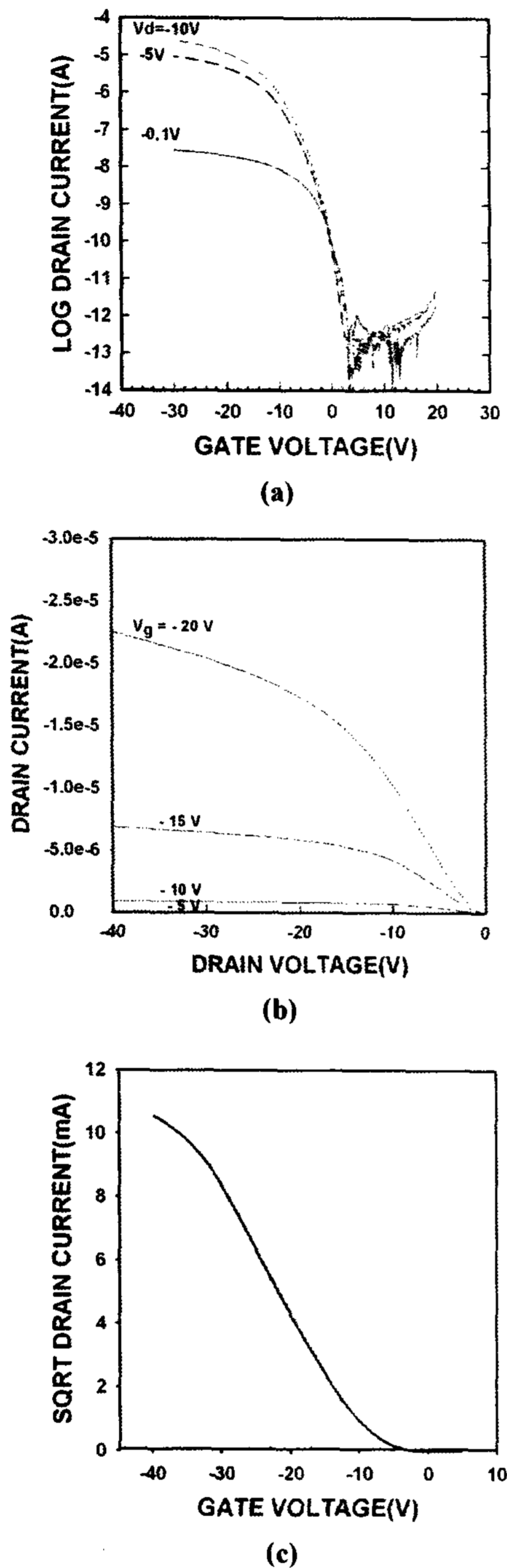


Figure 5. Transfer (a), output (b) and $I_D^{1/2} - V_G$ characteristics (c) of a pentacene OTFT with OTS treatment. Device parameters for this sample were $\mu_{FE} = 1.3 \text{ cm}^2/\text{Vs}$, $V_{TH} = -9 \text{ V}$ and $I_{ON}/I_{OFF} = 10^8$.

Figure 4 shows the performance of an OTFT using the pentacene grown on PVP without OTS treatment. On the other hand, Figure 5 shows the performance of an OTFT using the pentacene grown on the OTS treated PVP surface. The ratio of channel width to length of the TFT was $305 \mu\text{m} / 8 \mu\text{m}$. We evaluated the pentacene OTFT characteristics using semiconductor parameter

analyzer (HP 4156 B). A plot of $I_D^{1/2}$ (I_D ; drain current) versus V_G (gate voltage), where drain and gate were connected together, gives a linear line as shown in Fig. 4 (c) and 5 (c). The off currents shown in Fig. 4 (a) and Fig. 5 (a) are almost the same and less than 1 pA, but on current of Fig. 5 (a) is ~ 22 times higher as compared with Fig. 4 (a). Therefore, on/off current ratio (I_{ON}/I_{OFF}) of OTS treated TFT is at least one order higher than that of non-treated TFT.

The TFT without OTS treatment exhibited μ_{FE} of $0.1 \text{ cm}^2/\text{Vs}$ in saturation region [9], a threshold voltage (V_{TH}) of -6 V and I_{ON}/I_{OFF} of 10^7 , and the TFT with OTS treatment exhibited μ_{FE} of $1.3 \text{ cm}^2/\text{Vs}$, V_{TH} of -9 V , I_{ON}/I_{OFF} of 10^8 . Both TFTs show the off current of less than 1 pA. These are summarized in Table 2.

For the pentacene OTFT array, we carried out the self-organized patterning of pentacene between source and drain of an active area. It is possible to pattern an active layer without direct photolithography process on organic active layer [10].

Table 3 shows the contact angles measured before and after the surface treatment. It is clear that the OTS treatment increases the contact angle, but O_2 plasma treatment decreases it on both PVP and Au surfaces. It was measured by a contact angle & surface tension analyzer produced by Surface-Electro Optics Cooperation using deionized (DI) water.

Table 3. The contact angles of D.I. water on PVP and Au surfaces after various treatments.

Substrate	As-coated	OTS	O_2 plasma	O_2 plasma + OTS
PVP	26.6°	63.4°	8.6°	28.9°
IZO	46.1°	41.4°	8.4°	26.1°
Au	60.0°	83.9°	39.9°	55.0°

The surface changes from hydrophobic to hydrophilic after O_2 plasma treatment and inverse effect is shown after OTS treatment. The Au (83.9°) and the PVP surfaces (63.4°) have more hydrophobic than IZO (26.1°) and the PVP surfaces (28.9°). Therefore, pentacene moves from the PVP and IZO surfaces to the Au and TFT channel. The selective growth of the pentacene can be explained not only by the difference of diffusion coefficient of pentacene at the interface but also on the surface sticking behavior. The selective growth could be seen more clearly when the PVP and IZO surfaces were treated by O_2 plasma. Therefore, the surface was O_2 plasma exposed with the PR on the TFT area before OTS treatment. Note that OTS was treated over the whole surface.

Figure 6 shows the optical image of the pixel array before (a) and after (b) deposition of pentacene and after passivation (c) on PES substrate. Gate and common electrode, organic gate insulator, source / drain electrode and IZO pixel electrode can be seen in Fig. 5(a). Before pentacene deposition, surface was treated by O_2 plasma with photo-resist (PR) barrier on the TFT and then OTS was treated over the whole surface. After treatment, pixel area changes to hydrophilic, and TFT areas change to hydrophobic surface on the TFT array. Therefore, a pentacene was grown on the TFT area so that its color is dark-blue or black as in Fig. 5(b). Therefore, there is clearly self-organized pentacene on the TFT area only, not on the pixel.

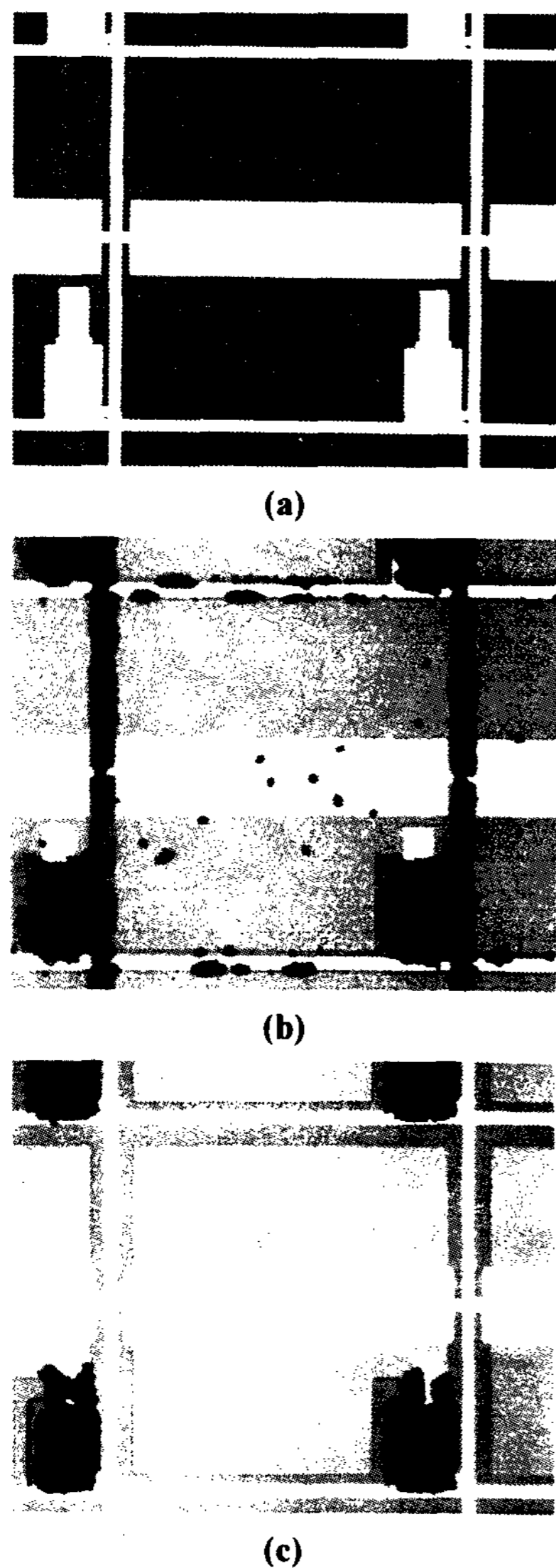


Figure 6. The optical images of the pixel array before (a) and after (b) deposition of pentacene and after forming a photo curable passivation layer (c).

Then, we used the photo-acryl for the passivation of OTFTs. It was coated by spin coating and it is 2 μm thick. Photo-definable process can make the passivation islands on the TFT areas. Fig. 5(c) shows the photo image taken after the formation of the TFT passivation layer. Note that some pentacene dots appeared on the pixel area were removed during this photo-definable process because the pentacene can be easily removed by weak alkaline solutions.

Figure 7 shows the photo image of a pentacene OTFT array backplane on 10 cm \times 10 cm PES substrate. The active area is 4 inch diagonal with a resolution of 160 \times 120 pixels. One pixel has 500 μm \times 500 μm area, corresponding to 50 ppi.

4. Conclusion

We studied the effect of OTS treatment on the PVP gate insulator on the structure of pentacene and TFT performance. We used the



Figure 7. The optical image of a 4 inch pentacene OTFT array on PES.

selective growth of pentacene to make a thin-film transistor island on plastic substrate. The grain size of the pentacene deposited at the substrate temperature of 180 $^{\circ}\text{C}$ was \sim 20 μm under the gas pressure of 2 Torr and the film shows a strongly (001) XRD peak with a small FWHM of 0.08. The on current of the OTFT with the OTS treated surface on plastic substrate exhibited \sim 22 times that of the TFT without OTS treatment. The OTFT with OTS treatment exhibited a field-effect mobility of 1.3 cm^2/Vs and a threshold voltage of -9 V. The on/off current ratio of 10^8 and the off-current of less than 1 pA were achieved.

5. Acknowledgement

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6. References

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