Pentacene Thin Film Transistors Fabricated by High-aspect Ratio Metal Shadow Mask

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Abstract

The robust and large-area applicable metal shadow masks with a high aspect ratio more than 20 are fabricated by a combination of micro-electro-discharge machining (μ-EDM) and electro chemical etching (ECE). After defining S/D contacts using a 100 μm thick stainless steel shadow mask, the top-contact pentacene TFTs with channel length of 5 μm showed routinely the results of mobility of 0.498 $\pm$ 0.05 cm^2/Vsec, current on/off ratio of 1.6 $\times$ 10^5, and threshold voltage of 0 V. The straightly defined atomic force microscopy (AFM) images of channel area demonstrated that shadow effects caused by the S/D electrode deposition were negligible. The fabricated pentacene TFTs have an average channel length of 5 $\pm$ 0.25 μm.

1. Introduction

Among various organic semiconductors, pentacene continues to be an attractive material choice because of its high mobility on the order of 1 cm^2/Vsec for a variety of electronic applications, including information display [1-3], electronic paper [4], and radio frequency identification (RFID) [5].

Even though pentacene thin film transistors (TFTs) can be implemented in one of two configurations, i.e., top contact and bottom contact [6], the best performances of pentacene TFTs in the literature [7,8] have been always demonstrated in the top contact configuration due to the inherently favorable conditions of pentacene growth compared with bottom contact mode [6]. However, the top contact mode is incompatible with the conventional photolithography for the definition of source and drain (S/D) electrodes on organic semiconductor due to their intolerance to the exposure of solven-
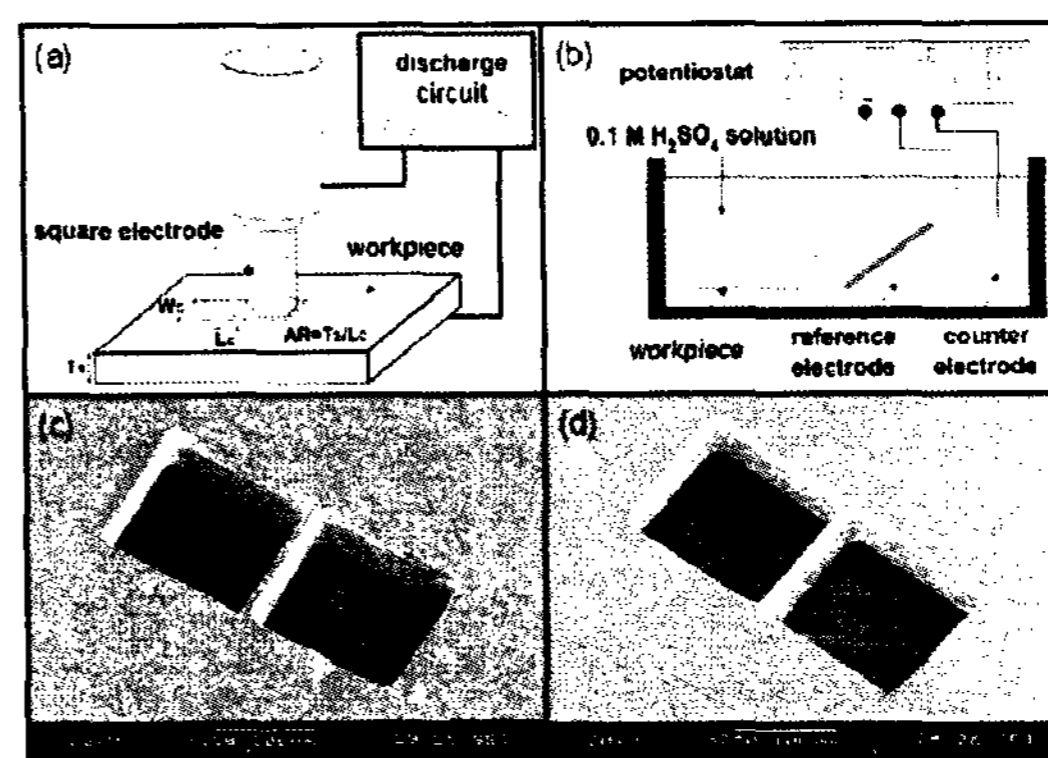

FIG 1. Schematic configurations for (a) micro-electro-discharge machining (μ-EDM) and (b) electro-chemical etching (ECE). The aspect ratio (AR) of an HR shadow mask denotes the ratio of the thickness of workpiece (T$_S$) to the length of a bridge (L$_C$). After μ-EDM processing up to the channel length of 10 μm, the work piece consecutively was electro chemically etched with an etch rate of 4.4 Å/sec in 0.1 mole H$_2$SO$_4$ solution (c) A SEM image for a stainless steel shadow mask right after μ-EDM process. After μ-EDM process, L$_C$ is 10 μm with an aspect ratio of 10 (d) A SEM image for a metal shadow mask right after μ-EDM and ECE process. L$_C$ is 3.6 μm with an aspect ratio of 28. The width of bridge (W$_C$) is 150 μm.

ts and other liquids [9].

Therefore metal shadow masks are generally used to define the top S/D contacts on organic materials because they can guarantee simple S/D definition process without damage of organic materials. But the S/D patterning process by the conventional metal shadow masks (L$_C$ $\approx$ 20 ~70 μm) [6], [9] has two major obstacles, which are high resolution patterning

[10] and mass manufacturability. While commercial products like OELD eliminate gradually the pessimistic prospect for the applications of a metal shadow mask to mass production [11], the high resolution patterning using shadow masks can be a remaining barrier on highly integrated top-contact OTFTs [8]. To achieve top-contact OTFTs with a high areal density, several approaches including cold welding [12], high resolution rubber stamping [13] and special Si membrane masks [14] have been reported in the literature, whereas each method has fundamental drawbacks of too much complicated implementation [12], low-level manufacurability for large area applications [13], and easy brittleness [14].

In this work, we proposed and implemented metal shadow masks with a high aspect ratio (AR >20) based on a combination of anisotropic micro-electro-discharge machining (μ-EDM) [15] and isotropic electro chemical etching (ECE) for the application of OTFTs scaled down less than 5 μm. The high-aspect ratio (HR) metal shadow masks have inherent merits of structural robustness, simple S/D patterning process, and re-usage. In addition, a batch mode μ-EDM technique can be fundamentally applicable to metal shadow masks of a high throughput and good uniformity for a large area application [17].

2. Experiments and Results

Figure 1 presents a schematic illustration of (a) μ-EDM [15] and (b) ECE [16], which were used to fabricate metal shadow masks with high AR larger than 20. As shown in Fig. 1(a), an AR for a metal shadow mask is defined as the thickness of a shadow mask (T_S) to the length of a bridge (L_C). In this experiment, μ-EDM system used the applied voltage of 100 V, a single RC pulse timing circuits with 500 pF and 1 KΩ, and a square copper electrode with one side length of 130 μm and structural height of 1500 μm fabricated by wire electrode discharge gliding (WEDG)[18]. The work pieces for shadow masks are 100 ± 5 μm thick stainless steel (304 SS) with the size of 1.5 cm × 1.5 cm. After serially machining 150 μm square contact holes using μ-EDM, the combinational process of
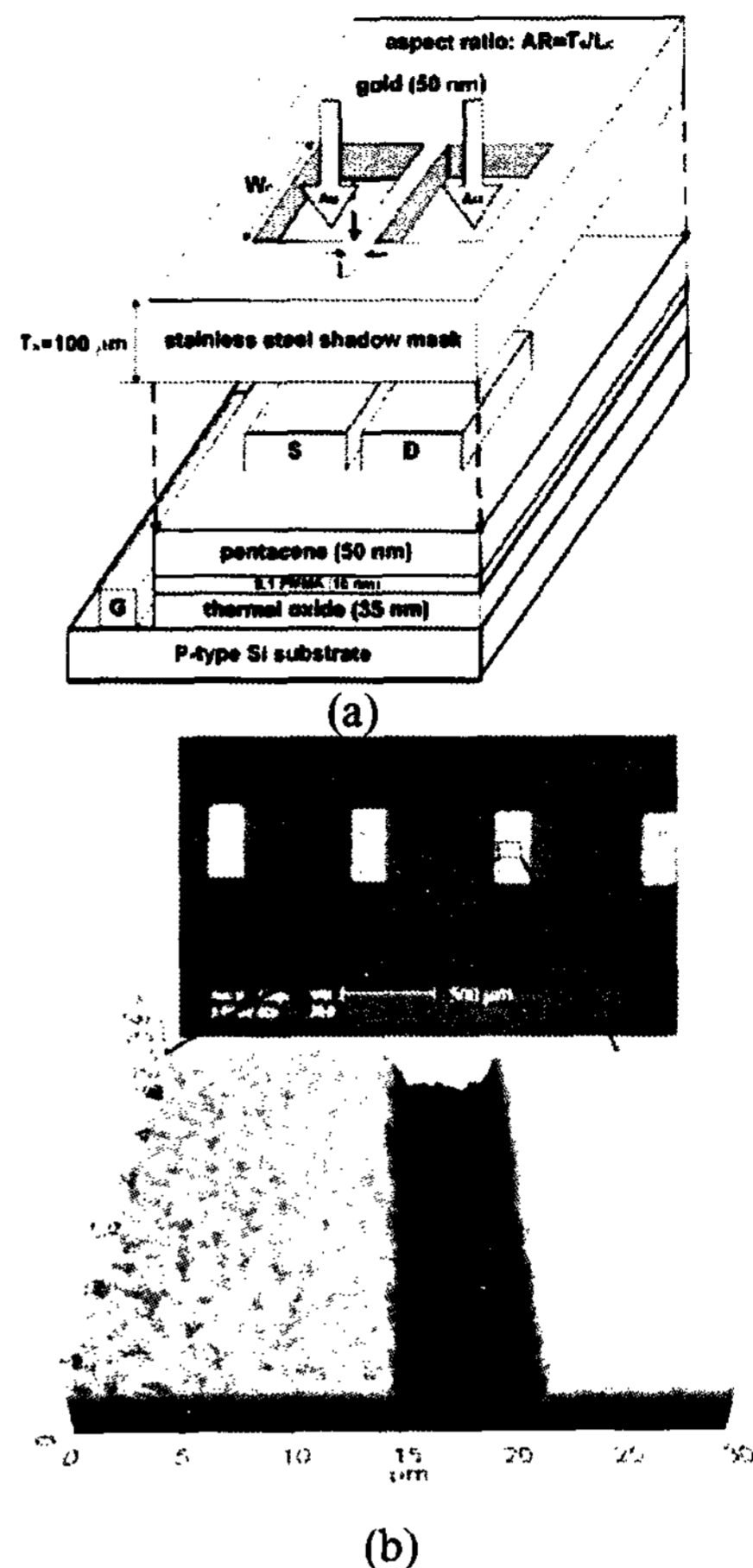

(a)

(b)

FIG. 2. (a) Schematic illustration of process steps for pentacene TFTs fabricated using an HR metal shadow mask. The width of the wall (L_C) for metal shadow masks ranges from 20 μm to 5 μm with a fixed channel width of 150 μm. (b) SEM image of pentacene TFTs with a channel length of 5 μm after measurement of electrical characteristics and AFM image of the channel area of a pentacene TFT.

ECE improves the AR of a metal shadow mask noticeably because the μ-EDM has a fundamental limit of the routinely machinable feature size ($L_C \approx 10$ μm) as shown in Fig. 1(c). Figure 1(b) shows that process conditions of ECE system are the applied voltage of 1.2 V and the 0.1 mole H_2SO_4 solution as electrolyte. Figure 1 (c) and (d) showed SEM images for a metal shadow mask after μ-EDM and ECE steps, respectively. To date, the length (L_C) and width (W_C) of the bridge can be routinely obtained as

small as 5 ± 0.25 μm and 70 ± 1 μm, respectively.

Figure 2(a) shows a schematic for the fabrication steps of pentacene TFTs. For a gate insulator, 35 nm thick thermal oxide was grown on a p-type wafer with the resistivity of 15 Ωcm. The thermal oxide was patterned by photolithography, and then etched by dilute HF solution for a gate electrode deposition. After cutting the patterned Si wafer to the size of 2 cm × 2 cm, each sample was spin-coated with a dilute PMMA solution to improve the ordering of pentacene due to the hydrophobic ending group methyl radical (-CH₃) [19]. The coated PMMA thickness was 10 nm as measured by ellipsometery. A 50 nm thick pentacene was thermally evaporated on the PMMA treated gate oxide at a rate of about 0.3 Å/sec. During the deposition, the substrate temperature maintained at the temperature of 90 °C in the pressure of 8×10^{-8} torr. Pentacene was purchased from Aldrich Company, and its purity was about 98 % based on a CHN (carbon, hydrogen, and nitrogen) elemental test. The pentacene source in this experiment was used without purification. Finally 50 nm of gold was e-beam evaporated on pentacene active layer through a 100 μm thick HR shadow mask to define S/D contacts as well as the gate contacts. The dimension of source and drain contacts have the channel length ranging from 20 μm to 5 μm at a fixed channel width of 150 μm. Figure 2 (b) shows the AFM and SEM image of channel area for an OTFT with W_C=150 μm and L_C=5 μm. As shown in Fig. 2 (b), the defined source and drain contacts have a good straight channel.

Figure 3 shows that electrical transfer and output characteristics of pentacene TFTs fabricated by an HR shadow mask with the L_C of 5 μm and W_C of 150 μm. From the transfer characteristics as shown in Fig. 3(a), a saturation mobility of 0.498 ± 0.05 cm²/Vsec, a current on/off ratio of 1.6 × 10⁵, a subthreshold swing (SS) of 2.5V/dec, and a threshold voltage of 0 V are extracted. The comparatively low level of current on/off ratio and SS are attributed to the periphery areas of pentacene layer, whereas the electrical performances can be improved by removing periphery areas of pentacene [20]. As
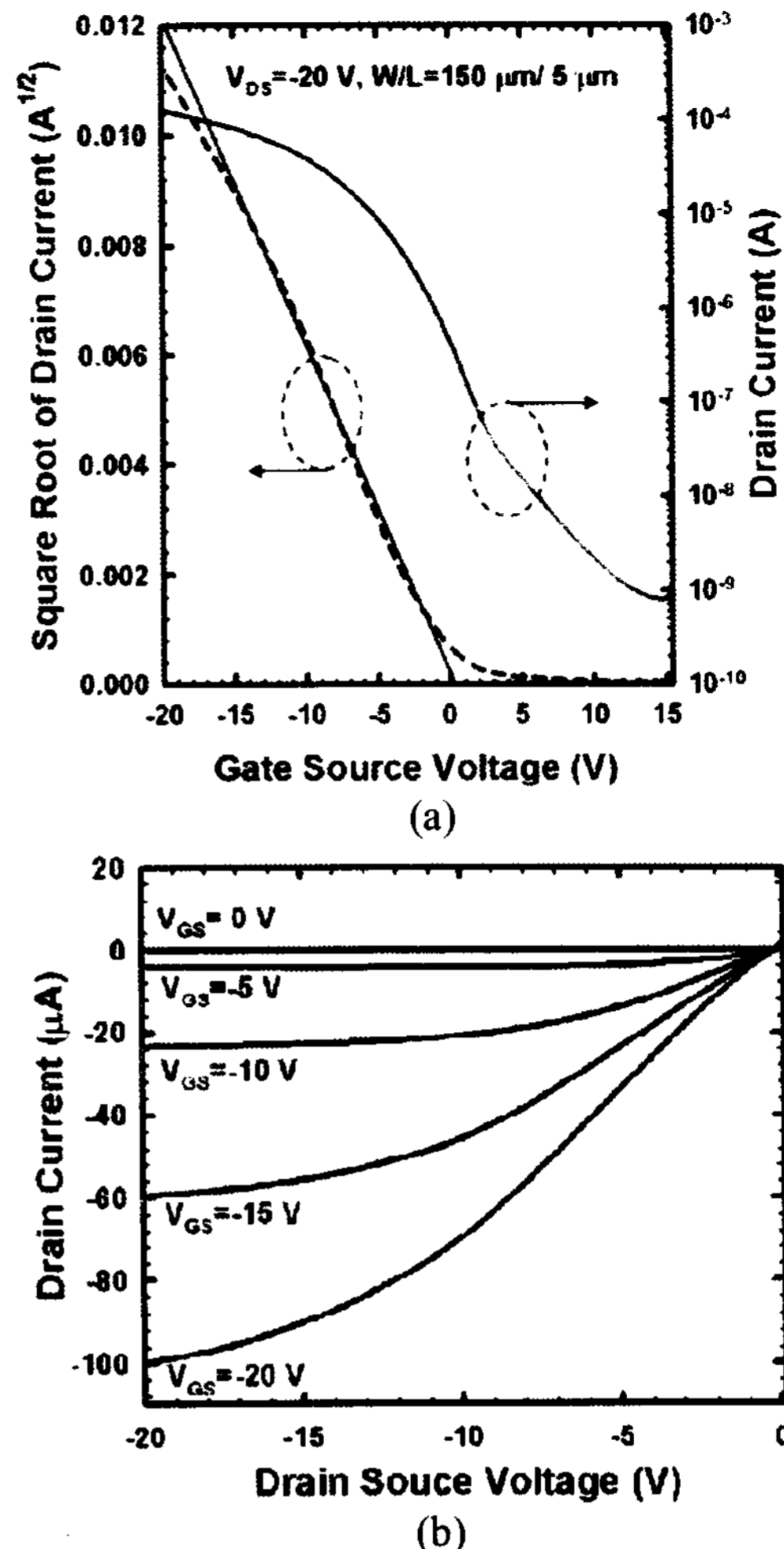

(a)

(b)

Fig 3. (a) Transfer and (b) output characteristics of a pentacene TFT with the ratio of W/L=150 μm/5 μm

shown in Fig. 3(b), a pentacene TFT has the nice saturation characteristics and the saturation current of 100 μA at the voltage of $V_{DS} = V_{GS} = -20V$.

3. Conclusion

We have proposed metal shadow masks with a high aspect ratio (AR > 20) using μ-EDM and ECE for high definition of S/D contacts (L ≤ 5 μm and W ≤ 150 μm) on organic semiconductors. The fabricated pentacene TFTs with the channel length of about 5 μm showed routinely mobility of 0.498 ±0.05 cm²/Vsec and current on/off ratio of 1.6 × 10⁵. The HR metal shadow masks with high aspect ratio more than

20 can be used repeatedly for S/D electrodes deposition due to the structural robustness. The pentacene TFTs by HR shadow masks can meet the required OELD pixel resolution ($\leq$ 100 × 100 μm^2) as well as high current drivability through the scaling-down of the width of OTFTs [11]. In addition, a batch mode μ-EDM can potentially solve a throughput and yield problem of HR metal shadow mask generation.

4. Acknowledgements

5. References

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