Technology of Organic Thin-Film Transistors for Active-Matrix Display

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Abstract

A method of improving device performance of OTFT was investigated. The mobility of device is more than 0.51 cm^2/Vs and I_{on}/I_{off} is higher than 10^6. An Active-matrix LCD driven by OTFT was fabricated. The resolution of this panel is 64 × 128 pixels and the pixel size is 550 μm × 550 μm.

1. Introduction

An organic thin-film transistor (OTFT) can be formed on plastic substrate due its low process temperature, <150°C. Therefore, the manufacturing cost of OTFT is lower than Si TFT because the printing process can be employed. OTFT based on conjugated organic semiconductor have become attractive for use in flat panel display, smart cards, RF identification tags and large-area sensor arrays [1-3]. Most of the active layer of OTFT with high carrier mobility is polycrystalline. The high mobility observed in these materials is resulted from larger grain sizes and fewer grain boundaries which could reduce the potential barriers that would impede the carrier motion from one crystallite to another [4-6]. While OTFT is applied to electronic components, the importance of the passivation layer become obvious. The electrical properties of OTFT such as the saturation current, the off current, the voltage threshold, and the sub threshold slope are affected by moisture, oxygen or chemical solution. Therefore, the phenomenon of degradation of OTFT under different environment has to be analyzed.

2. Experiment

The OTFT arrays with 64×128 pixels has been fabricated by solution process and thermal evaporation process. The device structure is the bottom gate structure. The process flow of OTFT arrays is shown in Figure 1. In Figure 1(a)-(e), the indium tin oxide (ITO) is deposited and patterned on substrate as a gate electrode and storage capacitor. Silicon dioxide or polyimide is deposited by PECVD or spin coating to form the insulator. ITO is used as the source/drain electrode material. The channel length and width are 50 and 500 μm, respectively. A typical interlayer layer is prepared by spin coater to enlarge the pentacene grain. Pentacene is deposited on channel by thermal evaporation and the pressure is controlled at less than 5×10^{-5} Pa. The substrate is heated to 70°C and the deposition rate is about 1 Å/sec during pentacene deposition. The thickness of pentacene is 1000 Å and interlayer layer is 800Å, measured by α-step. Different kinds of polymer solutions are spin coated to protect the pentacene and the thickness is about 6000 Å. A polyimide is coated for the LC alignment as shown in Figure 1(f) and (g). The integration of OTFT arrays and color filter is shown in Figure 1(h).

(a) ITO deposition and patterning as a gate electrode

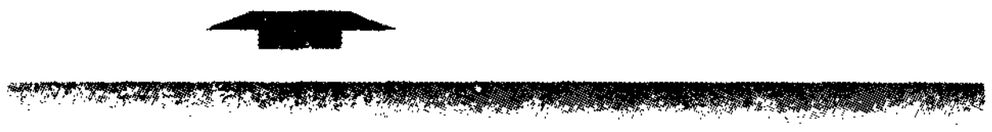
(b) Deposition of insulator

(c) ITO deposition and patterning as a source and drain electrode

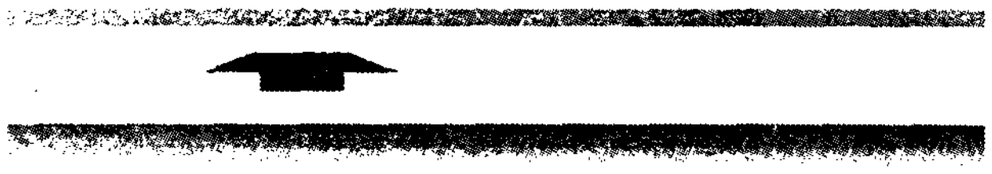
(d) Interlayer layer coating

(e) Pentacene thermal deposition as an active layer

(f) Polymer passivation layer coating



(g) PI layer coating for LC alignment



(h) LC injection and sealing

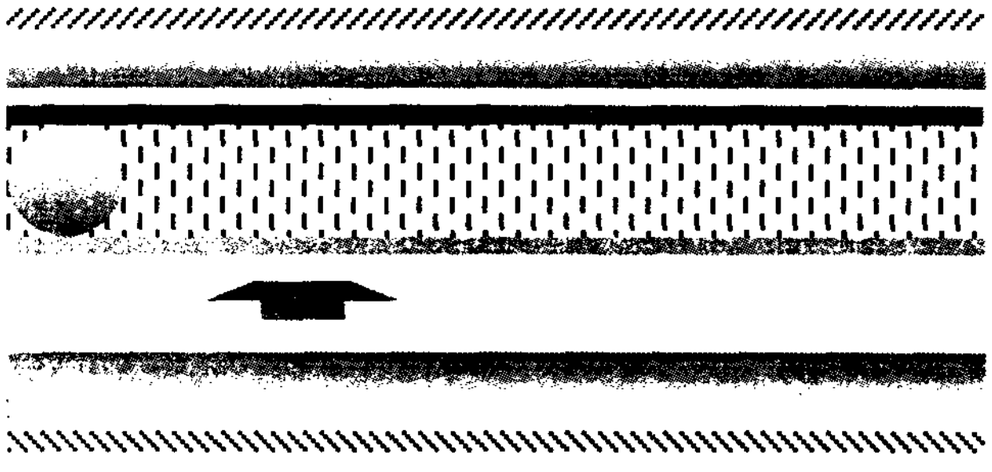


Figure 1. Process flow of OTFT-LCD.

3. Result and Discussion

The effects of the measuring conditions on the performance of OTFT device without coating any interlayer in air and in vacuum are investigated. Figure 2 shows the output characteristics of a pentacene transistor at various values of gate voltage (V_G). Measurements were made firstly in air and then in a vacuum at 10^{-6} torr. The output current of a pentacene transistor under high vacuum is clearly larger than that in air. The magnitude of the maximum saturation in vacuum is nearly four times that in air.

Figure 3 plots the I_D-V_G and $I_D^{1/2}$-V_G characteristics of a pentacene transistor at a V_{DS} of -100 V. Under high vacuum, the off-current of the pentacene transistor is lower and the on-current is higher than those in air. A field-effect mobility of the pentacene transistor is 0.43 cm^2/Vs under vacuum. The modulated on/off ratio is 10^6; the threshold voltage is -7.26 V and subthreshold slope is 1.7 V/decade. However, the device in air performed poorly, exhibited a field-effect mobility of around 0.11 cm^2/Vs, an on/off ratio of near 10^5, a threshold voltage of -20 V and a subthreshold slope of 5 V/decade. A high vacuum environment markedly improves the performance of the pentacene transistor. Clearly, the charge transport characteristics of pentacene depend strongly on the vacuum condition.

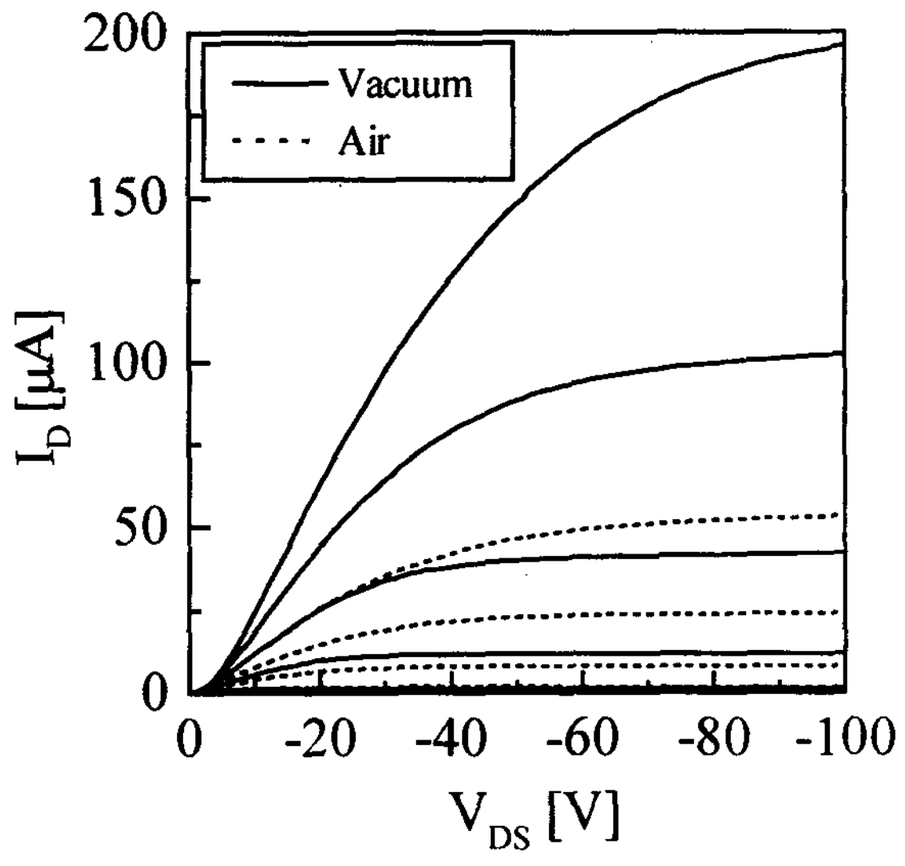


Figure 2. I_D-V_{DS} characteristics of a pentacene transistor measured in air and in a vacuum. The V_G was varied from -20 V to -100 V with -20 V step.

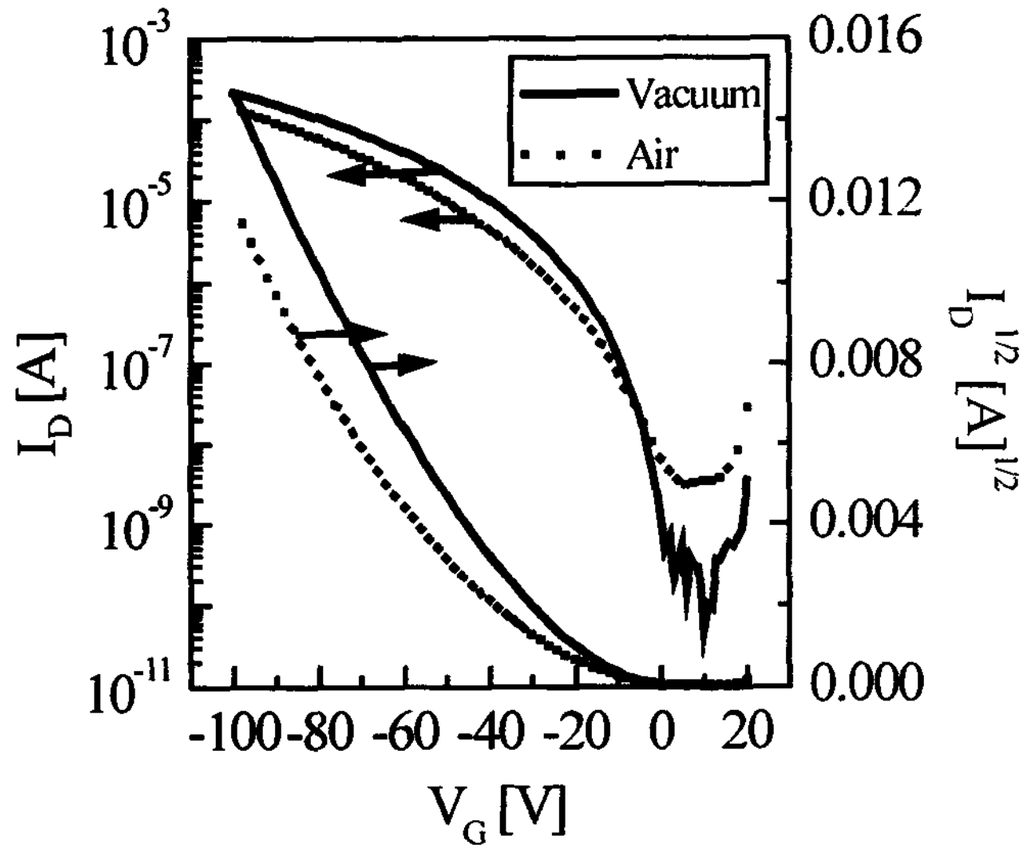


Figure 3. Log (I_D)-V_G (left-axis) and (I_D)$^{1/2}$-V_G (right axis) characteristics of a pentacene transistor measured in air and in a vacuum with a V_{DS} of -100 V.

The electrical characteristics of pentacene are strongly affected by the grain size of pentacene. Therefore, the polyimide coating is integrated into process to improve the surface condition. The atomic force microscopy (AFM) images of pentacene are shown in Figure 4. In Figure 4(a), the grain size of pentacene on the non-treated silicon dioxide is about 100~200 nm. With PI interlayer on silicon dioxide substrate, the grain size of pentacene is increased to 2~3 um, as shown in Figure 4(b).

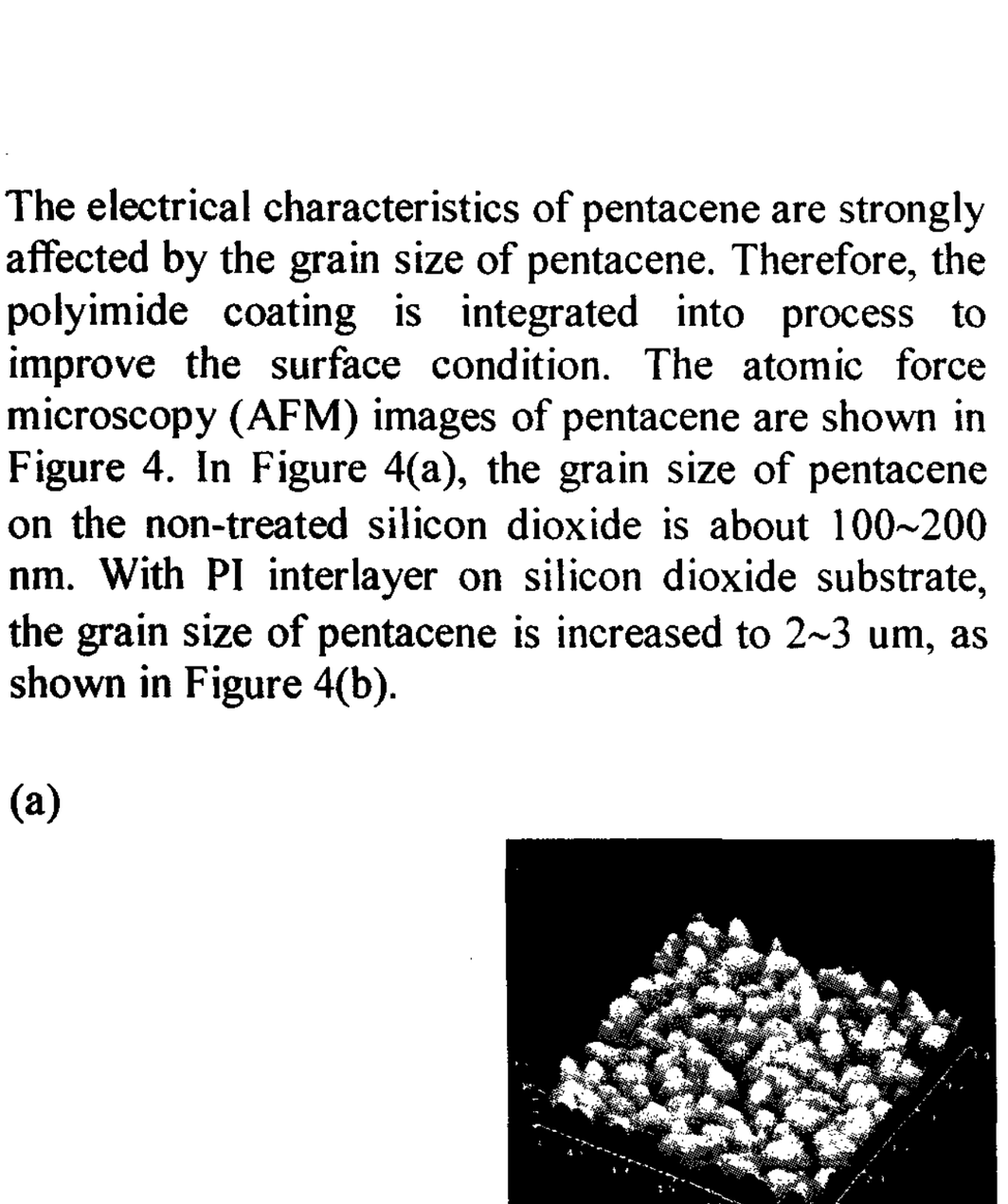


Figure 4. AFM images of pentacene deposited onto (a) SiO_2, (b) SiO_2 coated with polyimide interlayer

Furthermore, the wide angle X-ray diffraction, as shown in Figure 5, is employed for pentacene grain analysis. In Figure 5, the crystallinity of pentacene is obviously increased by PI treatment. There are two kinds of crystal phases inside pentacene grain. One is thin-film phase and the other is bulk phase. The thin-film phase of pentacene on polyimide and on pure SiO_2 is about 97 % and 40 %, respectively. Therefore, high crystallinity could be achieved by the polyimide interlayer coating. The field-effect mobility and on/off current ration of the device without PI interlayer are 0.02~0.1 $cm^2/V{\cdot}s$ and near 10^5. The field-effect mobility and on/off current ration of the device with PI interlayer are 0.51~2.0 $cm^2/V{\cdot}s$ and larger than 10^6.

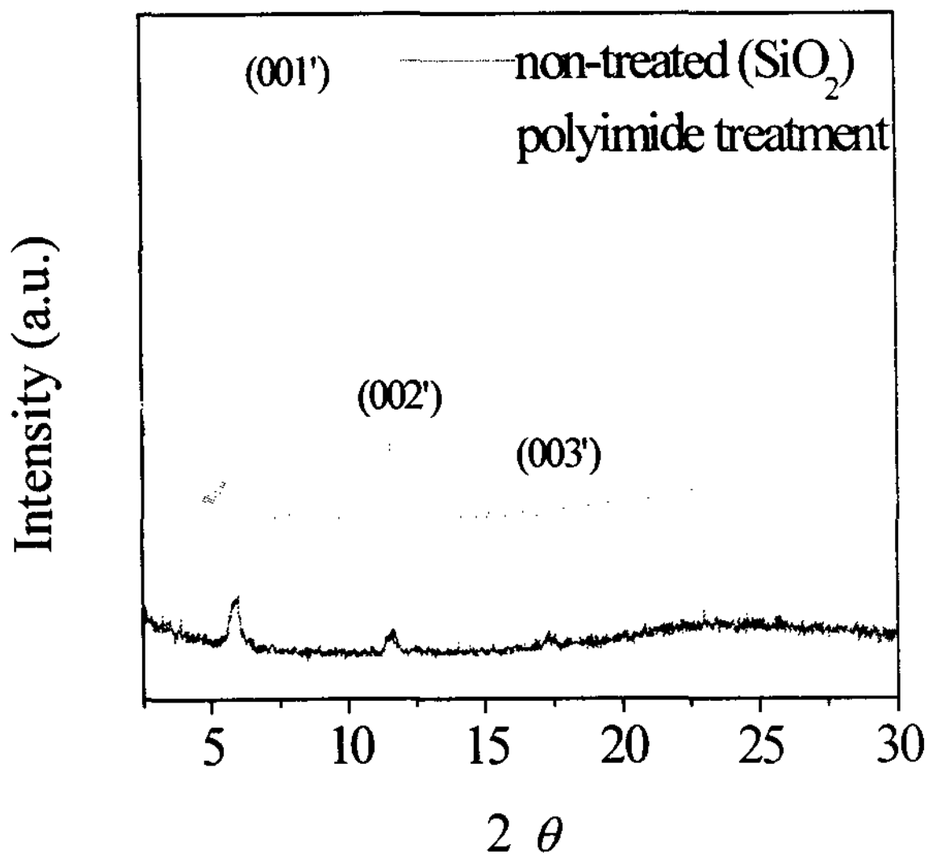


Figure 5. X-ray diffraction patterns of pentacene.

Based on the OTFT investigation, an active-matrix LCD driven by OTFT arrays was designed. In the pixel design, there are one p-type transistor and one storage capacitor as shown in Figure 6. The channel length and width are 50 and 500 μm, respectively. The area of pentacene is 100 μm × 500 μm. The monochrome and color twisted nematic liquid crystals display are driven by pentacene OTFT, as shown in Figure 7. The resolution of this panel is 64 × 128 pixels and the pixel size is 550 μm x 550 μm.

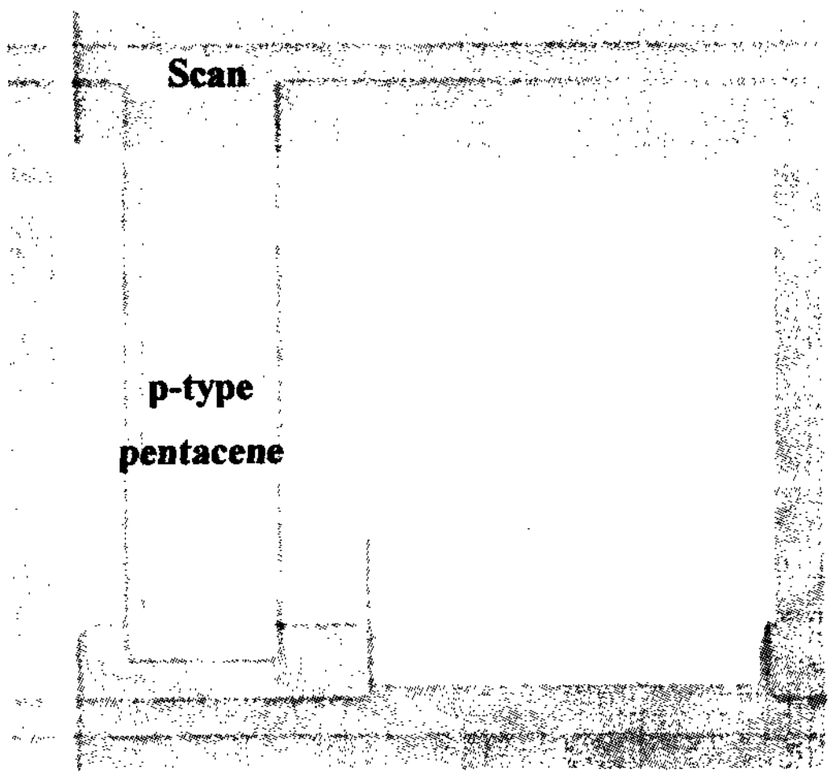


Figure 6. Layout of one pixel of OTFT

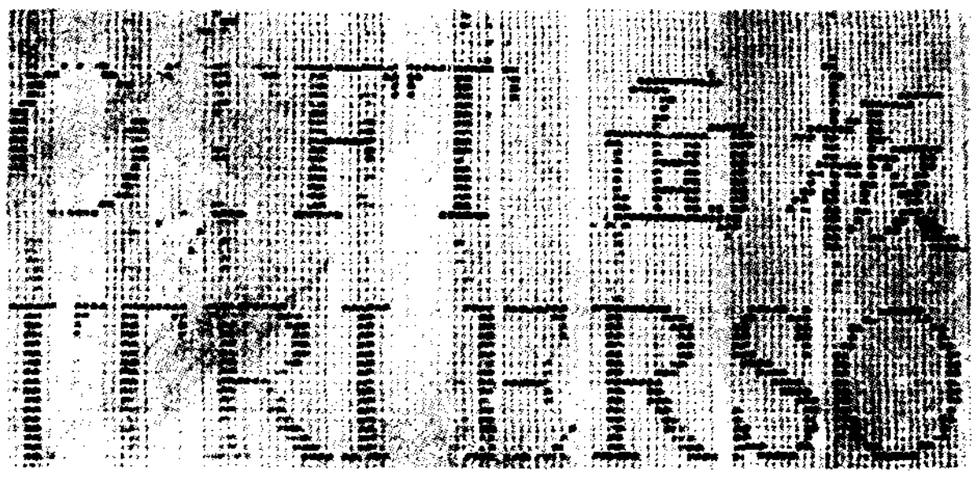


Figure 7. Display images of OTFT-LCD.

4. Conclusion

The field-effect mobility and on/off current ration of the device are approaching 0.51~2.0 $cm^2/V \cdot s$ and 10^6. A 3 inch twisted nematic liquid crystals display panels driven by OTFT arrays of 64 x 128 pixels was fabricated.

5. References

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