New Address Electrode Suitable for Fast Addressing with High Xe ac-PDP

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Abstract

New address electrode having separated dual electrode is suggested to reduce addressing time in ac PDP. Addressing characteristics of suggested electrode has been investigated in the test panel with high Xe partial pressure. It has been found that both the formative and jitter width of the suggested electrode is improved by 10 –20 % over the wide range of address voltage level compared with the conventional one. The dynamic margin of the panel also greatly improved. The key feature behind this type of structure is that it can extend the controllability of the wall charge distribution during the reset and address discharge without significant increase in capacitive load of address electrode.

1. Introduction

High Xe partial pressure gas mixture has recently been introduced in PDP industry to increase luminous efficiency and luminance. However as Xe content increases, many side effects simultaneously occur such as increase of driving voltage and address time. Therefore, reduction of discharge time lag during addressing discharge and operating voltage is necessary for improving performances of high Xe PDP. Especially, fast writing of picture data is very important in realizing single scan in high Xe, XGA grade panels, which makes the optimization of address electrode inevitable.

With this background, we have tried to improve PDP driving characteristics by modification of the structure of address electrode.

2. Experimental

Figure 1 shows one example of suggested electrode structure. Important feature is separation of the address electrode with keeping the total width at moderate value. In this configuration, we can extend the controllability of wall charge distribution and capacitive load of address electrode. The address electrode shown in this particular example has 40um, 60um in width and 40um gap size. Total width of 100um is the same as that of the reference design with conventional style used in this work.

Before testing the performances of suggested electrode, fundamental driving properties have been investigated as a function of Xe partial pressure in conventionally designed 7" test panel having Xe-Ne gas mixture. Cell dimensions of the test panel are equal to 42" VGA grade commercial panels. The characteristics of suggested electrode have been compared in Xe contents of 4% with the conventional electrode in terms of dynamic margin, discharge time lag and jitter width in address discharge.

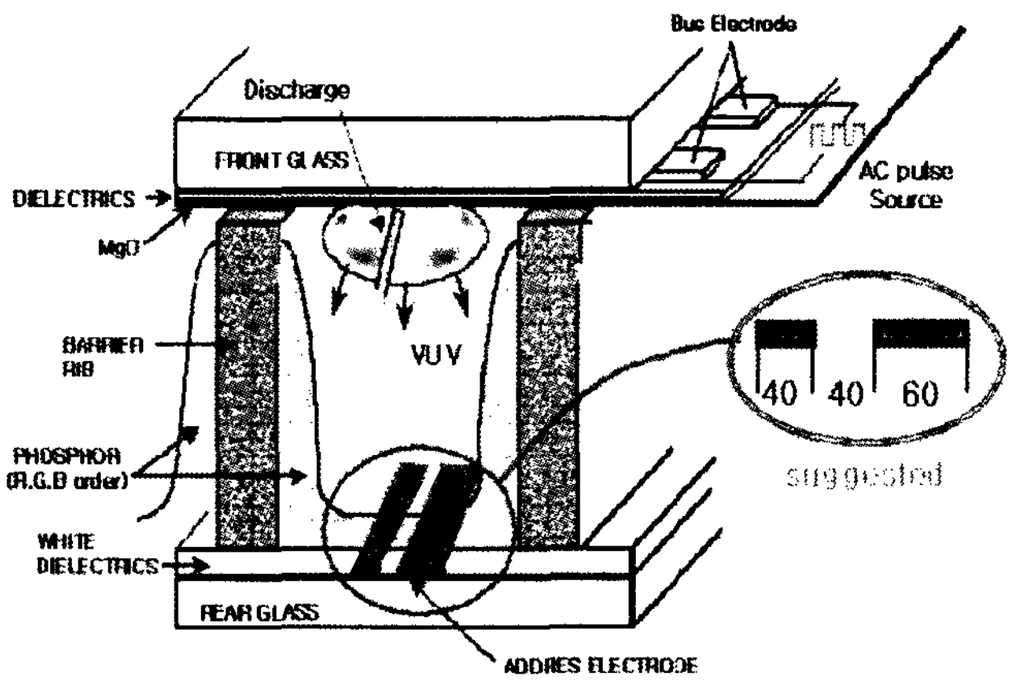

Fig 1. Structure of separated address panel

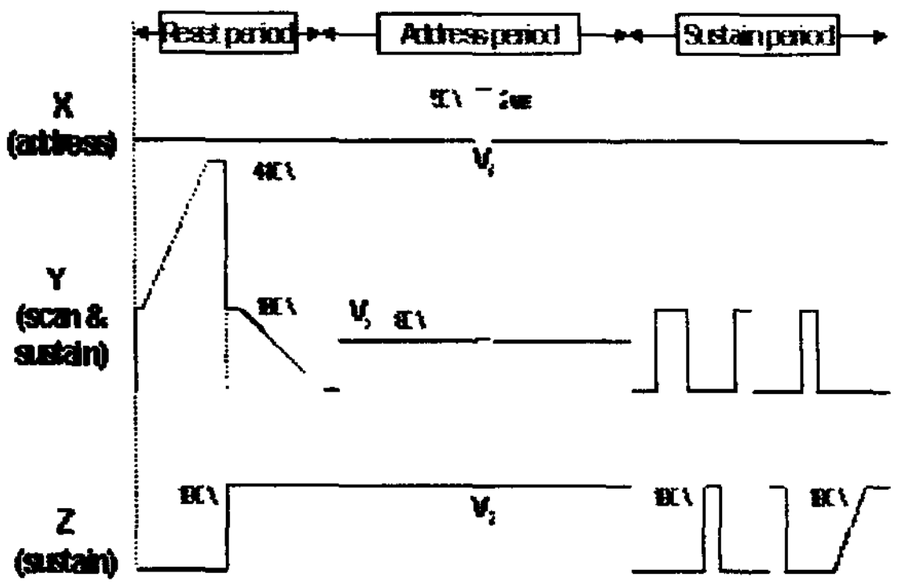

Fig 2. Driving waveform of ADS method

Figure 2 shows the driving waveforms of ADS method used in this experiment. ADS waveform of ramp method is used. The total period is 1.63ms, In the reset period, the ramp rising time is 100μs and the ramp falling time is 150μs. The address period is designed as about 1ms in order to make the same condition as the conventional 40-inch PDP. The pulse width of one address is about 3μs.

3. Results and discussion

Figure 3 shows the correlations between frequency and driving voltage (mid-value between maximum and minimum sustain voltage) in the given Xe %. As frequency increases, the static driving voltage of panel decreases gradually, regardless of Xe %. The values of driving voltages in 4%, 6%, 8% and 10% are 181V, 195V, 207V and 221V. This shows approximately 5V decreases between Xe 4% and 10%.

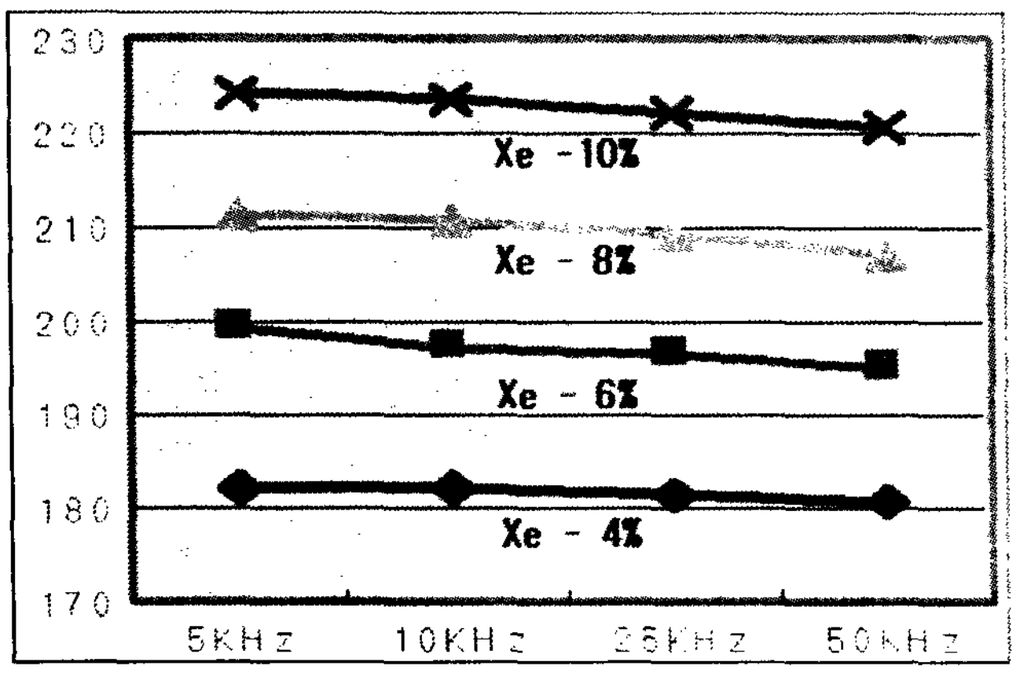

Fig 3. Driving voltage of each panel according to Xe% variation

Figure 4,5 show the discharge delay according to temperature and jitter width variation, in panels of Xe 4%, 6%, 8% and 10% in address voltage 70V. The variation of discharge delay changes 0.2μm at high and room temperature. The variation of jitter width at room temperature become longer as Xe increases from 4% to 10 % but R, G, B converges 0.4μm at high temperature.

Collectively, Address Time of R, G, B is as follows

(Add Time = Address discharge delay + jitter width)

Add Time of Green: 2.0 ~ 2.5μs

Add Time of Red : 1.2 ~ 1.9μs

Add Time of Blue : 1.0 ~ 1.4μs

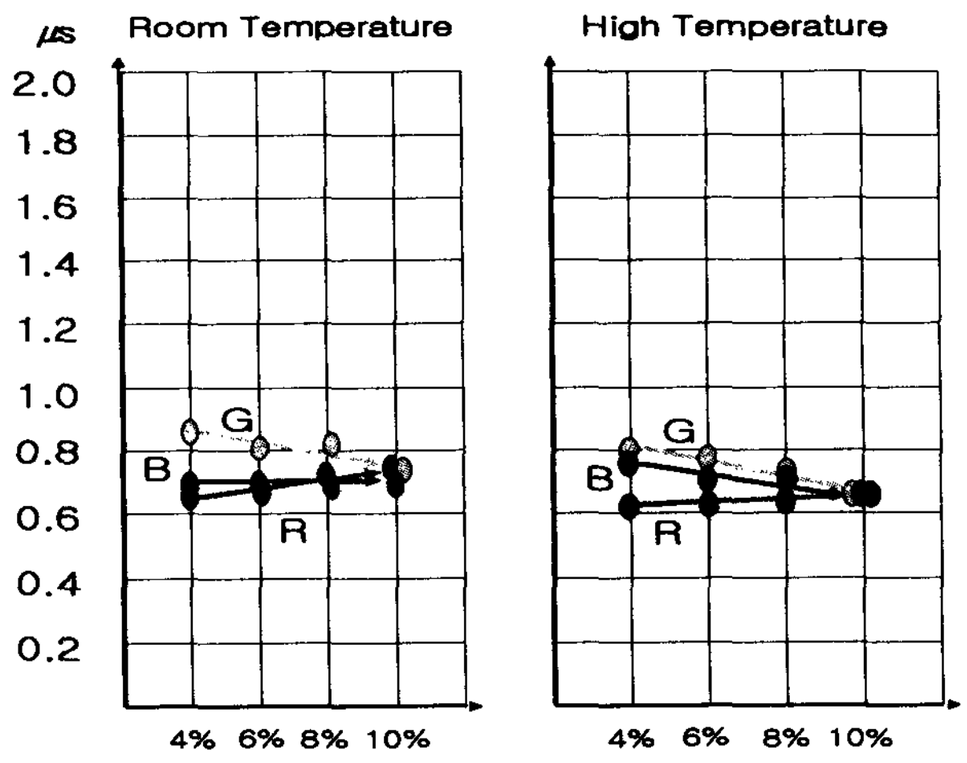

Fig 4. Variation of discharge delay according to Xe% and temperature

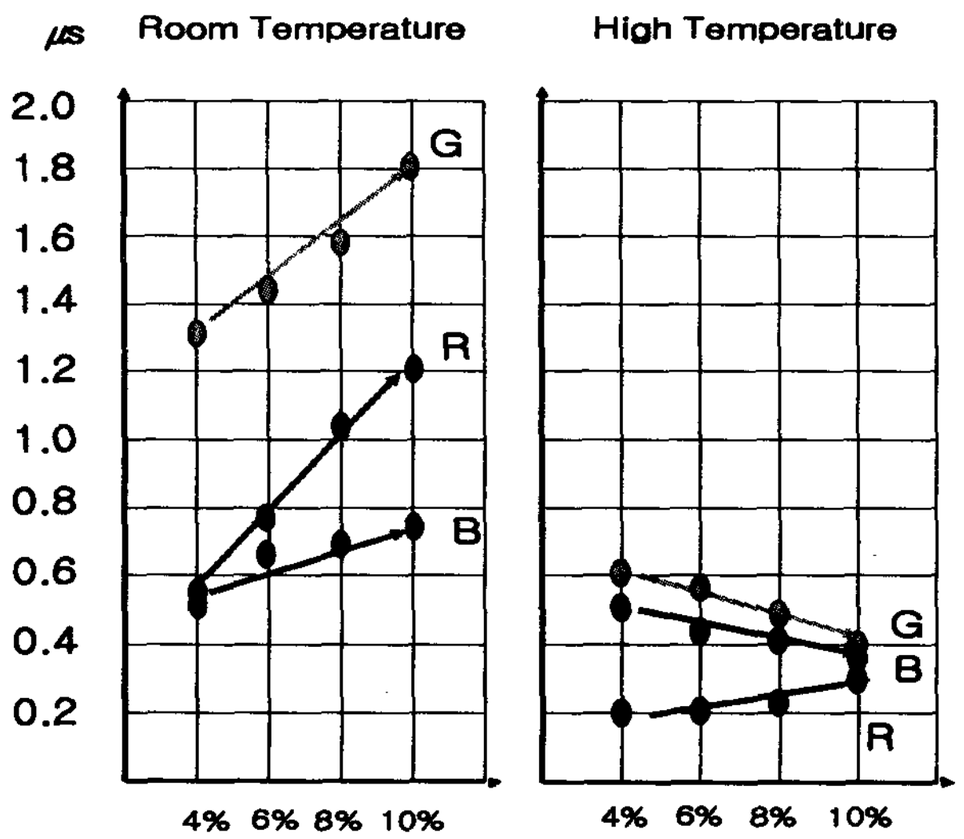

Fig 5. Jitter width variation according to Xe% and temperature.

Fig 6(a) shows the outline of discharge delay and (b) shows the outline of jitter width.

Discharge delay time and jitter width of the suggested structure is reduced to approximately 10 - 20 % over standard structure

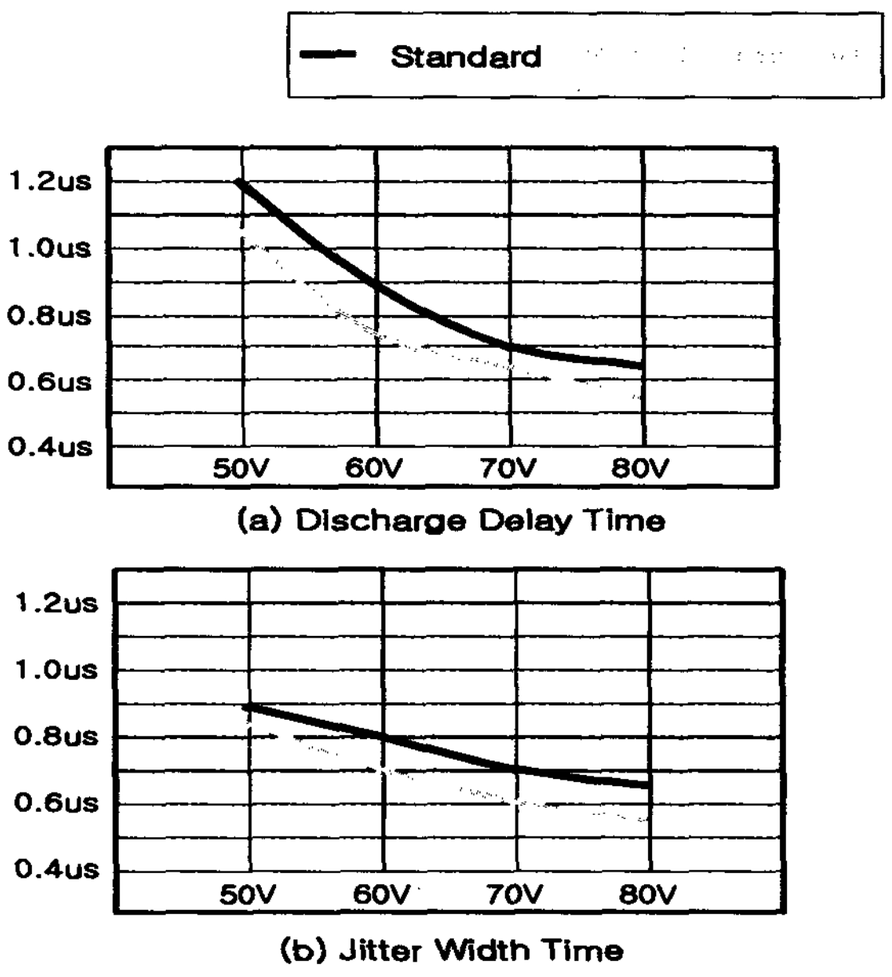

Fig 6. Improvement of Formative time lag and Jitter width in suggested electrode

Fig 7 shows the variation of dynamic margin of standard structure and suggested separated structure. Fig 7 (a) shows the dynamic margin between setup voltage and sustain voltage and (b) shows the dynamic margin between address voltage and sustain voltage.

Dynamic margin of the suggested structure is broader than the conventional structure. As its broadened margin domain is more stable in discharge, discharge delay time and jitter width is reduced.

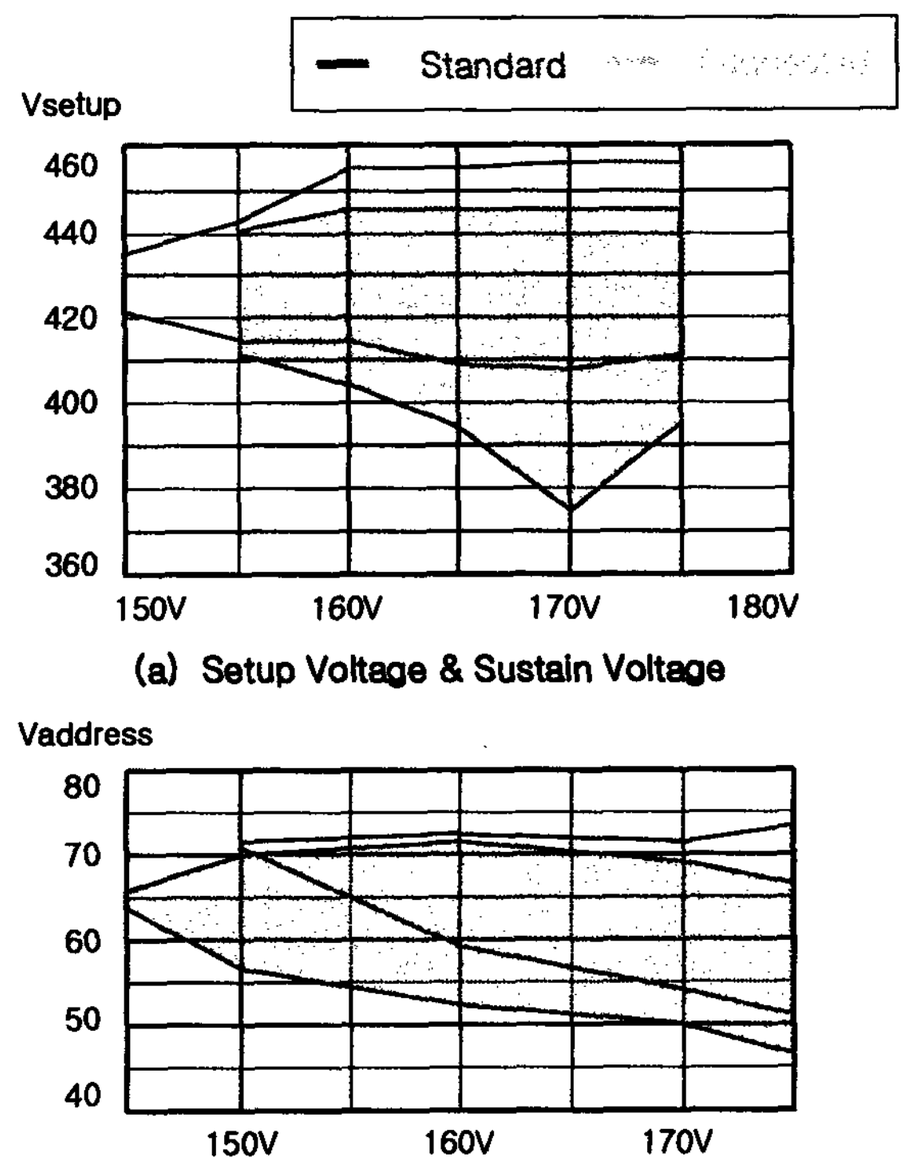

Fig 7. Dynamic margin characteristics of suggested structure

4. Conclusion

In this paper, the discharge characteristics of AC PDP panel included Xe gas are estimated to improve luminance and luminous efficiency.

Discharge delay is almost steady but because variation of jitter width is larger as the amount of Xe gas increases, misfiring discharge can be occurred in address discharge.

Our work shows that writing speed and driving

margin can be improved by simple modification of address electrode structure. Although our work needs more refinements, the results suggest that optimal design of address electrode based on the optimal wall charge distribution is necessary for fast and stable operation of PDP especially for high Xe gas mixture system.

5. References

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