Dynamic Digital Logic Style for LTPS TFT Based System-On-Panel Application

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Abstract

We developed a dynamic logic architecture which resulted better leakage current, lower power consumption and less area compared to the conventional dynamic logic structures. We demonstrated the advantage from HSPICE simulation and test chip design has been completed.

1. Introduction

In recent years, poly-silicon thin film transistor (TFT) characteristics have been improved very fast and people expect serious system-on-panel(SOP) application will be debuted within 3 to 5 years.[1] However, the LTPS TFT characteristics are far inferior to bulk and/or SOI MOSFET's. Therefore, one needs to find some way of designing faster TFT Logic circuit with given TFT properties.[2] [3] [4]

In this paper, we propose the new dynamic digital logic which we named as "clocked ground logic".

2. The proposed dynamic digital logic

We focused on high leakage current and low source/drain junction capacitance of LTPS TFT's. The high leakage current is responsible for the high DC power consumed by TFT logic while the low source/drain junction capacitance is advantageous to provide high speed operation.

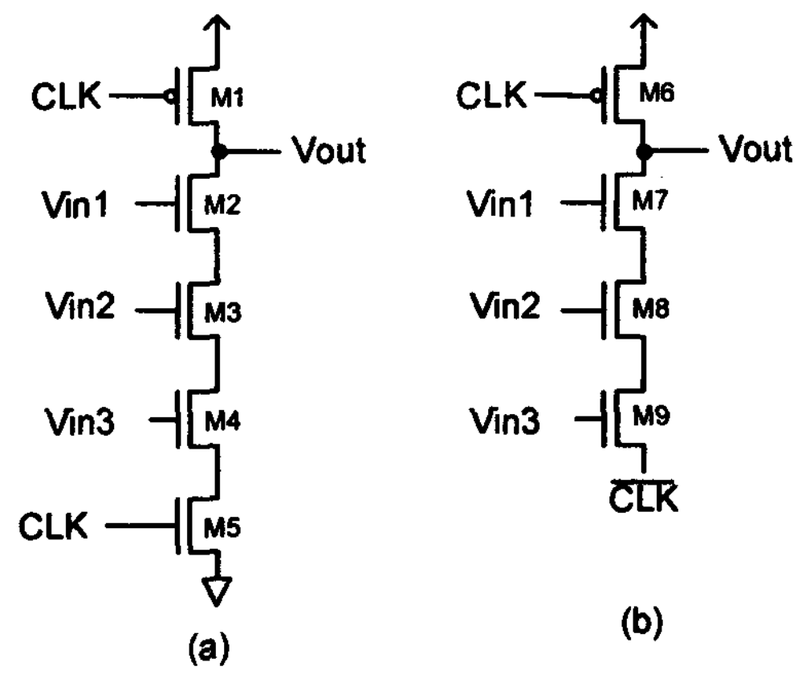

Figure 1. (a) Conventional dynamic 3 input NAND gate, (b) Clocked ground dynamic 3 input NAND gate.

Figure 1 (a) and (b) show the conventional and clocked ground dynamic 3 input NAND gates, respectively. Instead of M5 in Figure 1 (a), /CLK signal is applied in the clocked ground logic as shown in Figure 1 (b). /CLK signal is applied to the source of the n-type TFT pull down device(Transistor M9). Leakage current through the n-type TFT should be zero when the output is precharged to VDD during CLK='Low'. Because the voltage of M9 source node is VDD, no drain to source current can flow. This logic circuit

style has not been used in bulk MOSFET's since they have relatively large source/drain junction capacitance.

In addition, clocked ground logic does not need the pull down nMOSFET compared with conventional logic. This results smaller chip-area for the clocked ground logic.

Figure 2 (a), (b) and (c) show the conventional, clocked ground and modified clocked ground dynamic inverter, respectively. The operation of Figure 2 (c) is divided into two phases. In precharged phase, high /CLK signal is applied. When Vin is 'low', Vout node is VDD by M6 and when Vin is 'High', Vout node is VDD by M7. In evaluation phase, /CLK signal is 'low'. This inverter operates like a static inverter. Therefore, circuits in Figure 2 (a), (b) and (c) performs the same logic function. Figure 2 (c) has the advantage of simplicity since the CLK signal was removed from figure 2 (b).

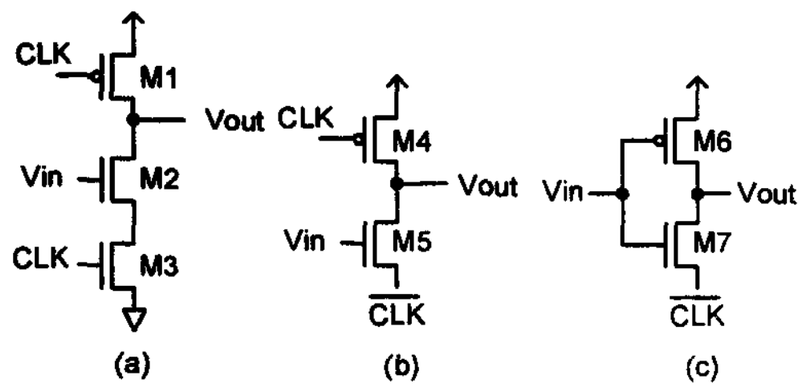

Figure 2. (a) Conventional dynamic inverter
(b) Clocked ground dynamic inverter
(c) Modified clocked ground dynamic inverter

3. Simulation results

Performance of the new design has been tested with HSPICE with RPI TFT device model. Static inverters are used for load at output node.

Figure 3 shows the simulated waveform of Figure 1. When all input signal is high, output of NAND gates are low. At this time, the simulation results show that operation of clocked ground style was faster than that of conventional style. The difference of falling propagation delay was measured to about 3 ns. In NOR case, it was measured to about 3.5 ns.

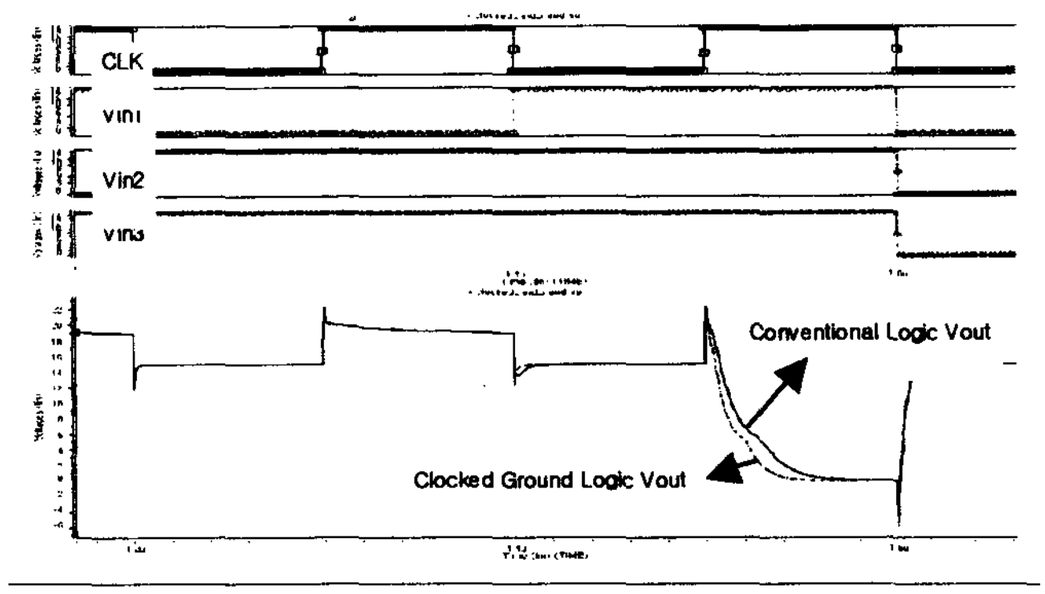

Figure 3. Simulated waveform of dynamic 3 input NAND gates designed in both conventional and clocked ground style.

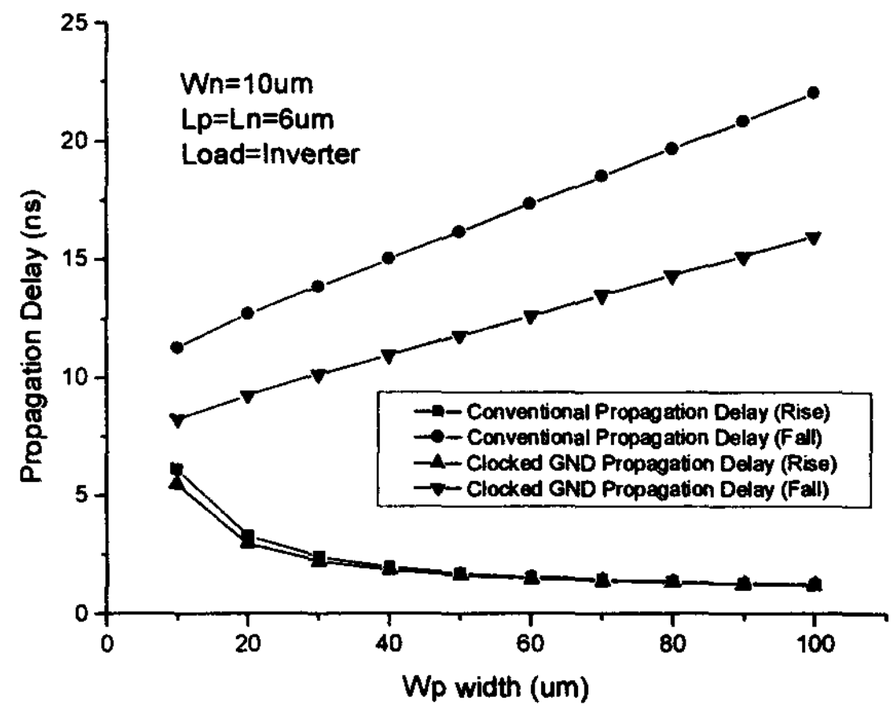

Figure 4. Propagation Delay of Dynamic 3 input NAND

Figure 4 and figure 5 show typical propagation delay characteristics of NAND and NOR, respectively. Since pull up network operation had not been changed, pull up(rising) propagation delay is almost identical for both design style. However, pull down(falling) propagation delay of the clocked ground style was siginificantly lower than that of the conventional design for both NAND and

NOR gates. Clocked ground style can reduce falling propagation delay.

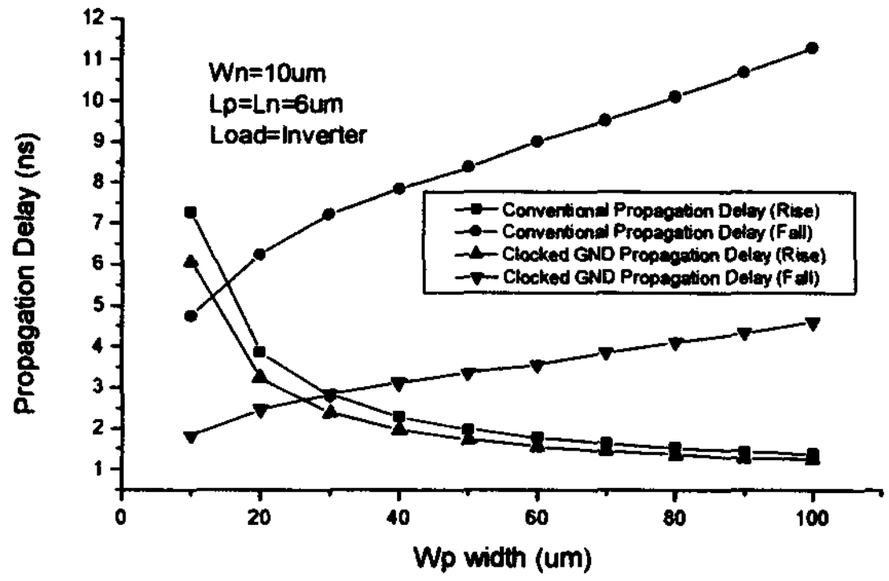

Figure 5. Propagation Delay of Dynamic 3 Input NOR.

Figure 6 shows the simulated waveform of dynamic inverter gates shown in figure 2. Output waveform of clocked ground dynamic inverter and modified clocked ground dynamic inverter is almost identical. The high to low propagation delay was improved by 4.5 ns in the clocked ground circuits. Figure 7 show typical propagation delay characteristics of dynamic inverters. Inverter of clocked ground style can also reduce falling propagation delay.

To demonstrate leakage property, we measured leakage current in NAND, NOR and inverter gates when CLK signal is 'low'. NAND gates of conventional and clocked ground style were measured to 350 nA, 129 nA, respectively. NOR gates of conventional and clocked ground style were measured to 140.8 nA and 6.56 nA, respectively. And inverter of conventional and clocked ground style was mesured to 166.5 nA and 40.5 nA This means that clocked ground style can reduce leakage current efficiently.

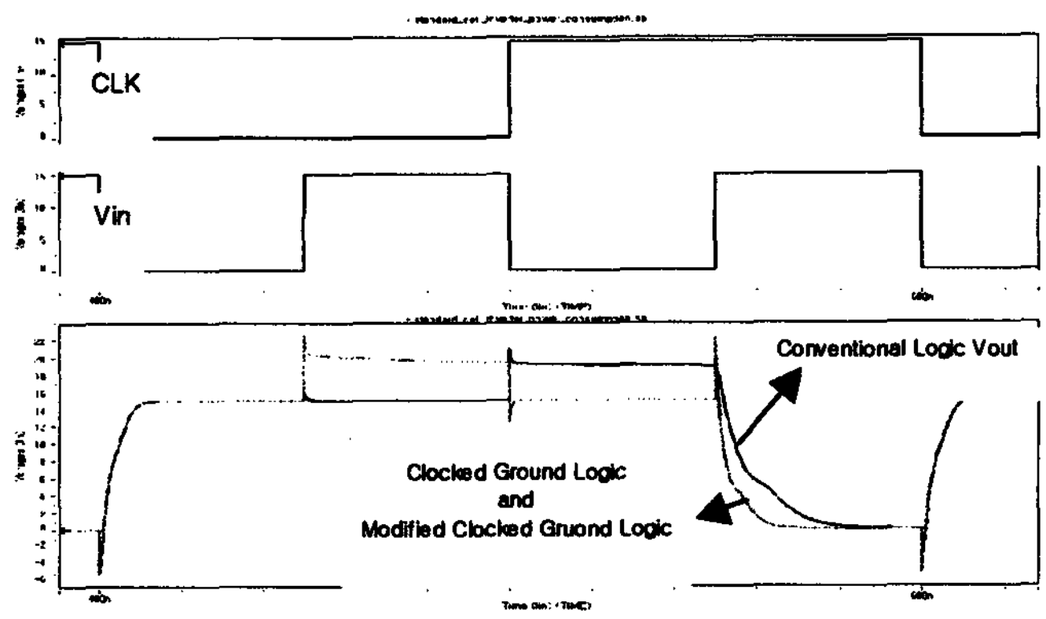

Figure 6. Simulated waveform of dynamic inverter gates shown in Figure 2.

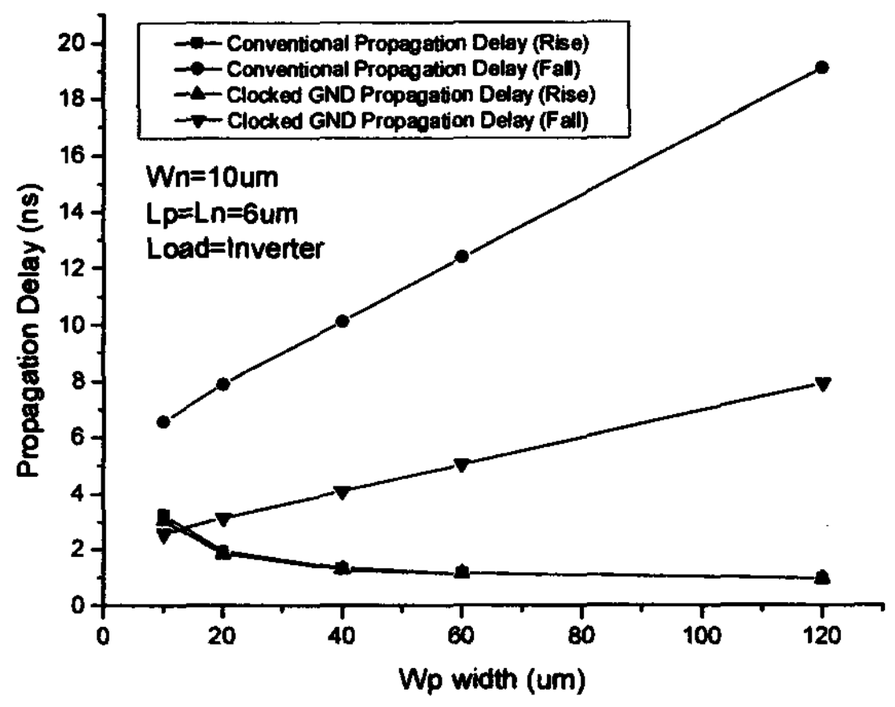

Figure 7. Propagation Delay of Dynamic Inverter.

Figure 8 shows the power consumption of NAND and NOR gates. We measured power consumption of NAND and NOR gates in precharged period. Clocked ground style can decrease the power consumption of NAND and NOR gates as see in figure 8. In inverter case, conventional and clocked ground style was mesured to 5.3 uW and 4.9 uW, respectively. Because it can decrease their leakage current during pre-charged period.

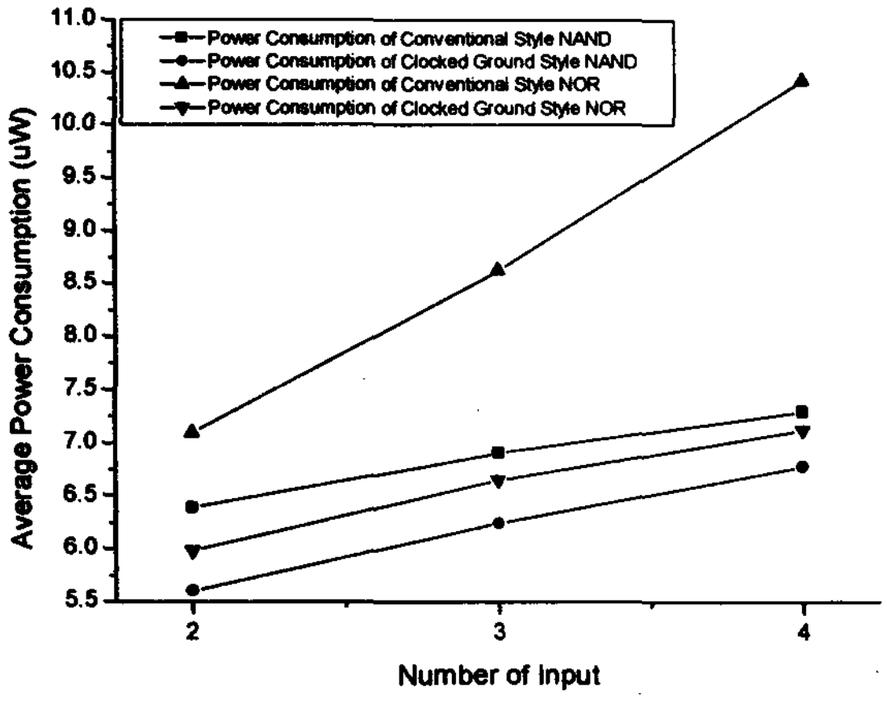

Figure 8. Power Consumption of NAND and NOR gates designed both conventional and clocked ground style.

4. Conclusion

We proposed a dynamic logic architecture which resulted better leakage current, lower power consumption and less area compared to the conventional dynamic logic structures. The propagation delay of proposed logic style was lower than of the conventional logic style.

The impact of this work is on the performance of logic circuits integrated in AMLCD or AMOLED panel. With proposed technique, one can obtain faster, more energy efficient, smaller area logic circuits.

5. References

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