# Layer-by-layer nitrogenation of microcrystalline silicon for TFT applications

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## Abstract

*We have optimized the low temperature growth of microcrystalline silicon at 80°C. This material has been used to fabricate* bottom gate μc-Si:H TFTs by using a layer-by-layer nitrogenation process. By using this process the amorphous incubation layer can be converted into silicon nitride and leads to an increase in field effect mobility of the TFT

## 1. Introduction

Currently the transistors used for active matrix liquid crystal displays (AMLCDs) are fabricated using hydrogenated amorphous silicon (a-Si:H) owing to its large area deposition capability. Future displays will however demand a material with higher field effect mobility than a-Si:H. Polycrystalline silicon (poly-Si) can meet these requirements but suffers from non uniformity over large area and low temperature substrate incompatibility. Thin Film Transistors (TFTs) on lightweight and robust plastic substrates are in high demand for small and medium size displays for mobile electronic applications such as mobile phone and personal digital assistants (PDAs). The fabrication of TFTs on plastic demands a very low temperature process < 150°C.

Low temperature microcrystalline silicon (μc-Si:H) is a biphasic material consisting of crystalline regions in an amorphous matrix and offers a large area, low temperature deposition process while providing an improvement in field effect mobility. μc-Si:H is conventionally deposited by Plasma enhanced chemical vapor deposition (PECVD) of $SiH_4/H_2$ [1]. μc-Si:H deposition by PECVD tends to produce grains with a conical structure. This results in the lower 5 to 10 nm of material being predominantly amorphous [2], [3] and [4] as a bottom gate TFT structure is preferred for display applications this presents a major problem because the accumulation layer is within the amorphous region and hence the field effect mobility of the device is low (<1 $cm^2 V^{-1} s^{-1}$). If a top gate structure is used then this effect is reduced as the accumulation layer coincides with the high crystallinity region. However, the channel layer has to be thick in order for high crystallinity to be achieved which causes the OFF state source-drain current to be increased. It is for this reason that high mobility μc-Si:H top gate TFTs tend to suffer from excessive OFF state currents [5 ]and [6].

In this paper, we report a new method to increase the mobility of bottom gate μc-Si:H TFTs. This is achieved using a layer-by-layer nitrogenation technique in which the bottom 50 nm of the μc-Si:H is converted into silicon nitride so that, when the device is switched ON, the accumulation layer will form in a region of high crystallinity.

## 2. Experimental

The μc-Si:H thin films were grown in an Astex PlasmaQuest Series III ECR reactor, as shown in Figure 1.

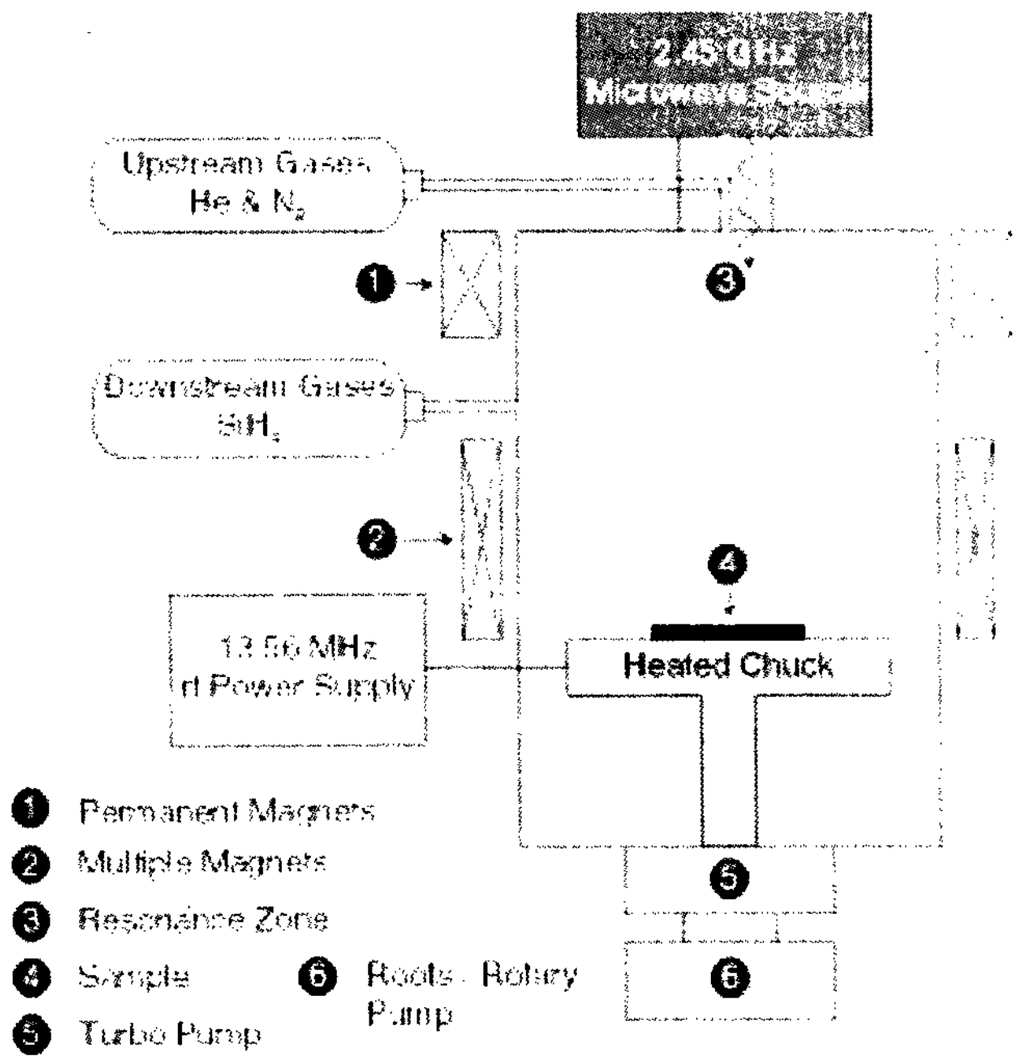


**Figure 1 Schematic ECR-PECVD system**

Corning 7059 glass and low doped, p-type, double sided polished crystalline silicon substrates were used for sample characterization. The thickness of the μc-Si:H samples was determined using a Dektak II profilometer. An ATI Unicam UV2 ultraviolet-visible (UV-vis) spectrometer with a wavelength spectrum of 190 to 1100 nm was used to find the optical Tauc gap. A RM 1000 Renishaw Raman system was used to determine the crystallinity of the film. Rutherford beam scattering analyses were done at the university of Surrey's Ion beam center. This work was carried out using a 2MV Tandetron accelerator from High Voltage Engineering. This machine is capable of generating proton beams up to 4MeV and alpha particle beams of up to 6MeV. Rutherford backscattering spectrometry (RBS) is an accurate, powerful and general thin film depth profiling technique carried out with about 1.558MeV He beams. The scattering angle was 166 $^0$ and the solid angle for detection was 1.6 msr with beam current of 70nA and a beam size 0.25mm×4mm.

The deposited μc-Si:H films were evaluated by Scanning electron microscopy (SEM) studies were carried out using a HITACHI S-5000 in-lens cold field emission SEM.

Bottom gate, inverted staggered structure TFTs were fabricated with *W/L* values between 10 and 1007, where *W* is the channel width and *L* is the channel length. In almost all cases, the channel length was 50 μm.

## 3. Results and discussion

The planar SEM picture, Figure 2 shows a typical μc-Si:H film, a biphasic material consisting of crystallites in an amorphous matrix. From Figure 2 the grain size is observed to be in the range of 10-50 nm

**Figure 2 Top-view SEM of a typical μc-Si:H deposited by ECR-PECVD**

Raman spectra of the μc-Si:H samples were used to analyze the crystalline volume fraction. There are usually two Raman peaks that appear in hydrogenated silicon in the range of 400-600cm$^{-1}$, the amorphous silicon peak at 480cm$^{-1}$ and the crystalline silicon peak at 520cm$^{-1}$. If the integrated intensity of the amorphous peak is $I_A$, the intermediate peak $I_i$ and that of the crystalline peak $I_C$ with $\lambda$ the ratio of integrated Raman cross sections for amorphous silicon to crystalline silicon, then the crystalline volume fraction $X_C$ maybe estimated by:

$$X_c = \frac{I_C + Ii}{I_C + I_i + \lambda I_A} \quad (1)$$

From the samples evaluated during the optimization of μc-Si:H, samples deposited at low-pressure exhibit crystallinity. Figure 3 shows the Raman scattering spectra of the μc-Si:H with crystalline volume fraction of 77 %.

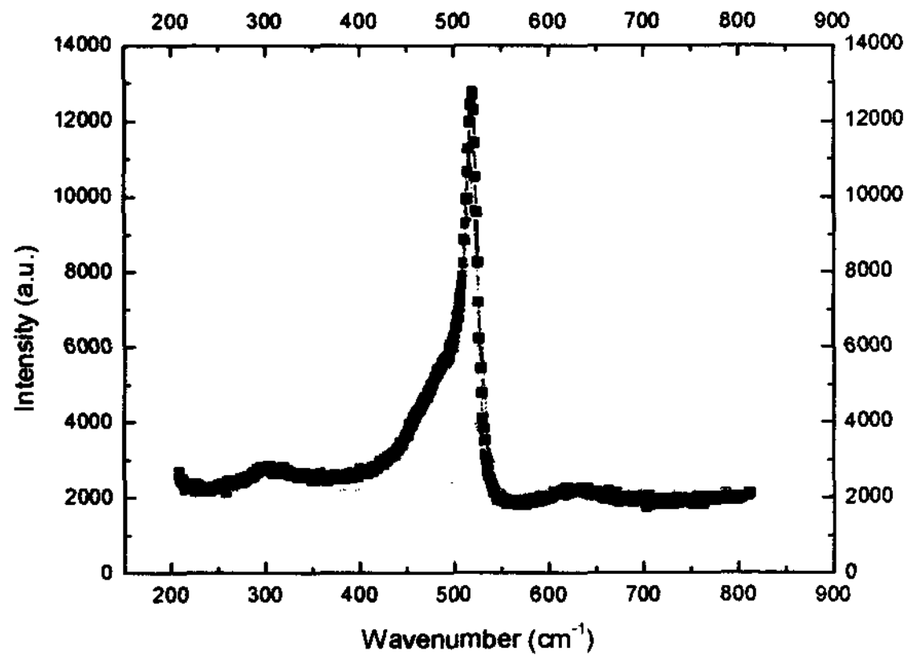


**Figure 3 Raman spectra of a typical film deposited at 80°C, with amorphous peak at 480cm$^{-1}$ and crystalline peak at 520 cm$^{-1}$ (Green line)**

Having determined the optimum condition for low temperature μc-Si:H deposition, a layer-by-layer nitrogenation process, using alternating $N_2$ plasma treatment and μc-Si:H deposition, was used to fabricate TFTs.

The nitrogenation process was performed 4 times, to create the SiN seed layer, before a 200 nm intrinsic μc-Si:H layer and 50 nm n+ μc-Si:H were deposited.

This process was used to deposit films on $SiO_2$ on Corning glass for TFT fabrication.

The gate and drain transfer characteristics for these devices (W/L = 38), are shown in Figure 4 and Figure 5

The highest mobility extracted for these devices was 3 $cm^2V^{-1}s^{-1}$ and the threshold voltage was about 10 V. From the gate and drain transfer characteristics there is little sign of leakage through the gate insulator and the ON/OFF ratio was 4 orders of magnitude.

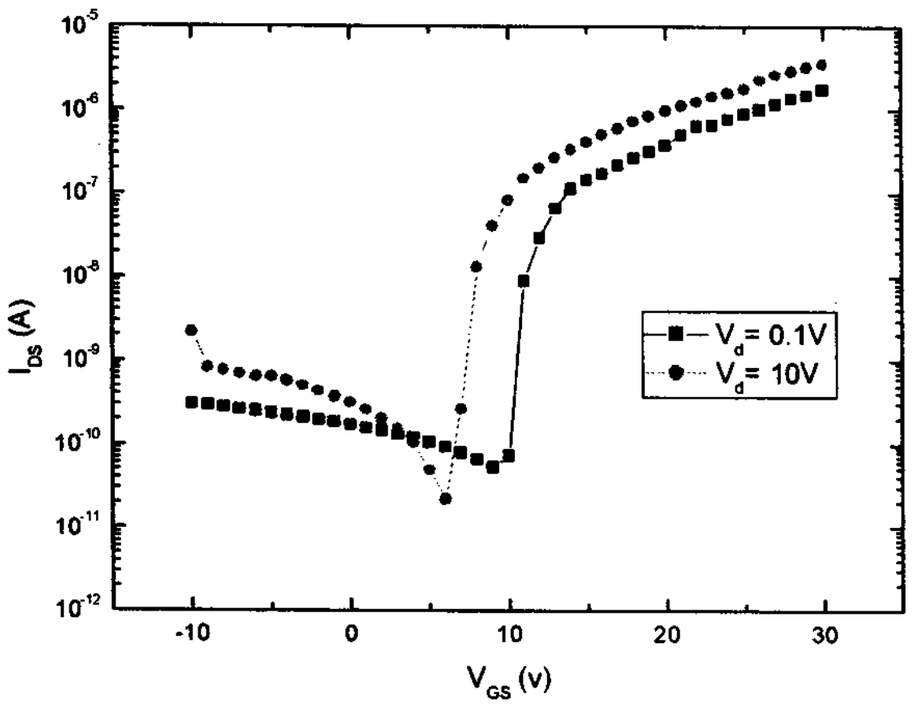


**Figure 4 Gate transfer characteristics for layer-by-layer nitrogenated μc-Si:H TFT**

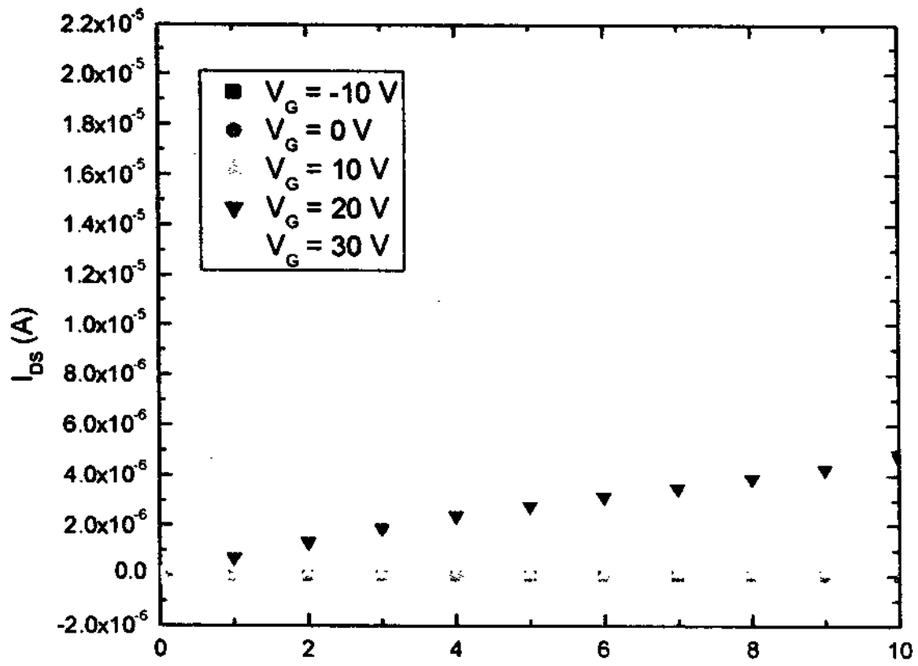


**Figure 5 Drain transfer characteristics for layer-by-layer nitrogenated μc-Si:H TFT**

These results show that low temperature layer-by-layer-nitrogenated μc-Si:H has the potential to be used in bottom-gate TFT applications. The leakage current is about an order higher than in conventional a-Si:H TFTs. This is due to the layer-by-layer nitridation process, which results in a non-optimized interface, and therefore the leakage current and threshold voltage is high. The threshold voltage is also high and this is also due to the interface.

The main advantage of the layer-by-layer-nitrogenated μc-Si:H TFT, is its high mobility when compared with as deposited bottom-gate μc-Si:H TFTs and a-Si:H TFTs. As expected the elimination of the amorphous incubation layer means the accumulation layer can benefit from the crystalline structure at the bottom and therefore enhance the field effect mobility.

## 4. Conclusion

In this paper, we have investigated the effect of nitrogenation on μc-Si:H. A silicon rich silicon nitride layer was produced with a N/Si ratio of 0.6, with most of the crystalline region preserved. The optimized nitrogenation technique was applied to TFT fabrication, which results in TFTs with high mobility. This is achieved using a layer-by-layer deposition technique in which the bottom 70 nm of μc-Si:H are converted into silicon nitride so that, when the device is switched ON, the accumulation layer will form in a region of high crystallinity

## 5. Reference

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