Ultra low temperature polycrystalline silicon thin film transistor using sequential lateral solidification and atomic layer deposition techniques

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Abstract

We present a novel process for the ultra low temperature (<150°C) polycrystalline silicon (ULTPS) TFT for the flexible display applications on the plastic substrate. The sequential lateral solidification (SLS) was used for the crystallization of the amorphous silicon film deposited by rf magnetron sputtering, resulting in high mobility polycrystalline silicon (poly-Si) film. The gate dielectric was composed of thin SiO_2 formed by plasma oxidation and Al_2O_3 deposited by plasma enhanced atomic layer deposition. The breakdown field of gate dielectric on poly-Si film showed above 6.3 MV/cm. Laser activation reduced the source/drain resistance below 200 Ω/□ for n^+ layer and 400 Ω/□ for p^+ layer. The fabricated ULTPS TFT shows excellent performance with mobilities of 114 cm^2/Vs (nMOS) and 42 cm^2/Vs (pMOS), on/off current ratios of 4.20×10^6 (nMOS) and 5.7×10^5 (pMOS).

1. Introduction

Plastic substrate has become an obvious candidate for the flexible display applications. Readily available transparent plastic substrates have generally temperature-resistance up to 200°C. Recent works on low temperature polycrystalline silicon (LTPS) thin film transistor (TFT) have reduced the processing temperature to be compatible with plastic substrate[1].

The interest in the low temperature poly-Si TFT stems from its much higher mobility than a-Si TFT (up to 200 times greater), which enables it to be used for the full integration of both the drive circuits and the pixel TFTs in a monolithic CMOS technology[2]. Because endurable temperature of transparent plastic substrates is up to 200 °C, it is required to reduce the process temperature below 150 °C[3-4].

Eximer laser annealing (ELA) has been used for crystallization for sputtered a-Si films [3-5]. However, sequential lateral solidification (SLS) is the preferred procedure for the formation of high quality poly-Si films[2]. Various attempts to grow high-quality gate oxide has been reported. In CVD using plasma generation, the successful growth of a high quality gate insulator has not yet been reported at ultra-low temperature, below 150 °C[6]

We present technologies for ultra low temperature (<150°C) poly-Si(ULTPS) TFT including SLS crystallization of rf magnetron sputtered a-Si film, high quality gate dielectric film grown by plasma enhanced atomic layer deposition (PEALD) and low sheet resistance by laser activation[9-13].

We also developed ULTPS TFT arrays on flexible plastic substrate. The film stress and overlay accuracy are very important factors to fabricate TFT array on plastic substrate. It was revealed that buffer films as a role of gas barrier and protection of plastic substrate with higher density are more effective in improving the overlay accuracy of plastics.

2. Experiment

We have fabricated ULTPS(below 150°C) TFTs. The SLS was used for the crystallization of the amorphous silicon film deposited by rf magnetron sputtering and the gate dielectric was fabricated by low temperature plasma oxidation followed by PEALD Al_2O_3 deposition[14].

The 80 nm a-Si film was deposited on 1μm SiO_2 buffer/silicon substrate with an rf magnetron sputtering system. Sputtering was performed with a high purity Si target in an argon ambient gas. The background pressure was 1.0×10^{-7} Torr in the sputtering chamber prior to the Si deposition. The target to substrate distance was fixed at 6.4 cm and the substrate holder was maintained at room temperature. The a-Si films were deposited in a

pressure range of 0.65 mTorr~15.5 mTorr argon pressure range by changing gas flow rate and the RF discharge power was 400W.

The sputtered a-Si films were crystallized by XeCl(λ=308nm) excimer laser SLS-200 system (Dukin). The sputtered a-Si films contain Ar gas and this gas affects the film quality during the laser annealing process.

After active layer patterning, the Al_2O_3 films for gate dielectric were deposited by using PEALD technique. Al_2O_3 is one of the most promising SiO_2 replacement materials for the gate dielectric material of low temperature poly-Si TFTs. S. Higashi et al. had improved the SiO_2/Si interface quality using oxygen plasma treatment which successfully terminated the trap states in the poly-Si films[13].

To obtain high quality gate dielectric film, we formed 5 nm SiO_2 using O_2 plasma treatment on the surface of poly-Si film and then deposit 65 nm Al_2O_3 film containing nitrogen (< 1 %) by PEALD at the temperature of 150°C. The precursors of Al, O, and N are trimethylaluminum, O_2, and N_2 respectively.

Following the gate dielectric formation, Cr gate electrode of 200 nm was formed by DC sputtering at room temperature. After the patterning of the gate electrode, the n+ and p+ source and drain (S/D) regions were formed by ion shower doping using PH_3/4keV and B_2H_6/10keV. The laser activation is necessary for ultra low temperature process. With laser energy 312 mJ/cm^2, we obtain the S/D sheet resistance below 200 Ω/□ for n+ S/D and 400 Ω/□ for p+ S/D. Finally the contact hole opening was followed by 300 nm Al formation.

We also developed ULTPS TFT arrays on flexible plastic substrate. Polyethersulfone (PES) was used for flexible substrate and PES substrates were laminated on glass substrate before TFT process. The glass transition temperature of PES is 225°C and PES substrate has been recommended to be used at a temperature lower than 200°C. The thermal expansion coefficient of PES is 45-55 ppm/K and the thermal shrinkage of PES has known to be as high as 100 ppm when it is treated at 200 °C for 1h[8]. So, the overlay accuracy is very important to fabricate TFT array on PES substrate. It was revealed that the gas-barrier film with higher density are more effective in improving the overlay accuracy of plastics.

3. Result and Discussion

Figure 1 shows the Ar content within the a-Si film and the maximum laser energy density over which the a-Si film is damaged by explosive Ar gas effusion. Although increasing the working gas pressure decreases the Ar content within the a-Si film, the a-Si film grown at 2.7 mTorr shows the highest resistance upon damage with 792 mJ/cm^2. The films prepared at low pressure exhibit little surface morphology and a densely packed structure that is indicative of a zone T dense structure. The most resistant a-Si film for Ar gas effusion damage may be determined by competition between the film density and the argon gas concentration.

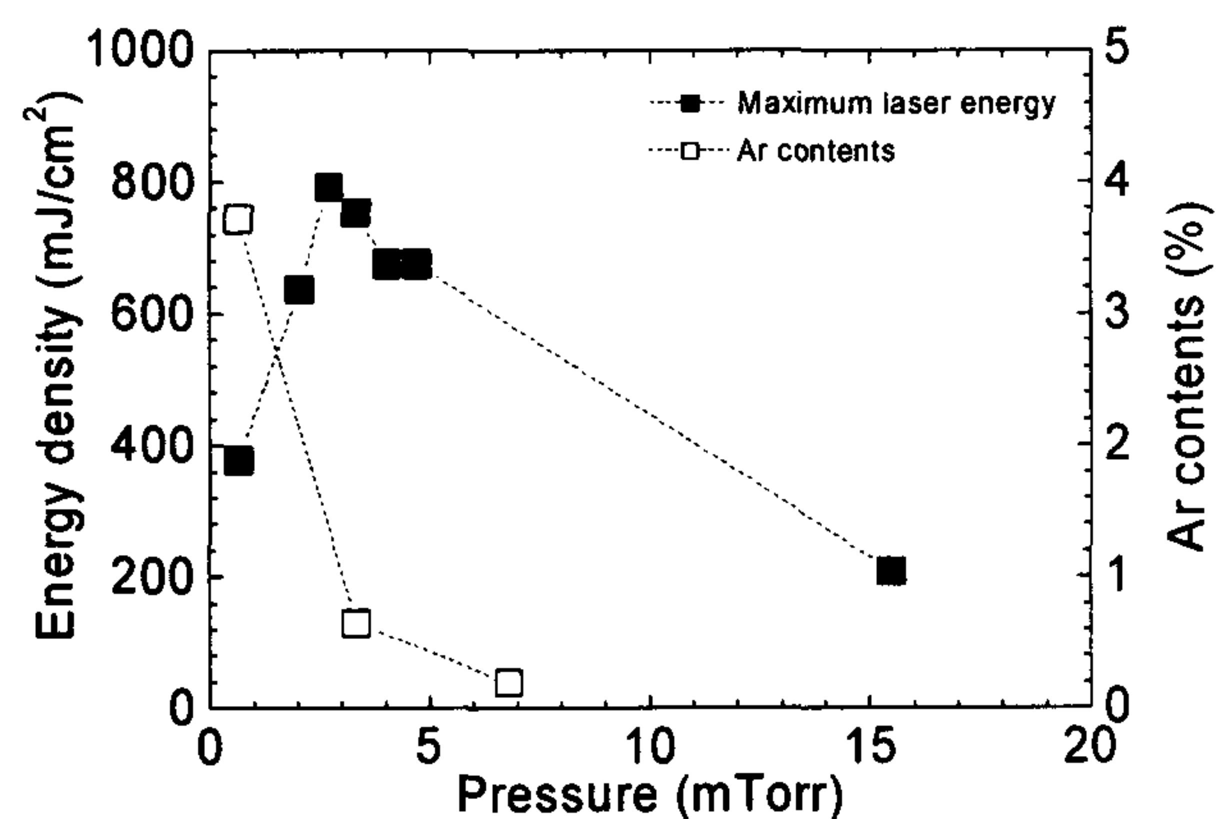

Figure 1. The Ar content within the a-Si film and the maximum laser energy density over which the a-Si film is damaged by explosive Ar gas effusion with pressure variation.

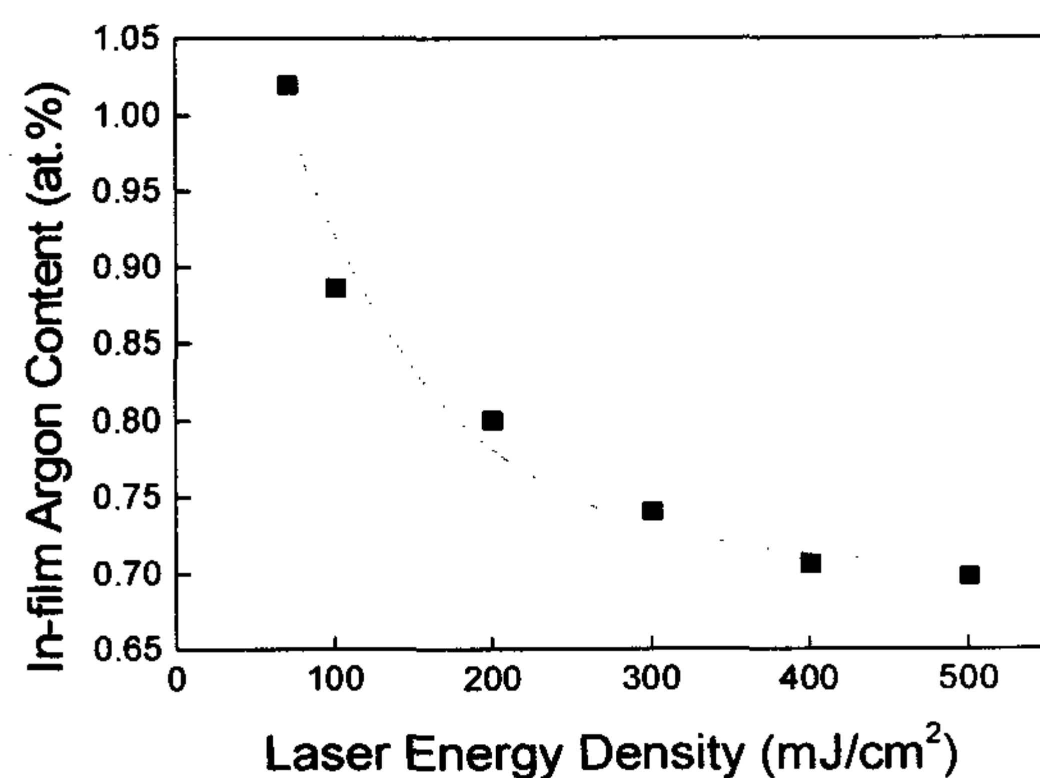

Figure 2. The Ar content within the a-Si film as the consecutive laser annealing.

Figure 2 shows the Ar content within the a-Si film as the consecutive laser annealing. The argon content in

the a-Si film analyzed by Rutherford Backscattering Scattering (RBS) is reduced from 1.0 % to 0.7 % by consecutive laser annealing from 70 mJ/cm^2 to 500 mJ/cm^2. Figure 3 shows the plan-view SEM micrographs of (a) 1 shot and (b) multi-shot SLS crystallized poly-Si film of sputter deposited amorphous film. As shown in figure, crystallized poly-Si film is composed of multi grain both in lateral and in vertical direction.

The poly-Si film with 80nm thickness is obtained by SLS crystallization at 550 mJ/cm^2 after first step laser annealing at 336 mJ/cm^2.

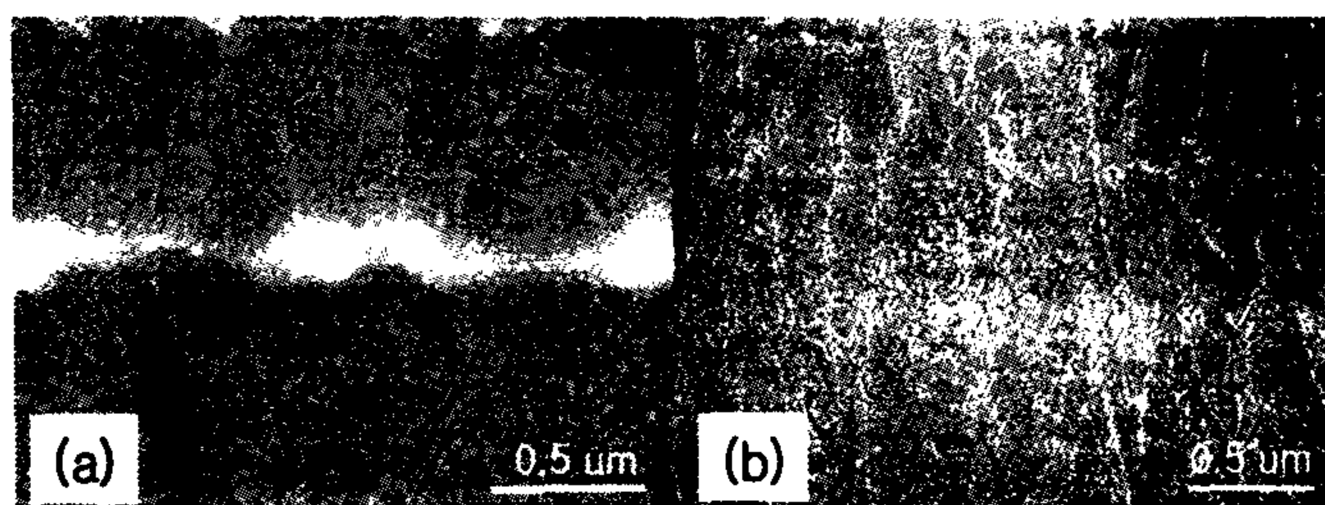

Figure 3. The plan-view SEM micrographs of (a) 1 shot and (b) multi-shot SLS crystallized poly-Si films of sputter deposited amorphous films.

Al_2O_3 film deposited by PEALD is a promising gate dielectric for the fabrication of TFTs on a plastic substrate[6-8]. The film can be deposited at a temperature lower than 150°C showed excellent electrical properties such as low leakage current and high dielectric constant. In the PEALD process of oxide films, oxygen radicals and ions are used as the oxidants and resultantly it is possible to enhance the reactivity of reactant gas.

Etch rates of Al_2O_3 films grown by PEALD were investigated and compared to ALD without plasma enhancement. The etch rate is a good measure of film density. 1.2-1.3 % HF solution was used as the etchant in performing etching process of Al_2O_3 films. Figure 4 shows etch rates of arbitrary unit for Al_2O_3 samples in the temperature range of 100-300°C. Etch rate of ALD Al_2O_3 films more rapidly increases compared to nitrogen added PEALD Al_2O_3 films indicating that severe degradation of film density for ALD Al_2O_3 films occurs as the growth temperature decreases[7].

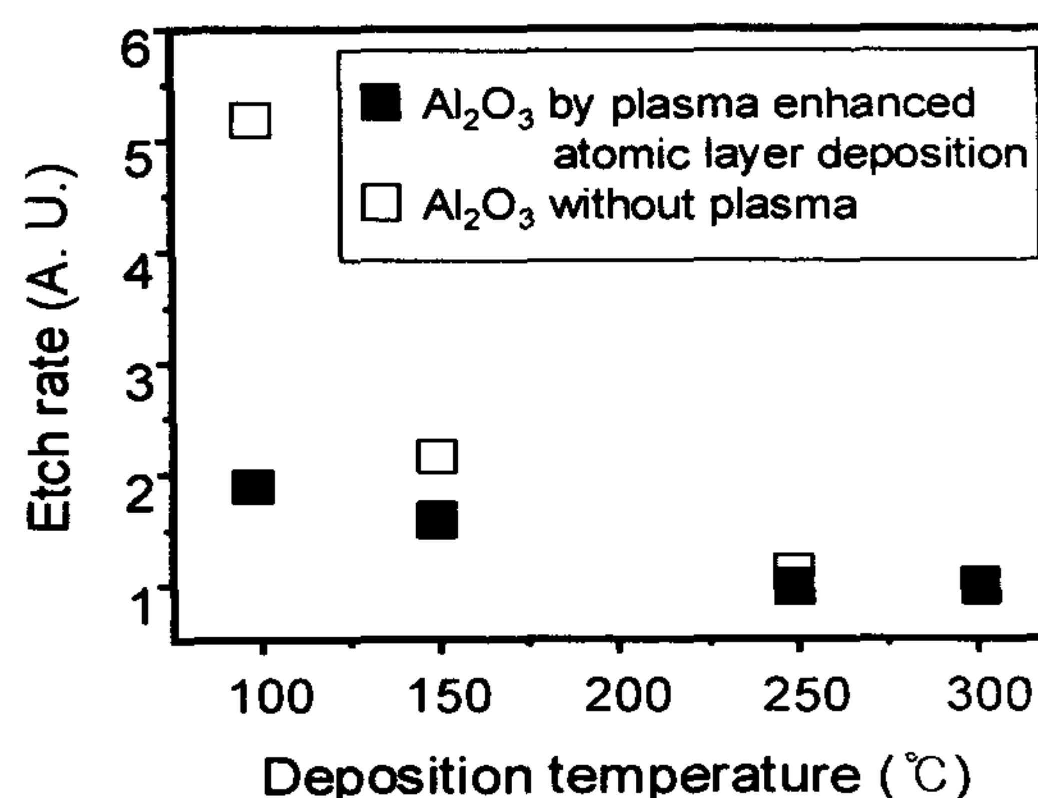

Figure 4. Etch rates of PEALD and ALD process for Al_2O_3 films obtained from the optical thickness measurements before and after etching the samples with HF solution.

Figure 5 shows the leakage current of the gate dielectric on poly-Si film at 200×100 μm^2 pattern and the breakdown field is above 6.3 MV/cm. The roughness of poly-Si film may reduce the breakdown field from 9 MV/cm, which is the measured value at crystalline silicon substrate[7].

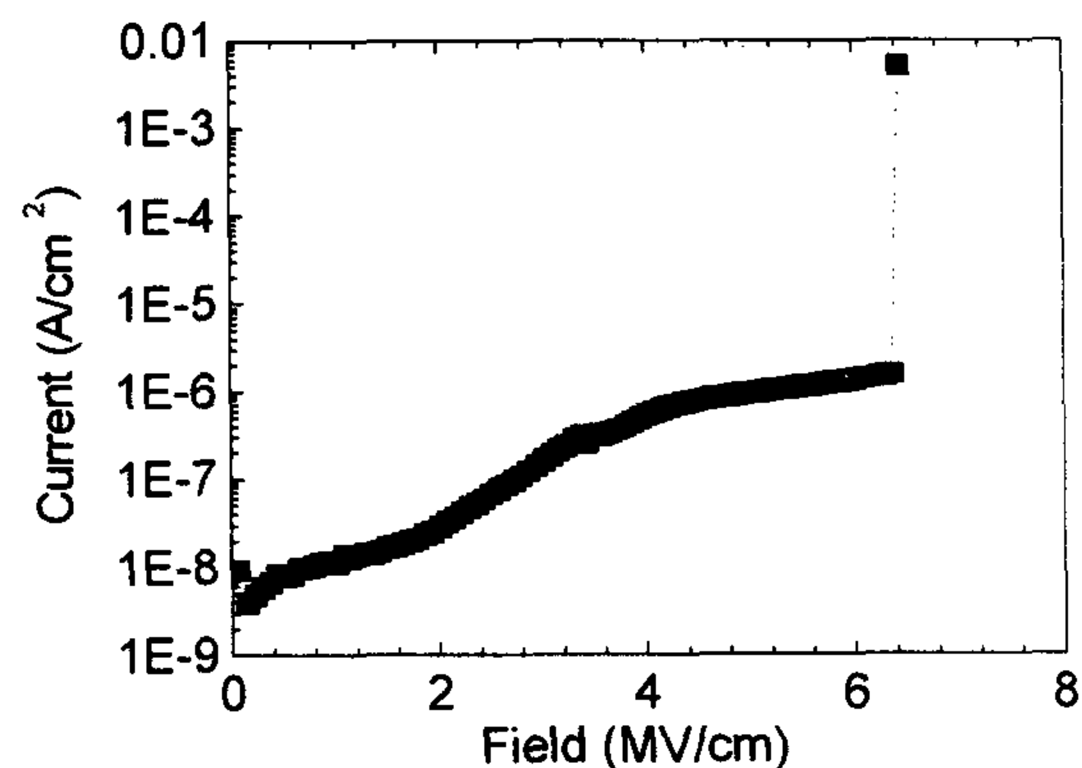

Figure 5. Leakage current of the gate dielectric on poly-Si film at 200×100 μm^2 pattern.

Figure 6 shows (a) the nMOS and (b) the pMOS transfer characteristics and (c) the nMOS and (d) pMOS output characteristics. The ULTPS TFT with W/L=30μm/30μm shows excellent performance with on/off current ratios of 4.20×10^6 (nMOS) and 5.7×10^5 (pMOS), high mobilities of 114 cm^2/Vs (nMOS) and 42 cm^2/Vs (pMOS), small V_{th} of 2.6 V (nMOS) and -3.7 V (pMOS), and swings of 0.73 V/dec (nMOS) and 0.83 V/dec (pMOS).

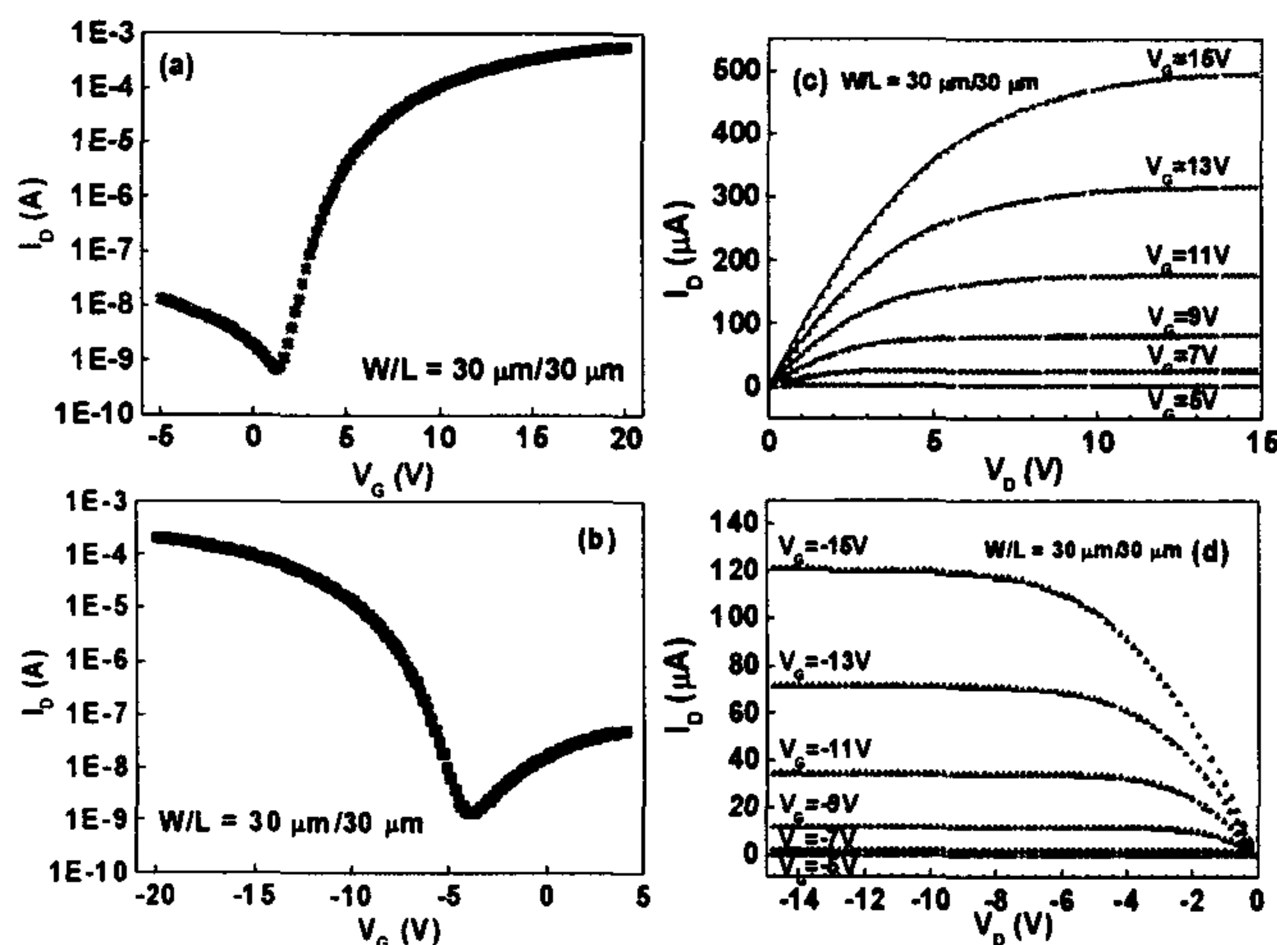

Figure 6. Transfer characteristics of (a) nMOS and (b) pMOS. Output characteristics of (c) nMOS and (d) pMOS. Channel length and width are 30 µm and 30µm.

It was revealed that the gas-barrier films with higher density were more effective in improving the overlay accuracy of plastics. We obtained a overlay tolerance within 5 µm in fabricating 2 inch TFT arrays on PES substrate, as shown in Figure 7 and Figure 8..

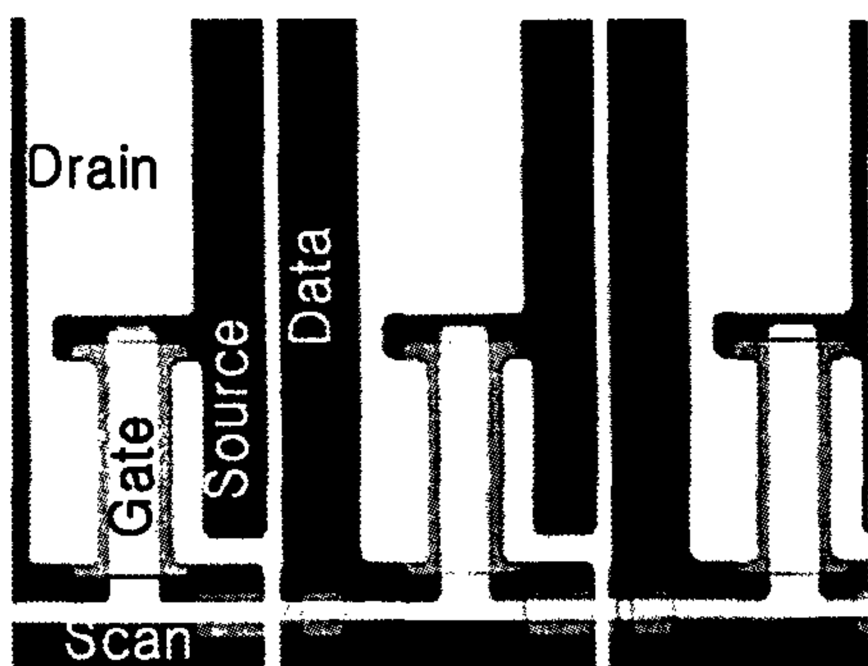

Figure 7. Layout of Poly-Si TFT array on plastic substrate.

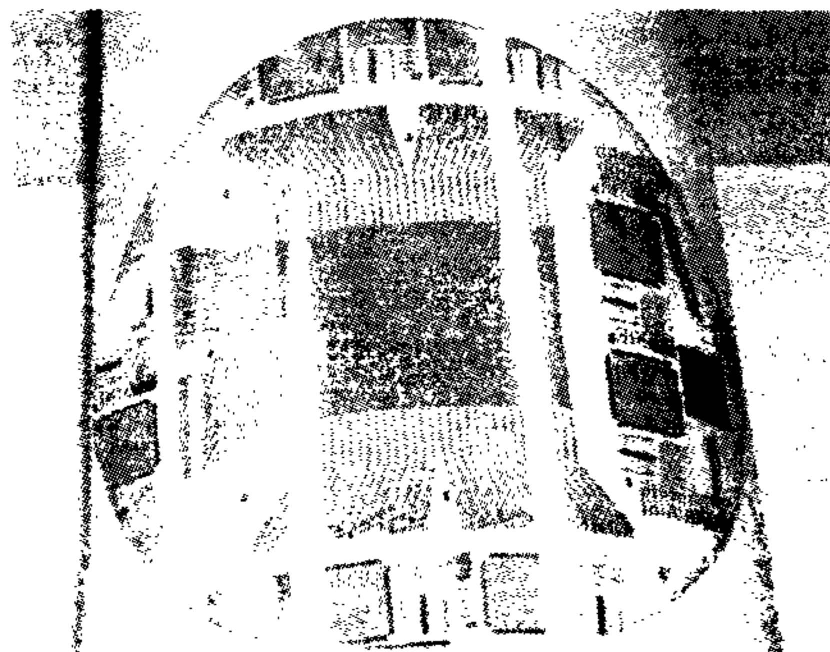

Figure 8. Poly-Si TFT Array on Plastic Substrate.

4. Conclusion

We have successfully fabricated ultra-low temperature poly-Si TFT using SLS and PEALD processes for plastic substrate. The maximum process temperature was below 150℃. Al_2O_3 film deposited by PEALD is a promising gate dielectric for the fabrication of TFTs on a plastic substrate. The breakdown field was above 6.3 MV/cm. Laser activation reduced the S/D resistance below 200 Ω/□ for the n+ layer and 400 Ω/□ for the p+ layer. The ULTPS TFT with W/L=30µm/30µm showed excellent performance with on/off current ratios of 4.20×10^6 (nMOS) and 5.7×10^5 (pMOS), high mobilities of 114 cm^2/Vs (nMOS) and 42 cm^2/Vs (pMOS). By applying this TFT process on PES substrate, we knew that this process would be suitable for flexible display on plastic substrate.

5. Acknowledgements

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6. References

[1] S. D. Brotherton, J. R. Ayres, M. J. Edwards, C. A. Fisher, C. Glaister, J. P. Gowers, D. J. McCullock, M.Trainor, Thin Solid Films **337**, 188 (1999).

[2] A. T. Voutsas, Appl. Surf. Sci., **9602**, 1 (2003).

[3] M. J. Lee, C. P. Judge, S. W. Wright, Solid State Electron **44**, 1431 (2000).

[4] D. P. Gosain, T. Noguchi, and S. Usui, Jpn. J. Appl. Phys. Part 2 **39**, L179 (2000).

[5] T. Serikawa and F. Omata, Jpn. J. Appl. Phys. Part 2 **39**, L393 (2000).

[6] J.W.Lim, S.J.Yun, Y.H.Kim, C.Y.Shon, J.H.Lee, Electrochemical & Solid-State Letters, 7(9) (2004).

[7] J.W.Lim, S.J.Yun, Electrochemical and Solid-State Letters, **7**, F45 (2004).

[8] S.J.Yun, J.W.Lim, J.H.Lee, Electrochemical and Solid-State Letters, **7**, C13 (2004).

[9] M. A. Crowder, M. Moriguchi, Y. Mitani, A. T. Voutsas, Thin Solid Films **427**, 101 (2003).

[10] D. P. Gosain, J. Westwater, and S. Usui, AMLCD 1997 Digest, pp. 51-54.

[11] T. Unagami, A. Lousa, and R. Messier, Jpn. J. Appl. Phys. Part 2 **36**, L737 (1997).

[12] D.W.Hoffman, J. Vac. Sci. Tech. A**12**, 953 (1994).

[13] S. Higashi, D. Abe, Y. Hiroshima, K. Miyashita, T. Kawamura, S. Inoue, and T. Shimoda, Jpn. J. Appl. Phys. Part 1 **41**, 3646 (2002).

[14] Y.H.Kim, C.Y.Sohn, J.W.Lim, S.J.Yun, C.S. Hwang, C.H.Chung, Y.W.Ko, J.H.Lee, IEEE Electron Device Letter (2004) In Pressing