Compensation of Addressing Time at High Temperature in ac PDP.

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Abstract

Misfiring is often observed during the high temperature quality assurance test of plasma display panel. This limits the productivity of PDP industry. In this paper, experimental observations on the misfiring at high panel temperature have been performed through time dependent discharge light output and static margin measurement. For the high temperature condition, firing voltage increment is found in both surface and facing discharges. This in turn increases time lag in address discharge, and results in increment of misfiring probability. In order to reduce this kind of misfiring, a new method that applies automatically different slope of ramp erasing pulse on the common electrode according to temperature variation is proposed. The experimental results show that controlling the slope of ramp erasing pulse is quite effective for compensating temperature-dependent variation of reset and address discharge.

1. Introduction

AC PDPs have recently achieved good performance and their image quality can now compete with that of cathode ray tubes (CRTs). However, improvement of luminous efficiency, image quality, and cost-reduction is still necessary to compete with other candidates (LCD, OLED, and Projection TV, etc.)[1]. On the practical point of view, production yield becomes one of prime concern. Large driving margin or good discharge stability is required for yield improvement, which means unwanted misfiring or non-firing should never occur under wide variety of graphic signal input and operating circumstances. For the PDP driven with ADS (Address-Display period Separated) scheme, however, misfiring of small number of cells is often observed during the high temperature QA (quality assurance) test. These temperature-dependent misfiring problems should be overcome to improve yield and productivity. In spite of the importance of the issue, there are very limited reports concerning the effects of panel temperature on the driving characteristics of PDP.

In this paper, we report experimental observations on the high temperature misfiring in ADS driving scheme. In order to reduce the probability of the misfiring at high temperature, a new method that applies automatically different slope of ramp erasing pulse on the common electrode according to environmental temperature variation is suggested. Effectiveness of the proposed method is verified by various output light measurements.

2. Experimental

Fig. 1 shows the driving waveform used in this study. The reset-up and down times of each subfield are 100 μs and 150 μs, respectively, in the reset period. The width of scanning pulses generated by the scan driver IC is designed as 3 μs which has a similar pulse width to the conventional 42 inch ac PDP. Each address period of eight subfields is designed to be about 1 ms. In measuring static characteristics simple square pulse wave was applied.

The discharge light waveform is obtained by a photo-diode (C5460, Hamamatsu Co.) The discharge current waveform can be estimated from the light waveform of a cell because the similarities between a discharge current waveform and an emitting light waveform were known [2], [7]. The addressing time, which is defined by the sum of discharge time-lag and current-duration, is measured by a digital storage oscilloscope (LT354, Lecroy Co.). The color spectrum of discharge cells is detected by a spectroradiometer (CS-1000, Minolta Co.). Homemade thermal chamber was used to control ambient temperature. To avoid influence of ambient temperature on the electronic circuits, all electronics was positioned outside of the thermal bath.

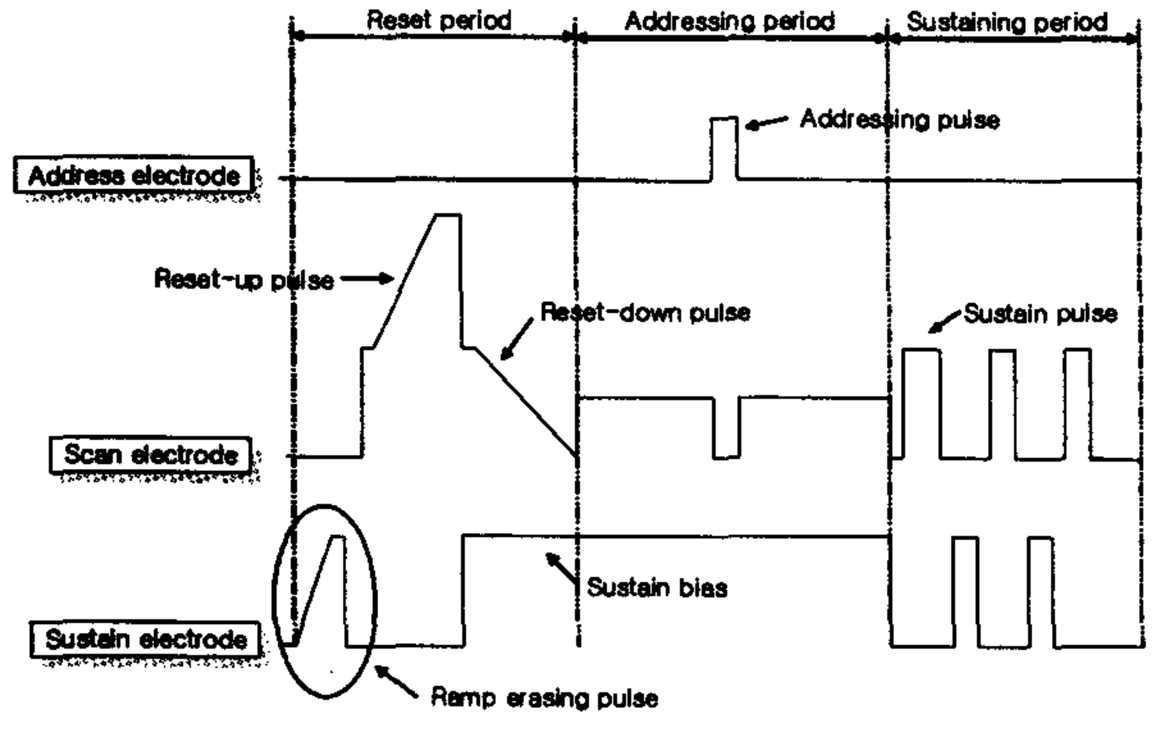


Fig. 1 Schematic diagram of driving waveform.

3. Influence of panel temperature on the static characteristics of the panel

Before analyzing high-temperature misfiring in real ADS driving scheme, firing and sustain voltage measurements have been performed. Fig. 2 compares the static characteristics of test panel at high temperature (80 ℃) condition with that of the room temperature case. Apart from the influence of panel temperature, driving frequency also affects firing characteristics. In ac discharge, wall voltage transfer characteristics and priming from former discharge during transient state are important to achieve fully developed stable discharge. As the pulse frequency increases the probability of complete wall charge transfer decreases and the relative priming level increases at the just before applying the next pulse. The competition between these two factors probably results in frequency-dependent firing voltage characteristics as shown in the figure. Firing voltage for high temperature panel shows higher value. Basically, secondary electron emission coefficient γ of MgO layer and ionization coefficient α is the most important factors that determine breakdown voltage. Although a complete analysis on the origin of V_f differences according to panel temperature is not available at present and beyond the scope of this work, we speculate that α and γ are not so much affected by temperature variation with in our experimental conditions. Since number density of particles inside the panel is conserved in spite of temperature variation and the electron temperature is quite higher than neutral temperature, ionization process is hardly affected by temperature variation of about 50K. An interesting point is that V_f differences become larger at low frequency regime where wall charge transfer is more important to maintain stable steady state pulse discharge. This result suggests that apparent wall charge transfer is less effective in high temperature conditions.

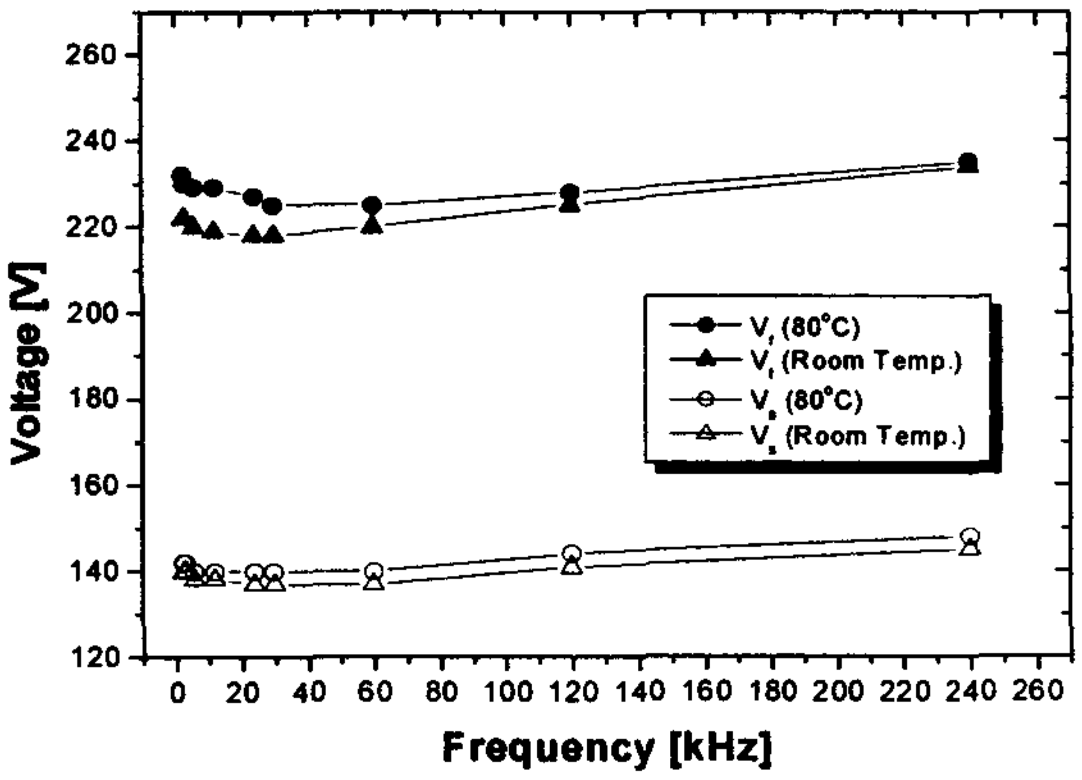
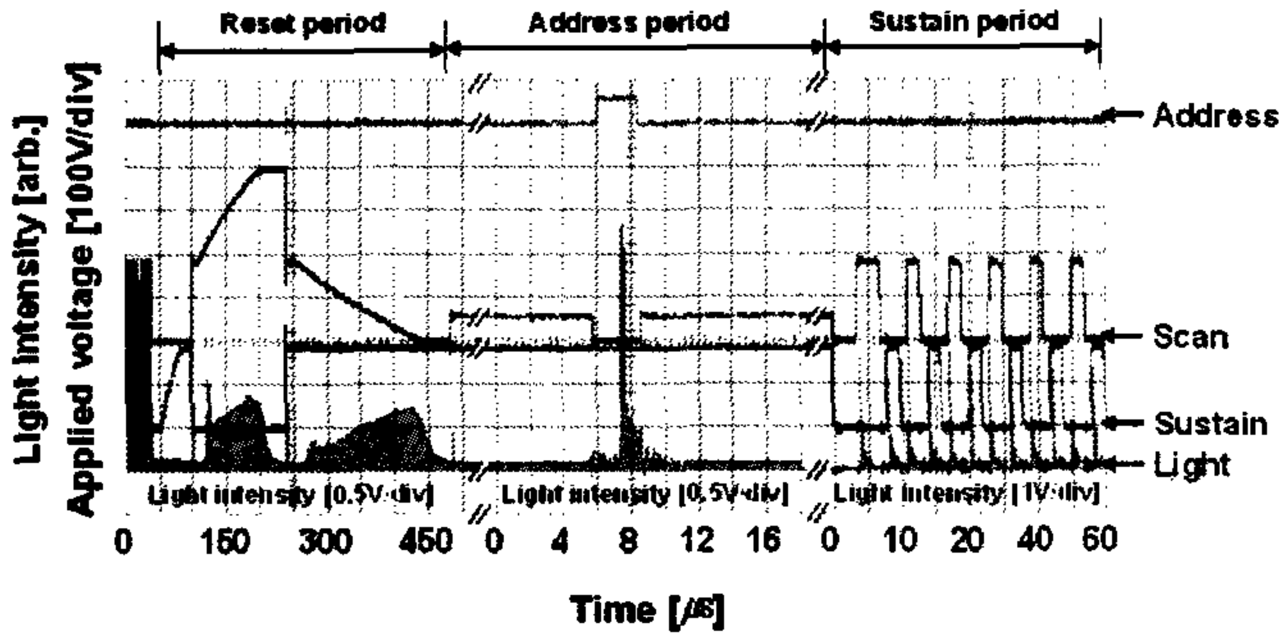


Fig. 1 Static characteristics of test panel at room temperature and 80℃.

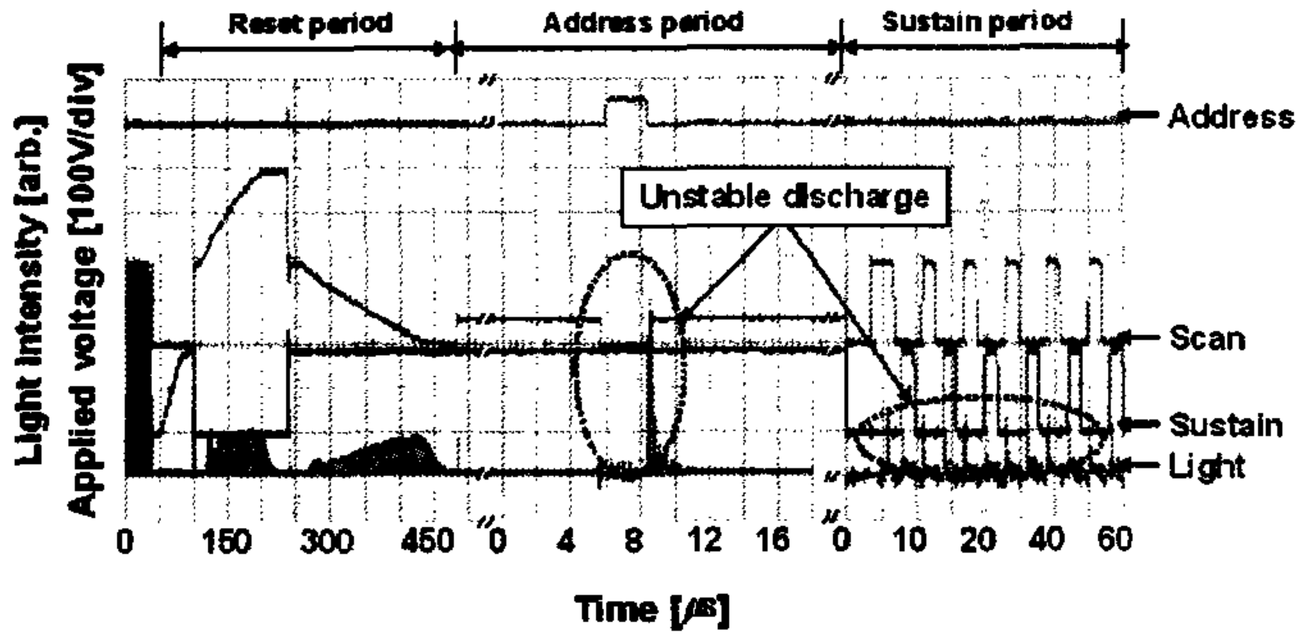
4 Observation of high temperature misfiring in ADS driving scheme

As a driving method of ac PDP, address-display separated (ADS) scheme [4], [5] has been widely used. In ADS method, a picture of one frame is divided into eight sub-fields where each sub-field has reset, address and sustain periods as shown in Fig. 1[6]. Each sub-field has different number of sustain pulses that realize different luminance of each sub-field. In the reset period, the wall charges are uniformly accumulated on dielectric layer of all cells by applying the ramp rising pulse on the scan electrode (reset-up pulse) regardless of the wall charge condition of previous sub-field. The charges are then properly erased by applying the ramp falling pulse on the scan electrode (reset-down pulse). However, the accumulated charges on the dielectric layer of address electrode are nearly constant because the surface discharge occurs nearly by applying the reset-down pulse for the distribution of wall charge. As a result, the surface condition of all cells becomes uniform in the reset period. The role of address period is to accumulate new wall charges on the dielectric layer of selective cells by applying the addressing pulse between scan electrode and address electrode. The addressing is helped by the accumulated wall charges on the address electrode. A sustain bias (blocking voltage) should be applied to the sustain electrode during addressing to assist in forming the wall charges. The role of sustain period is to make an image on the panel by applying the ac sustaining pulses to all display electrodes. The selected cells, which are accumulated in address period, are picked up by the first sustaining pulse and then a discharge with sufficient wall charges is sustained by the following sustaining pulses to display.

The image quality of ac plasma display panels (PDPs) is directly correlated with the misfiring of discharge in the sustaining period. The misfiring occurs more frequently at high temperature. In the driving point of view, the cause of misfiring at high temperature mainly comes from the failure of addressing which closely correlates with discharges of sustain and reset periods in the ADS driving scheme [3]. Fig. 3(a) shows normal discharge light waveforms of a subfield for one discharge cell at room temperature. When ambient temperature increases up to 80 ℃, a light intensity of the reset period is reduced and the addressing and the sustaining waveforms become unstable as shown in Fig. 3(b), that is, the flicker of discharging cell occurs with high temperature. Especially, the misfiring at the high temperature occurs more frequently in the green discharge cell. In order to reduce misfiring probability at high temperature, the ramp voltages, the slope rate of ramp pulses, the addressing voltage, the sustain bias voltage, the sustaining voltage, etc. can be modified. However, these methods are practically difficult to apply because the ambient temperature of panels varies for a situation and a season. Therefore, simple and cost-effective self-adjusted driving is needed.



(a) Normal discharge light waveform at a room temperature



(b) Discharge light waveform of misfiring at a high temperature

Fig. 3 Discharge light waveforms at different temperatures.

5 Reset and address characteristics influence by ambient temperature

In this chapter, more detail observations on the temperature effects is presented. Fig. 4 shows the light waveforms of discharge cells for both room temperature and 80 ℃ in the reset period. The discharge light waveform of 80 ℃ is weaker and more delayed than that of room temperature. These reset characteristics in turn affects the discharge characteristic of the address period. Fig. 5 shows the dispersions of addressing discharges. The addressing light waveforms are accumulated during discharge of 500 times. The time of addressing dispersion, 1.3 μs, is increased up to 2.2 μs with increasing temperature up to 80℃. Especially, the delay of the addressing time occurs mostly in the discharge cells with green phosphor. This is probably due to the facing discharge characteristics of green phosphor. Fig. 6 shows the static characteristics of the discharge cells for the facing discharge. The firing and the sustain voltages of the green cell are higher about 20 [V] than those of the other cells, that is, the addressing voltage of the green cell is higher than that of the other cells.

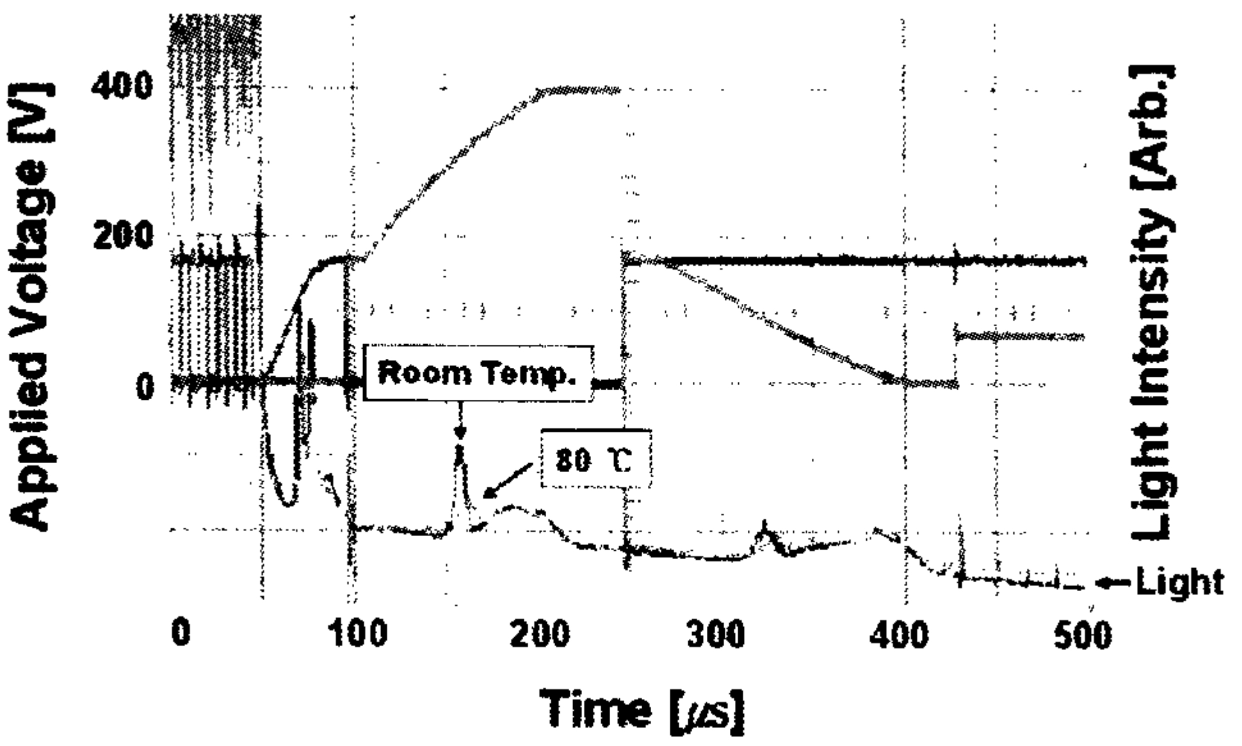
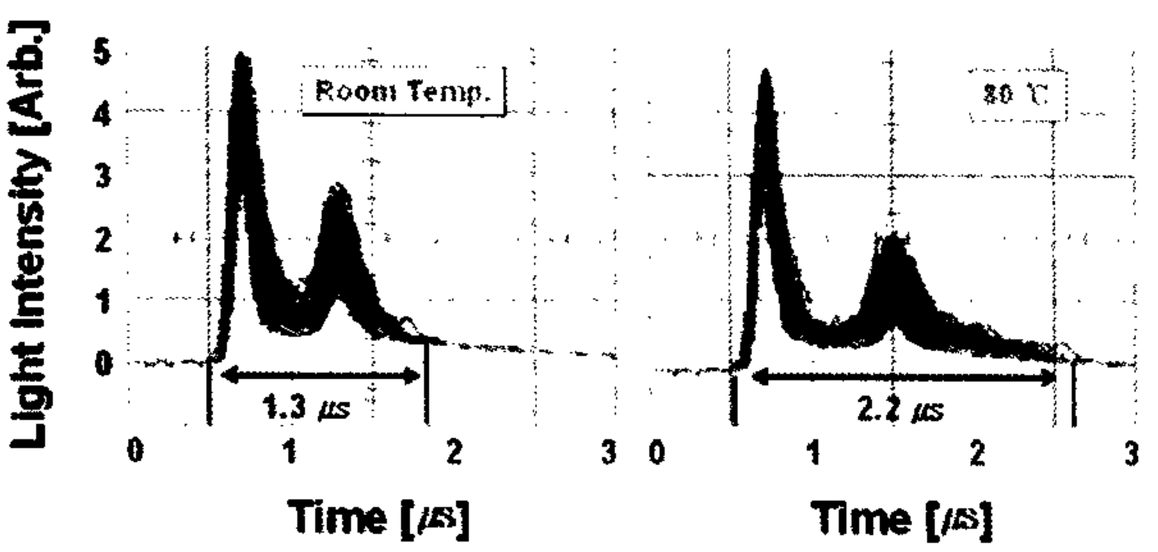


Fig. 4 Light waveforms of discharge cells at room and high temperatures.



(a) Room temperature (b) 80℃

Fig. 5 Addressing dispersions of discharge cells (a) at a room temperature and (b) at 80℃

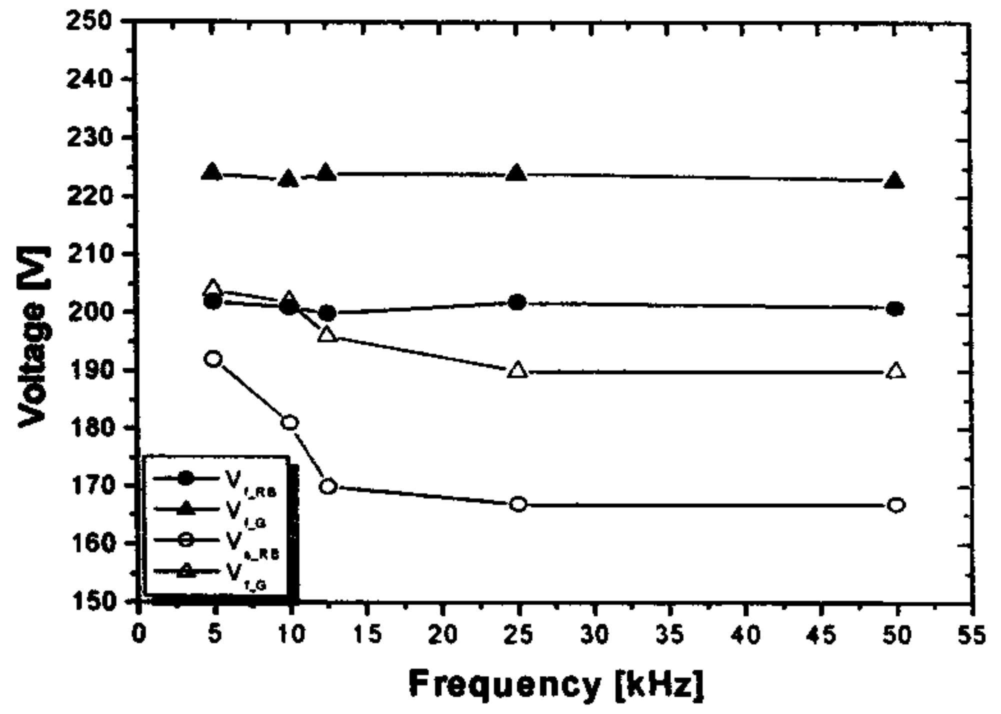


Fig. 6 Static characteristics of discharge cells with different phosphor as a function of frequency for the facing discharge.

The role of the ramp rising pulse on the common electrode at the end of sustain period (ramp erasing pulse) is to erase wall charges on the dielectric layer of a discharged cell in the previous subfield. The wall charge state created by the ramp erasing pulse has influence on the discharge characteristics of a next reset-up pulse. Fig. 7 shows the discharge light waveforms of reset-up pulse for varying slope rates of the ramp erasing pulse. As the slope of the ramp erasing pulse increases the discharge firing time of the reset-up pulse decreases since higher slope induces stronger erase discharge and accumulate relatively higher positive wall charge in sustain electrode. Consequently, the wall charges on the address electrode can be controlled by the slope of ramp erasing pulse. The controllability is presented in Fig. 8. It shows the relationships between the slope rate of the ramp erasing pulse and the time of addressing dispersion. The time of addressing dispersion decreases as a function of the slope rate of the ramp erasing pulse.

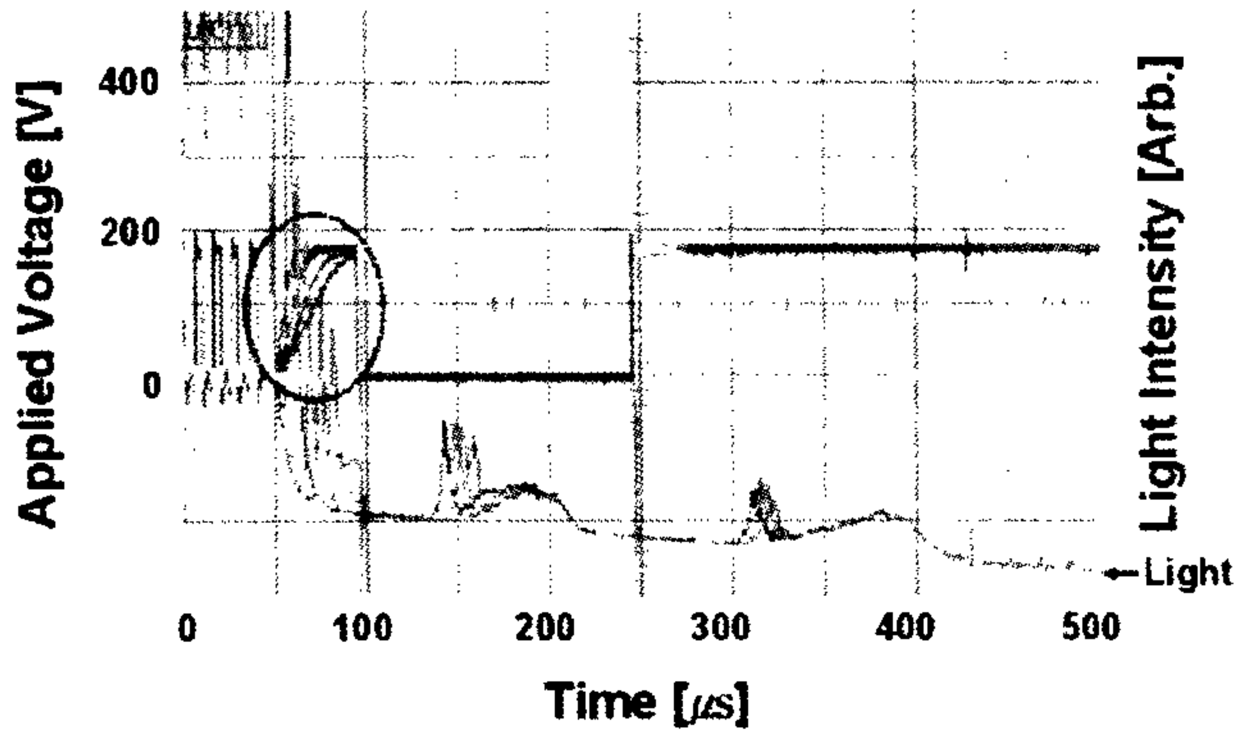


Fig. 7 Discharge light waveforms of reset-up pulse for various slope rates of the ramp erasing pulse at room temperature.

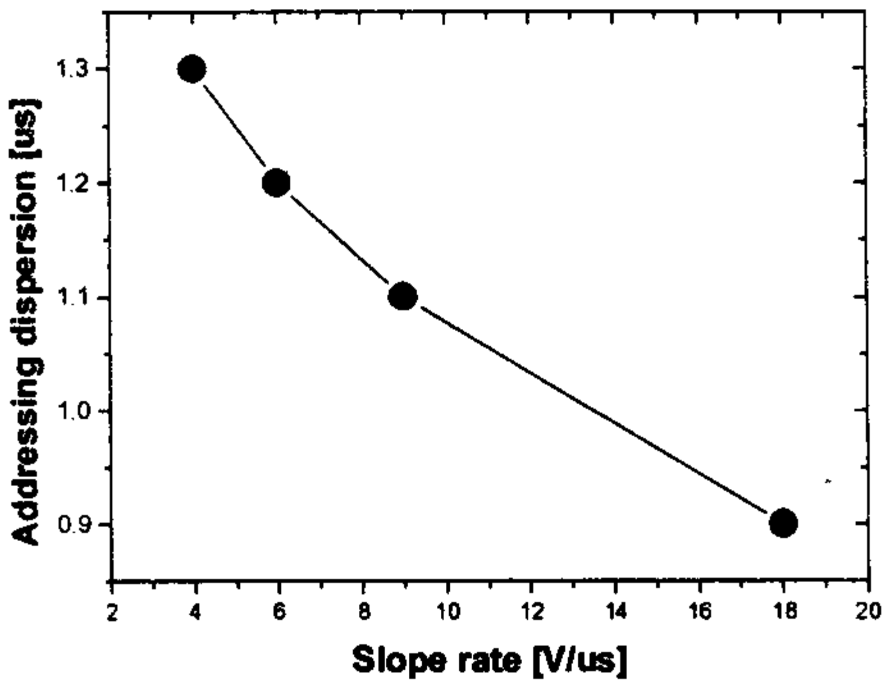
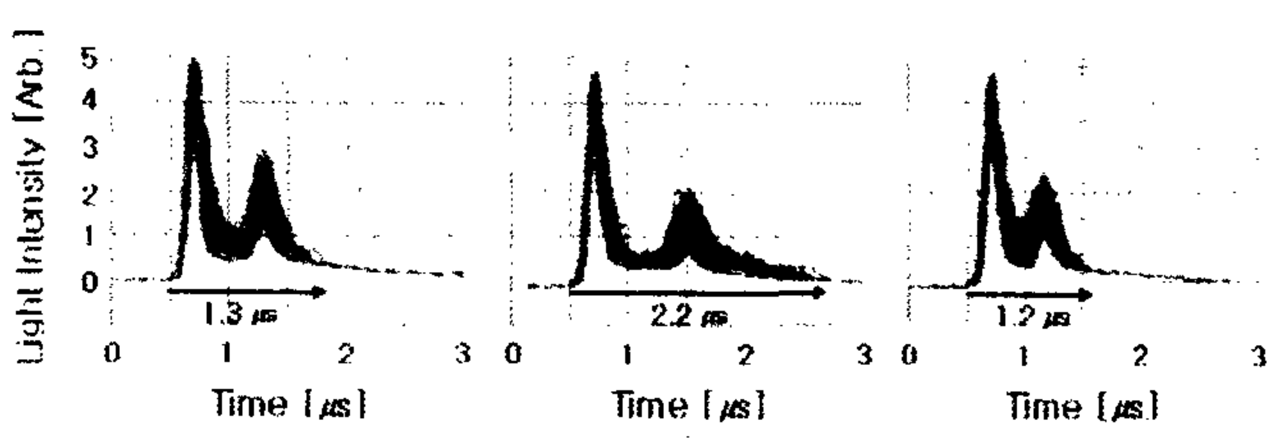


Fig. 8 Relationships between the slope of the ramp erasing pulse and the time of addressing dispersion.

Fig. 9 shows the addressing light waveforms of discharge cells for different temperatures and different slope rates of the ramp erasing pulse. The time of addressing dispersion, 1.3 µs, after applying a ramp erasing pulse of 6 V/µs at room temperature [Fig. 9 (a)] increases up to 2.2 µs with increasing temperature up to 80℃ [Fig. 9 (b)] and then the time of addressing dispersion decreases from 2.2 to 1.2 µs after applying a ramp erasing pulse of 18 V/µs at 80℃ [Fig. 9(c)]. Fig. 10 shows the variation of spectrum intensities for the case of Fig. 9. The spectrum intensity, 41 %, with applying a ramp erasing pulse of 6 V/µs at room temperature [Fig. 10(a)] decreases to 37 % with increasing temperature up to 80℃ [Fig. 10(b)] and then the intensity recovers up to 40 % after applying a ramp erasing pulse of 18 V/µs at 80℃ [Fig. 10(c)]. Intensity decrease in green color comes from unstable, flickering of green cells. The flicker phenomenon of addressed cells with the green phosphor disappears by applying a ramp erasing pulse of 18 V/µs at 80℃.



(a) 6 [V/µs] at room temp. (b) 6 [V/µs] at 80 ℃ (c) 18 [V/µs] at 80 ℃

Fig. 9 Addressing light waveforms of discharge cells for different temperatures and different slope rates of ramp erasing pulse.

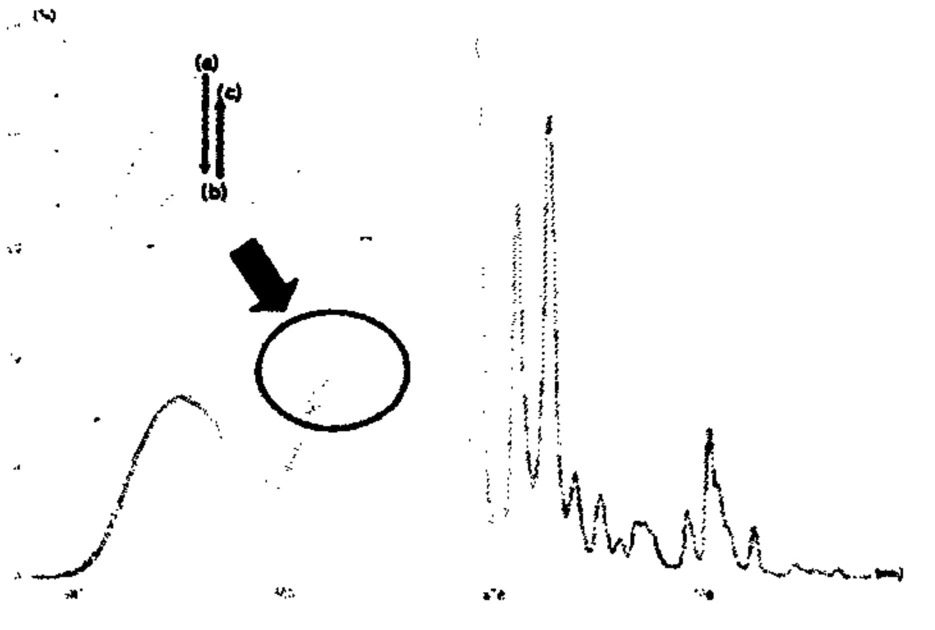
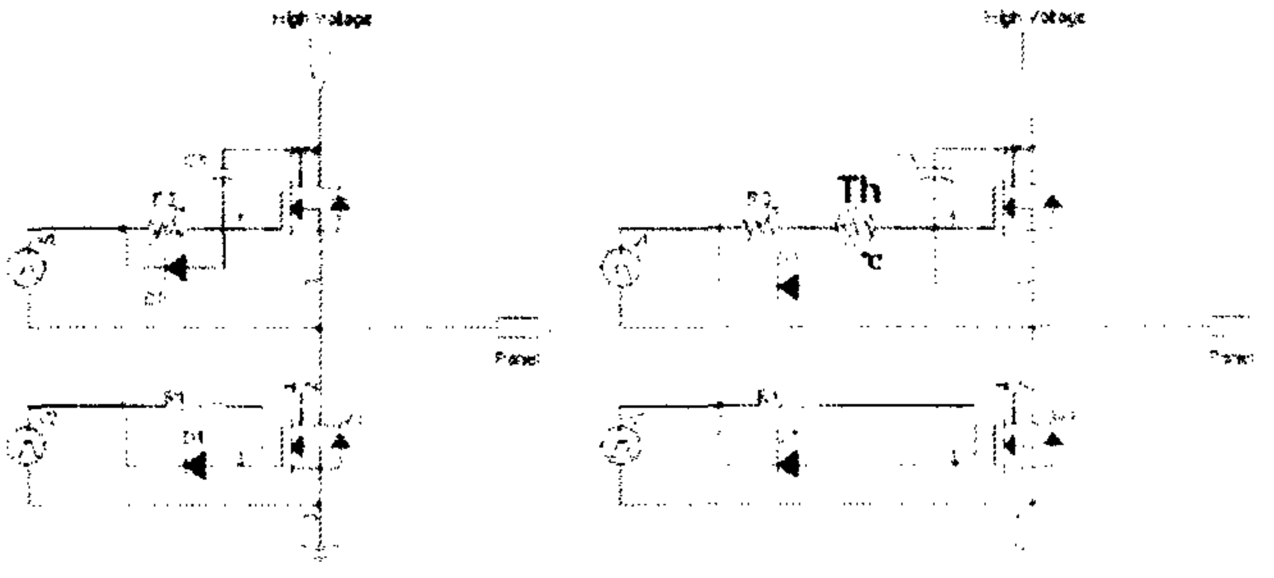


Fig. 10 Variation of spectrum intensities for the case of Fig. 9.

6 Driving method to compensate the high temperature misfiring

Fig. 11(a) shows the schematic diagram of a voltage-controlled ramp (VCR) waveform generator which has been used widely [8]. The ramp waveform with a constant slope can be generated by this circuit. In this case, the slope can be controlled by the resistor on n-channel FET gate and capacitor between the drain and the gate. Fig. 11(b) shows the schematic diagram of a suggested waveform generator. In this case, the slope can be controlled by the resistor and the thermistor whose resistance is varied with temperature.

Fig. 12 shows the discharge waveforms of the reset-up pulse by using the suggested method for both room temperature and 80 ℃ in the reset period. The discharge firing time and the light intensity are nearly constant regardless of temperature variation because the slope rate of the ramp erasing pulse is automatically varied for temperature variation.



(a) Conventional ramp waveform generator (b) Suggested ramp waveform generator

Fig. 11 Schematic diagram of waveform generator.

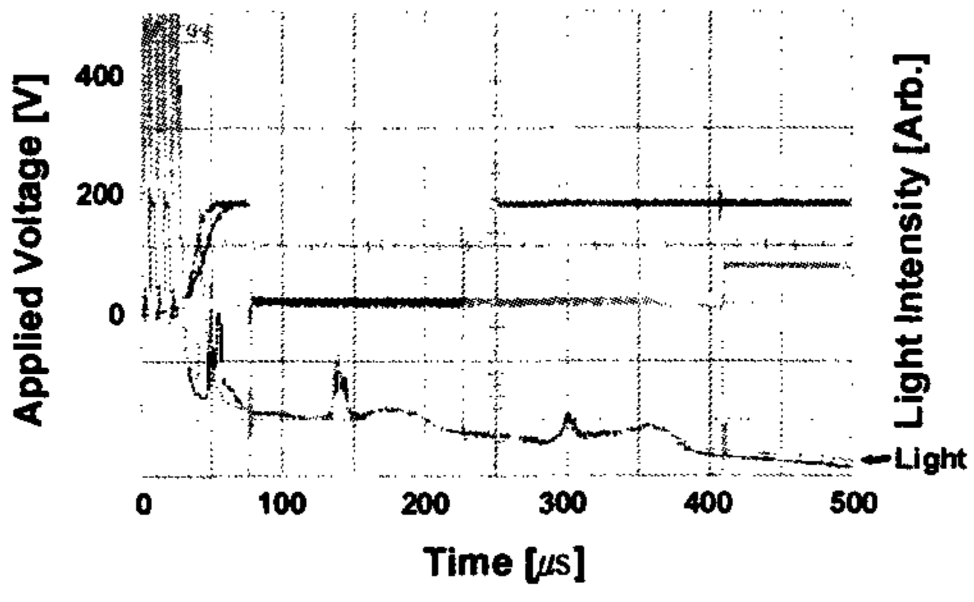
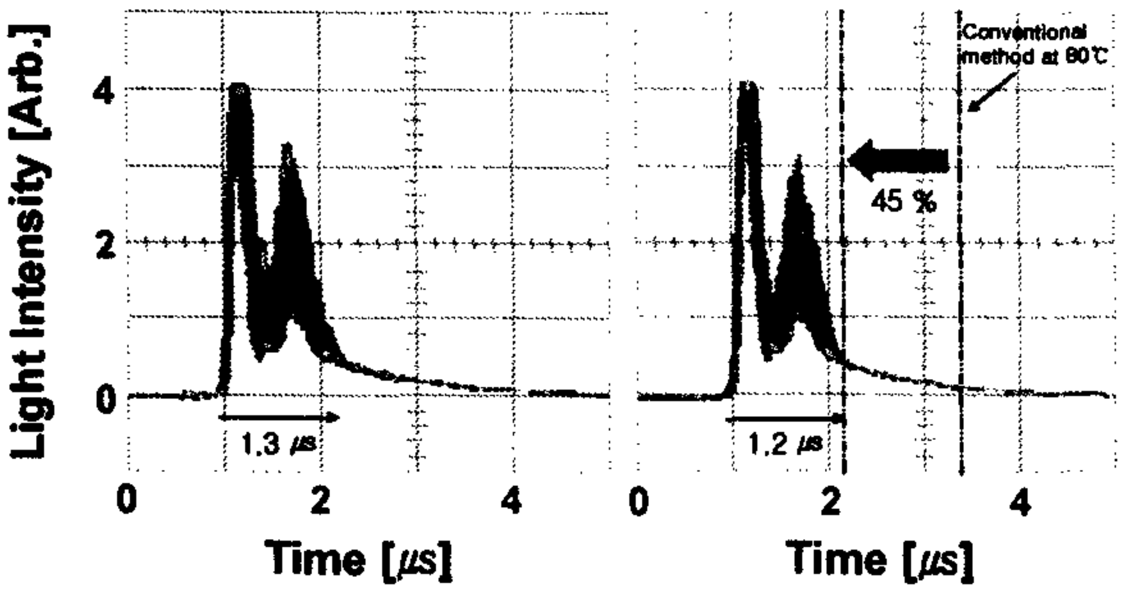


Fig. 12 Discharge waveforms of reset-up pulse using suggested method for both room temperature and 80℃ in the reset period.

Fig. 13 shows the addressing dispersions of discharge cells from Fig. 12. The time of addressing dispersions are also nearly constant regardless of temperature variation. The addressing dispersion of the suggested method decreases about 45 % compared with that of the conventional method at 80℃. As a result, the addressing time can be reduced about 45 % compared with the conventional addressing time at 80℃.

Fig. 14 shows the spectrum intensity of discharging cells by using the suggested method for temperature variation. The variation of spectrum intensity is nearly constant regardless of temperature variation. Fig. 15 shows the relationship between the spectrum intensity of discharging cells with green phosphor and the temperature. The spectrum intensity of suggested method increases about 10 % compared with that of the conventional method at 80℃. This is an indication of misfiring free discharge.



(a) Room temperature (b) 80 ℃

Fig. 13 Addressing dispersions of discharge cells from Fig. 12.

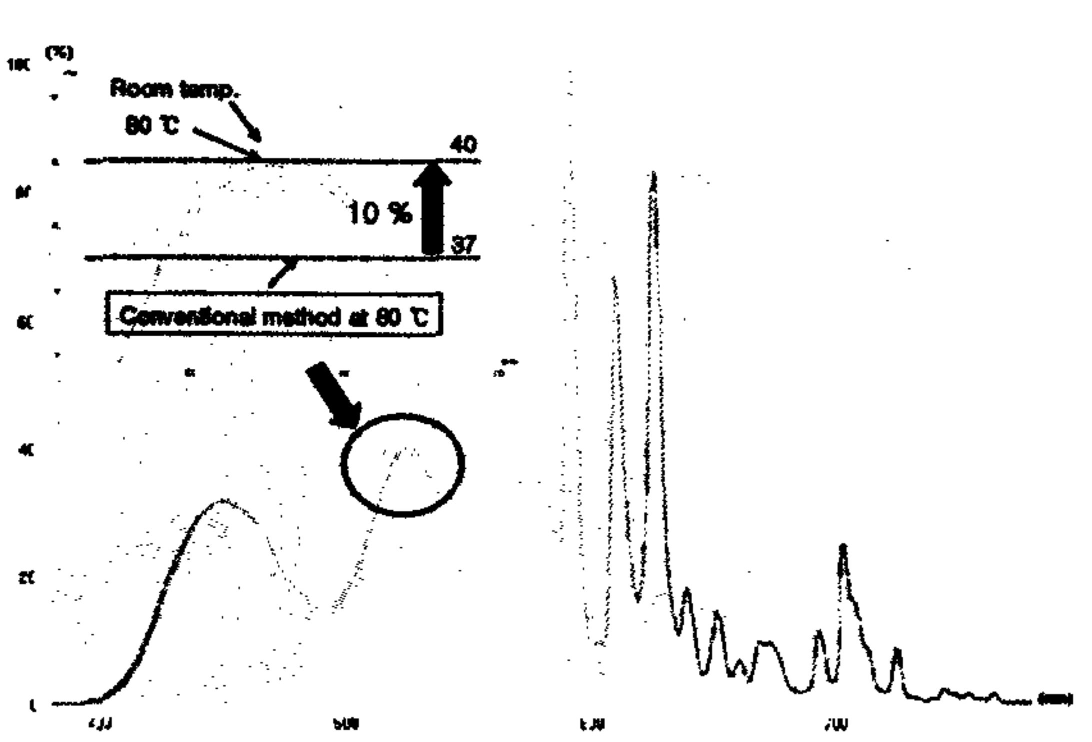


Fig. 14 Spectrum intensities of discharging cells using the suggested method for temperature variation.

7 Conclusion

In this paper a new method which applies automatically different slopes of a ramp erasing pulse for temperature variation is suggested in order to improve the misfiring at high temperature. The effects were experimentally examined by comparing with the conventional method that applies constant slope rates of the ramp erasing pulse. In the case of the conventional method, it is difficult to reduce the misfiring at high temperature because the ambient temperature of panels varies for a situation and a season. Therefore, misfiring with the increases of the addressing time and its dispersion occurs at high temperature. However, in the case of the suggested method, it is possible to reduce the misfiring at high temperature because the new method applies automatically different slope rates of the ramp erasing pulse for temperature variation. Therefore, the discharge firing time of reset period and the addressing time are almost constant regardless of the temperature and the addressing time can be reduced about 45 % compared with the conventional addressing time at 80℃. Moreover, the spectrum intensity of the suggested method increases about 10 % compared with that of the conventional method at 80℃.

References

[1] J P Boeuf, "Plasma display panels: physics, recent developments and key issues", J. Phys. D: Appl. Phys, 36 (2003) R53-R69.

[2] C.-H. Park, S.-H. Lee, D.-H. Kim, W.-G. Lee, and J.-E. Heo, "Improvement of Addressing Time and Its Dispersion in AC Plasma Display Panel", IEEE Trans. Electron Devices, vol. 48, No. 10, pp. 2260-2265, Oct. 2001.

[3] J.-Y. Choi, D.-H. Kim, J.-E. Heo, S.-N. Ryu, J.-H. Ryu, H.-J. Lee, and C.-H. Park, "Effect of ramp-type erase pulse waveform on the high Temperature driving characteristics of ac PDP", Proceedings of The 2nd IMID, pp. 57-60, Aug. 2002.

[4] T. shinoda et al., "High level gray scale for AC plasma display panels using address-display period-separated sub-field method", Trans. IEICE, vol. C-2, no. 3, pp. 349-355, 1998.

[5] S. Yoshikawa et al., "Full-color AC plasma display with 256 gray scale", Jpn. Display, pp. 605-608, 1992.

[6] Larry F. Weber, "Plasma Display Device

Challenges", Proc. Asia display '98, pp. 15-27, Sept. 1998.

[7] C.-H. Park, S.-H. Lee, D.-H. Kim, Y.-K. Kim, and J.-H. Shin, "A Stucy on the New Type Sustaining Electrode Showing High Luminous Efficiency in AC PDPs" IEEE Trans. Electron Devices, vol. 48, No. 10, pp. 2255-2259, Oct. 2001.

[8] C.-H. Park, S.-H. Lee, D.-H. Kim, J.-H. Ryu, and H.-J. Lee, "A Modified Ramp Waveform to Reduce Reset Period in AC Plasma Display Panel", IEEE Trans. Electron Devices, vol. 49, No. 5, pp. 782-786, May 2002.