# 9.1: Flexible electronic-paper active-matrix displays

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## Abstract

*A QVGA active-matrix backplane is produced on a 25µm thin plastic substrate. A 4-mask photolithographic process is used. The insulator layer and the semiconductor layer are organic material processed from solution. This backplane is combined with the electrophoretic display effect supplied by SiPix and E ink, resulting in an electronic paper display with a thickness of only 100µm. This is world's thinnest active-matrix display ever made.*

## 1. Introduction

Flexible displays have the potential to replace part of the paper used today and are therefore a focus of the current display research. The advantages of flexible displays compared to their rigid counterparts are that they weight less, are more rugged and that they could become truly rollable. These are important features for the mobile market.

Flexible displays have been demonstrated based on liquid-crystal [1], polymer light-emitting diodes [2] and electrophoretic ink [3,4]. The use of organic materials in flexible active-matrix displays has a number of important advantages over conventional techniques using mainly inorganic materials. The use of soluble organic materials simplifies the display manufacturing process compared to the conventional chemical vapor deposition techniques. The processing temperature is as low as 170°C, creating the possibility to use a wide range of plastic substrates instead of glass. Furthermore, the mechanical properties of organic materials are compatible with plastic substrates.

The first active-matrix display with an organic semiconductor was reported in 2000 [5]. The display was processed on glass, contained 4096 pixels and was able to show monochrome images. This was rapidly followed by the first active-matrix displays with organic semiconductors on plastic substrates [6,7,8,9].

Here, rollable QVGA active-matrix displays with an organic insulator layer and an organic semiconductor layer that are processed from solution are reported. The active-matrix backplane is combined with the electrophoretic display effects supplied by SiPix and E ink, resulting in a reflective bi-stable display with a thickness of only 100µm.

## 2. The active-matrix backplane

### 2.1 Processing

Our thin-film transistor (TFT) technology is based on a bottom-gate device architecture (Figure 1). This geometry is comparable to the inverted staggered electrode structure as is commonly used for amorphous silicon TFTs. Photolithography is used to pattern the layers, resulting in a total of 4-mask steps. The TFTs are processed on 150mm diameter, 25µm thin polyethylene naphthalate (PEN) films. During the processing the foils are laminated on a silicon support wafer. The organic semiconductor and gate dielectric are processed from solution. Given the specifications of sheet conductivity of the column and row lines in the display metallic electrodes are used. Gate electrodes and first level interconnect lines (*i.e.* the rows) are made by patterning gold using photolithography techniques. The gate dielectric is a 350nm thick photo-imageable polymer (polyvinylphenol) that is spincoated and subsequently exposed to UV light to define contact holes. Source-drain electrodes, pixel pad and second level interconnect lines (*i.e.* the columns) are defined in the second gold layer. On top of this stack, a 100nm thick precursor pentacene film is spincoated. Conversion of the precursor to its active form requires a short heating step at 170°C. The semiconductor is patterned using a subtractive photolithography process.

The key features of this technology are that first a thin flexible foil is glued onto a rigid support, then the functional layer stack is processed and finally the foil containing the microelectronic devices is delaminated from its support without degradation of the devices. The rigid support can be re-used. This allows the use of standard of-the-shelf patterning and deposition equipment. Typically, a registration better than 2.5µm over a 150mm wafer for a 4-mask process is achieved. Integration of transistors over large areas with a relatively small overlap of 5µm is possible. This allows the production of transistors with sufficiently small parasitic stray capacitances for active-matrix displays.

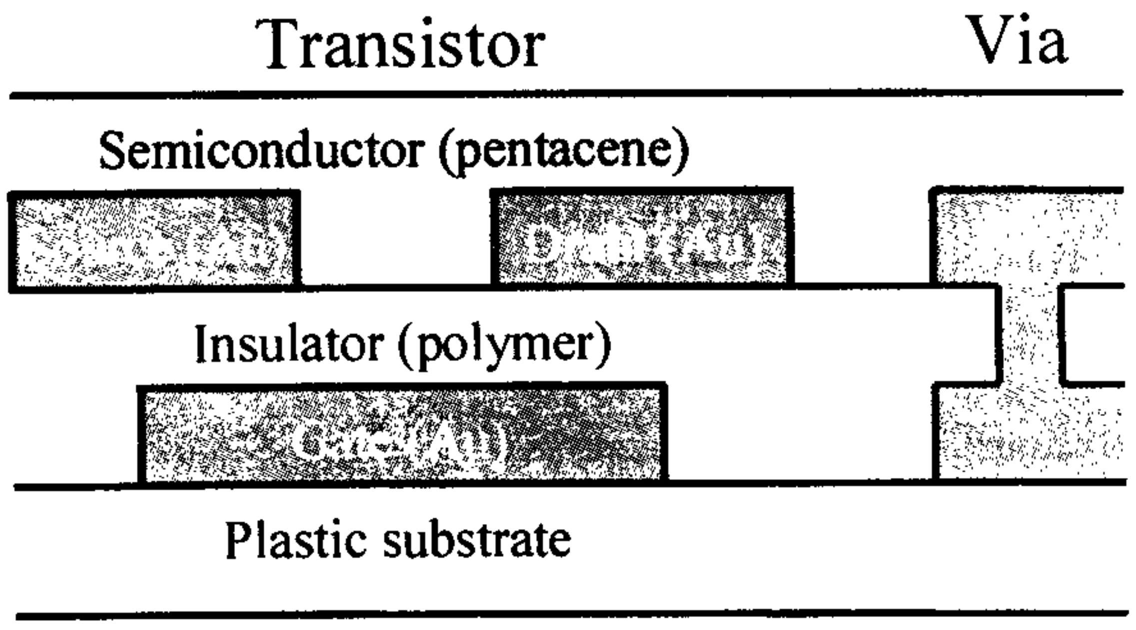


**Figure 1 Cross section of a TFT and vertical interconnect (*via*).**

## 2.2 Design

The display contains 240 rows and 320 columns. The pixel layout is shown in Figure 2. The pixel size is 300x300μm$^2$ resulting in a display diagonal of 4.7 inch. The TFT channel length ($L$) and width ($W$) are 5μm and 140μm, respectively. The pixel pads are made from gold, processed on the source-drain level. This results in a reflective active matrix display, with an optical aperture ratio of 79%. The pixel pads overlap with the preceding row, thus forming the storage capacitors in the usual way.

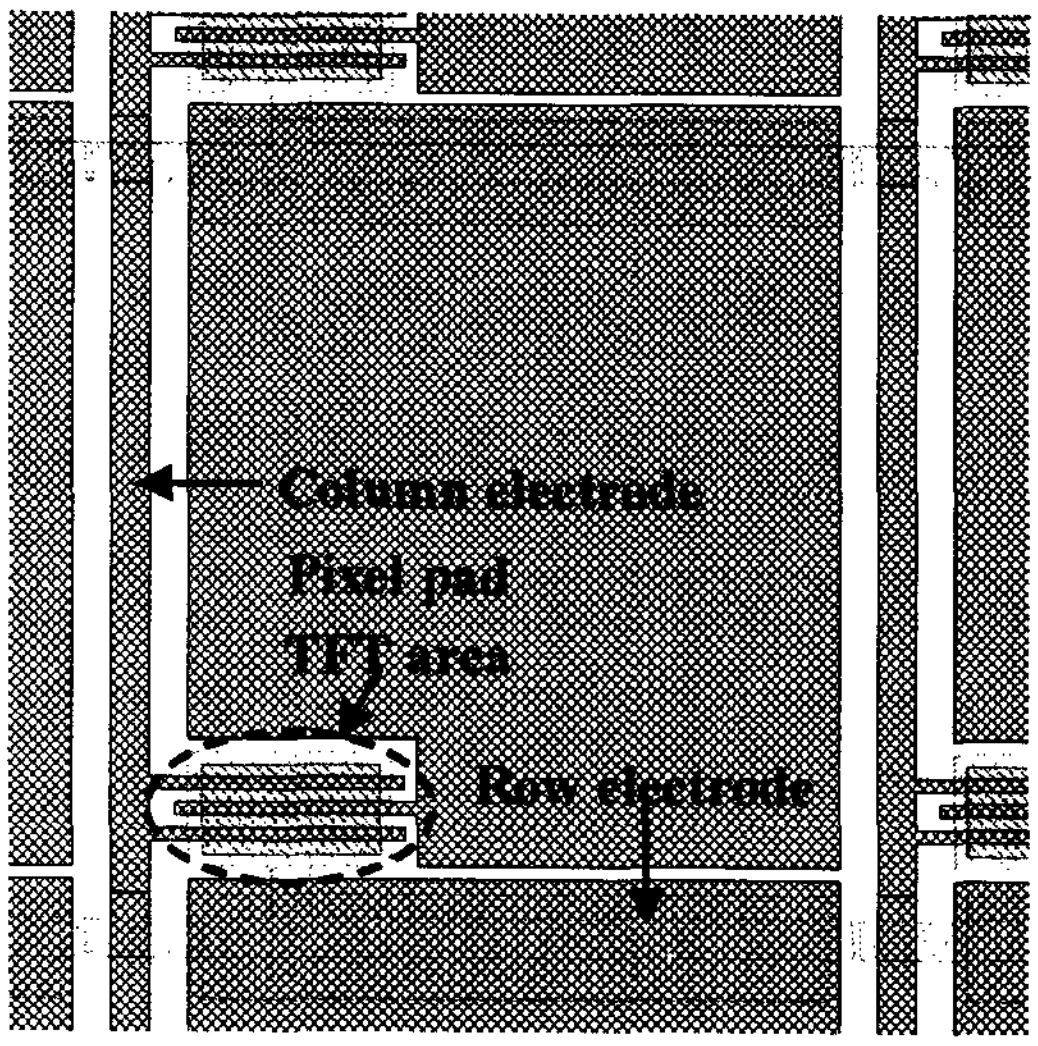


**Figure 2 a) Pixel layout of the QVGA display.**

## 2.3 Transistor characteristics

In Figure 3a the transfer characteristic of an organic TFT is shown. A prerequisite for an active-matrix display is sufficient control over the spread in TFT parameters. An impression of the uniformity is given in Figure 3b, where the distribution of the field-effect mobility of a large number of our TFTs in the active-matrix backplane is shown. The average field-effect mobility is 0.01cm$^2$/Vs at a gate bias of -20V. The current modulation, measured between a gate bias of 0V and -20V, exceeds $10^6$.

## 2.4 Transistor requirements

### 2.4.1 *Display addressing*

The displays are addressed row-at-a-time. During one frame all the rows are sequentially selected by applying a voltage that switch the TFTs from the non-conducting to the conducting state. During the row selection period the pixel capacitors of the selected row are charged to the voltage supplied on the column electrodes. During the remaining frame time (*i.e.* the hold time) the other rows are addressed. The TFTs are then in their non-conducting state and the charge on the pixel capacitors must be retained. Typical voltages that are used on the rows are –25V during row selection and +25V during the hold time. Typical column voltages are –15V, 0V and +15V.

The electrophoretic display effect is bi-stable. Therefore both the initial switching state as well as the final switching state must be taken into account during the image update. This is called differential driving [10]. For example, when a pixel is in the low reflectance state and remains in the same state in the next image ideally no pulse should be applied to that pixel, while a full length

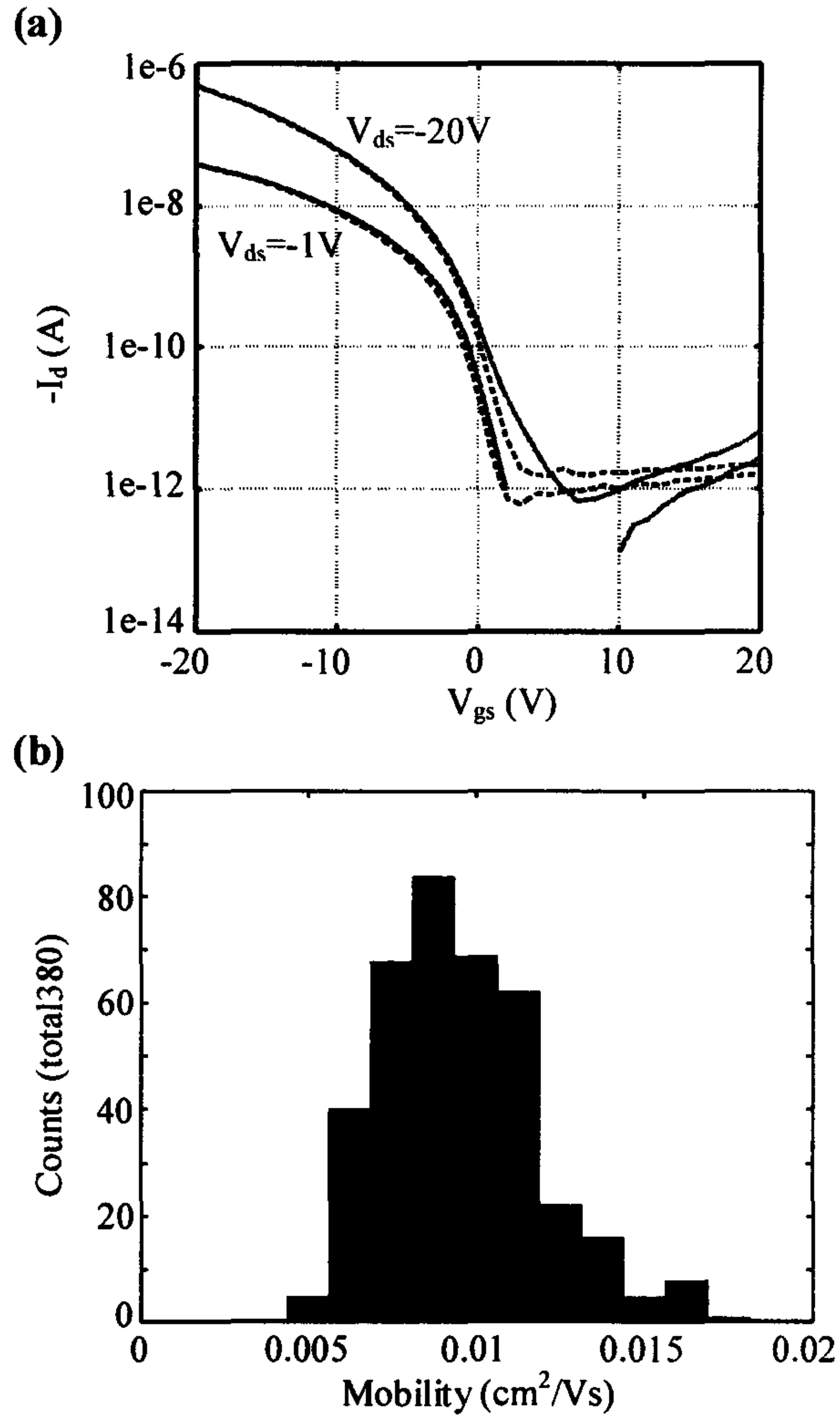


**Figure 3 a) Transfer characteristics of a pixel TFT with typical mobility 0.01cm$^2$/Vs. b) Distribution of the mobility (extracted for $V_{gs}$=-20V and $V_{ds}$=-1V) of 380 TFTs measured on a QVGA active-matrix backplane.**

pulse is required when the pixel is changed from the low reflectance to the high reflectance state. The application of shorter pulses (*i.e.* pulse width modulation) or a lower pixel voltage (*i.e.* amplitude modulation) results in intermediate reflectance levels (*i.e.* gray levels). We use pulse width modulation as this permits the use of simple 3-level column drivers (-15V, 0V and +15V).

Our TFT backplane design is optimized to be addressed at 50Hz. The smallest possible grey-to-grey transition time that can be generated by our active-matrix backplane is therefore 20ms. The switching time of electrophoretic display effects is generally larger. Grey levels are therefore generated by applying a pixel voltage during one or more frames.

### 2.4.2 *The TFT model*

A frame rate of 50 Hz imposes restrictions on the minimum field-effect mobility and the maximum off-current of the TFTs. In order to estimate the transistor requirements for our display, we make use of a transistor model that includes a gate-voltage dependent field effect mobility:

$$\mu_{FE} = \mu_0\left(-V_{gs} + V_T\right)^{\gamma},$$

where $V_T$ is the threshold voltage. Parameter $\gamma$ is a fit parameter that has a value close to 1 for the organic semiconductor and parameter $\mu_0$ is equal to the mobility at $-V_{gs}+V_T$=1V. By combining this equation with the classical analytical Shockley expression for the drain current in a MOS transistor [11], the following expression for the drain current in the linear regime is derived:

$$I_d = \frac{W}{L}\frac{\mu_0 C_i}{(\gamma+2)}\left[\left(-V_{gs}+V_T\right)^{\gamma+2} - \left(-V_{gs}+V_T+V_{ds}\right)^{\gamma+2}\right],$$

where $C_i$ is the gate insulator capacitance per unit area.

### 2.4.3 *Allowed leakage current*

A low leakage current in the pixel TFTs is required in order to achieve a constant pixel voltage during the complete frame. The leakage current of our pixel TFTs is very low (<10pA), as can be seen in Figure 3a. Circuit simulations with the equivalent circuit of the pixel layout shown in Figure 2 show that more than 99% of the pixel voltage is retained during the complete frame time. These are excellent TFT voltage holding properties for an active-matrix display.

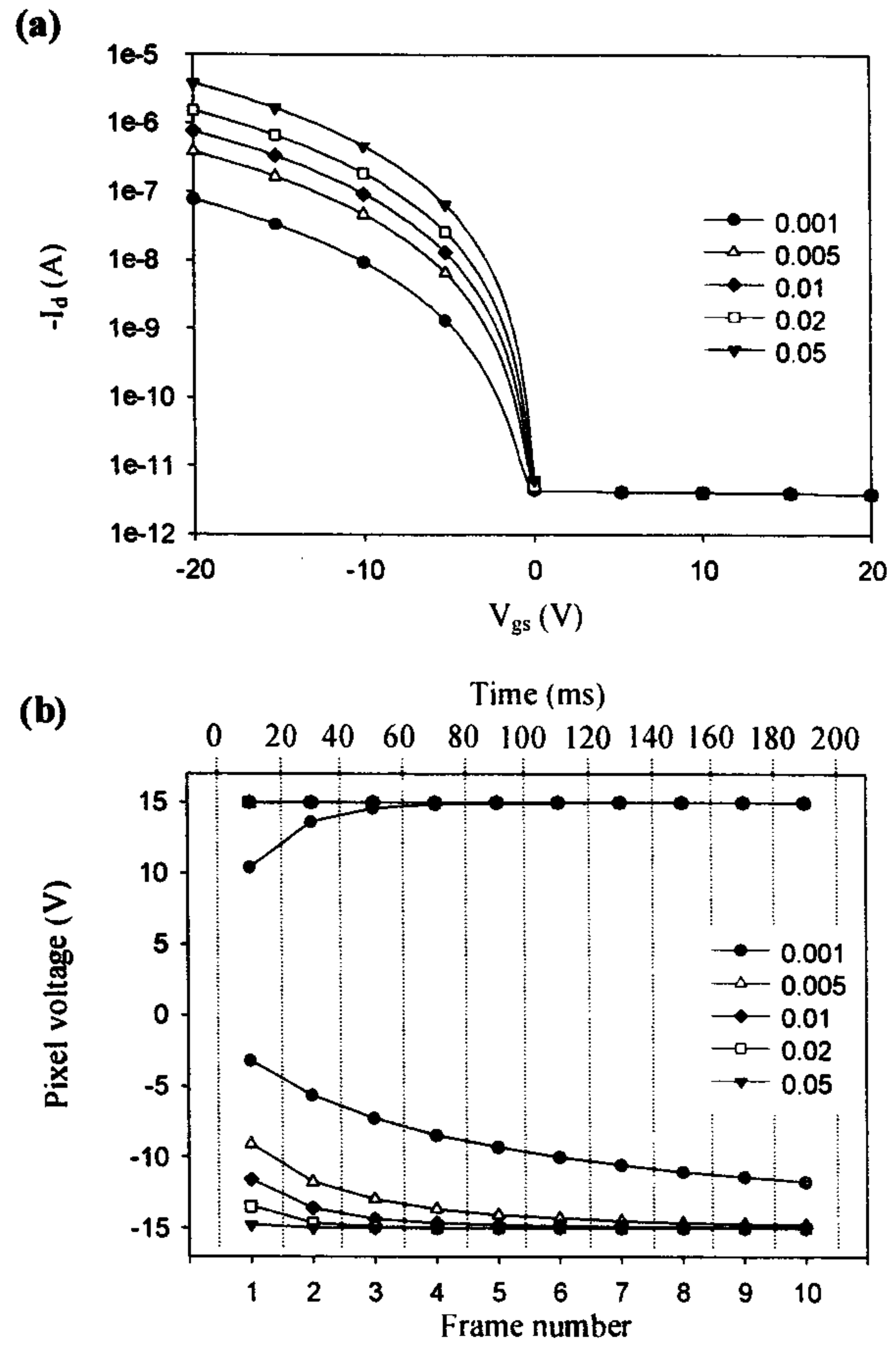


**Figure 4 a) Simulated transfer characteristics as a function of parameter $\mu_0$ for $V_{sd}$ = 20V. The resulting field-effect mobility at $V_{sg}$-$V_T$=25V and parameter $\gamma$=1.1 is indicated in the legend. The leakage current was set to 3pA. b) Simulated charging behavior for pixel with the same five values for the mobility. The vertical axis shows the pixel voltage, the horizontal axis the frame number. The simulated frame rate was 50Hz. No frame inversion is applied, as electrohporetic display effects are DC-driven.**

### 2.4.4 *Required field-effect mobility*

The required field-effect mobility is determined by performing circuit simulations of the pixel circuit. Parameter $\mu_0$ is varied between simulations. The resulting mobility is determined at $V_{gs}$=-20V, with $\gamma$=1.1. The transfer characteristics of the simulated transistor are shown in Figure 4a. The on-current increases with increasing field-effect mobility. The off-current is sufficiently small in order to retain more than 99% of the charge during the hold time for all simulations. The resulting charging behavior of the pixel is shown in Figure 4b. The vertical axis shows the average pixel voltage during one frame; the horizontal axis shows the frame number. Pixel charging toward -15V and 15V is simulated for every indicated value of the mobility. Charging to –15V is slower than charging to +15V due to the smaller source-gate voltage.

The average mobility of our pixel TFTs is 0.01cm$^2$/Vs (see Figure 3b). At a mobility of 0.01cm$^2$/Vs charging to +15V is complete, while charging to -15V results in a pixel voltage of -12V during the first frame. The average pixel voltage during the first five frames is –14V, which is a charging ratio of 93%. As the smallest pulses supplied to the pixels are five frames or longer when generating images with four gray levels at a refresh rate of 50Hz, the effect of incomplete charging during the first frame is small. By comparing the average pixel voltage with the switching curves (not shown here) it was verified that it is possible to generate at least four gray levels with sufficient uniformity at a mobility of 0.01cm$^2$/Vs.

## 2.5 Backplane summary

In Table 1 the specifications of our active-matrix backplane are summarized.

**Table 1 Specifications of the rollable QVGA active-matrix backplane.**

| | |
|---|---|
| Backplane size | 4.7inch (72mm x 96mm) |
| Resolution | 320x240 (85ppi) |
| Number of pixels | 76800 |
| Pixel size | 300µm x 300µm |
| Aperture ratio | 79% |
| Backplane thickness | 25µm |
| Backplane weight | 0.39grams |
| TFT channel length | 5µm |
| TFT channel width | 140µm |
| Mobility | 0.01cm$^2$/Vs |
| Current modulation | $10^6$ |

## 3. Functional electrophoretic displays

## 3.1 Rollable SiPix displays

The SiPix electrophoretic display effect uses microcups with positively charged white sub-micron particles in a blue ink [3]. Moving the white particles to the top of the microcapsules generates the white state. Moving the white particles to the bottom of the microcups generates the blue state. This "electronic ink" film is laminated onto the active-matrix backplane.

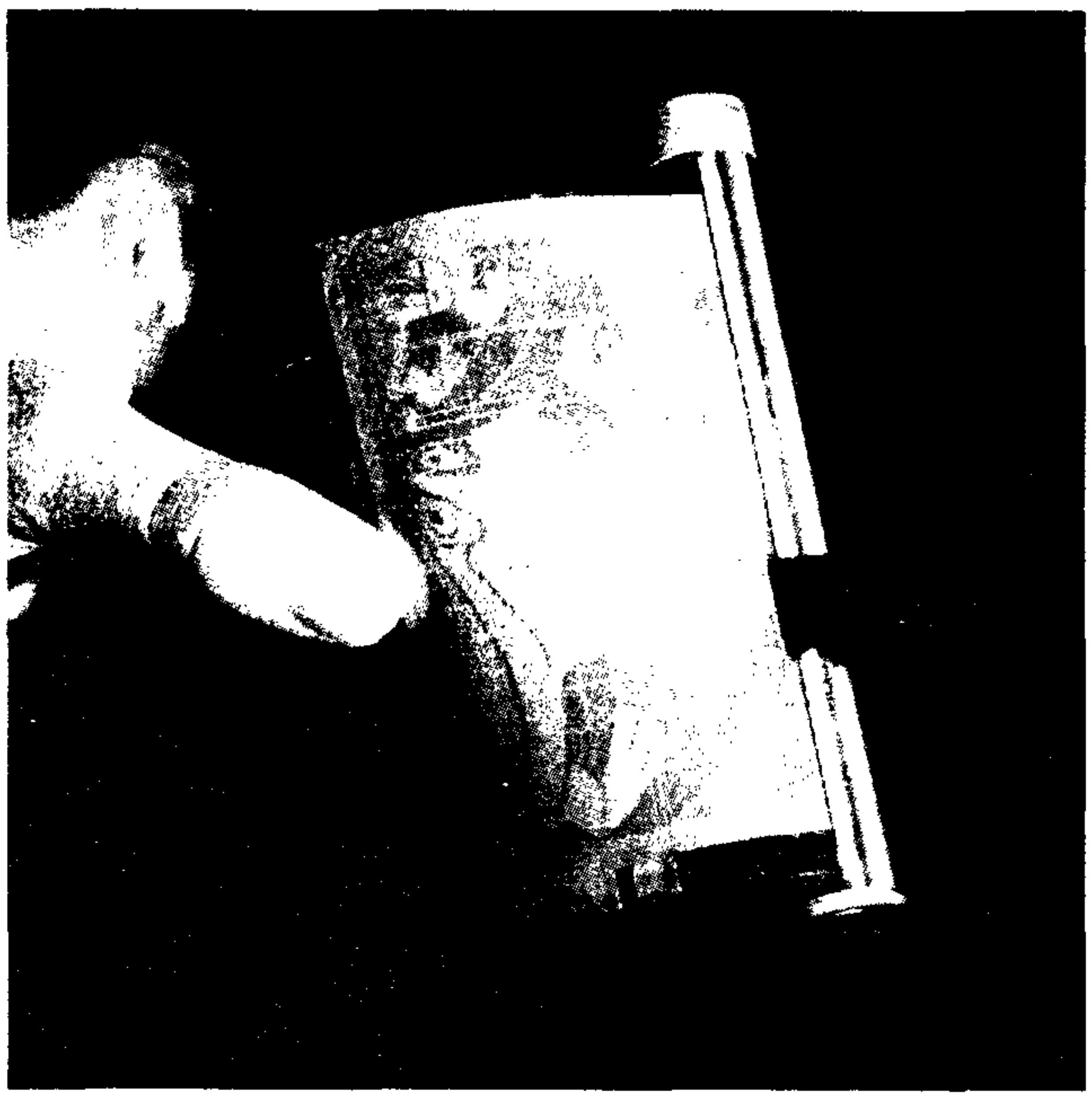

**Figure 5: A picture of the rollable QVGA active-matrix display with organic TFTs combined with the SiPix electrophoretic display effect. The frame rate is 50Hz, the image update time ~1s.**

In Figure 5 the display is shown while rolled into a stick with a diameter of 1cm. The display is 130μm thick and can be bent to a radius of 1cm (0.4inch) more than 400 times without degradation. The switching speed is about 1s at a pixel voltage of 15V. An image containing 4 grey levels is shown.

## 3.2 Rollable E ink displays

The E ink electrophoretic display effect film consists of microcapsules in a polymer binder, coated onto a polyester / indium tin oxide sheet [4]. Optical contrast is achieved by moving black and white sub-micron particles with opposite charge in a transparent fluid within a microcapsule. Depending on which sub-micron particles are closest to the viewer, light is scattered back (white state) or absorbed (black state).

A picture of a functional display is shown in Figure 6. The display is 100μm thick and can be bent to a radius of 1cm without degradation. The switching speed is about 0.5s at a pixel voltage of 15V. The white state has a reflectivity of 35%. The optical contrast is 12. An image containing 4 grey levels is shown.

## 4. Conclusions

World's thinnest active-matrix displays have been demonstrated. The combination of the 25μm thick active-matrix backplane with the SiPix and the E ink electrophoretic display effects resulted in displays with a thickness of 130μm and 100μm, respectively. As the displays can be bent hundreds of times to a radius of 1cm, these displays can be used as flexible electronic paper.

## 5. Acknowledgements

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**Figure 6: A picture of the rollable QVGA active-matrix display with organic TFTs combined with the E ink electrophoretic display effect. The frame rate is 50Hz, the image update time ~0.5s.**

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