8.3: Progess in Fabrication Technologies of Polycrystalline Silicon Thin Film Transistors at Low Temperatures

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Abstract

The development of fabrication processes of polycrystalline-silicon-thin-film transistors (poly-Si TFTs) at low temperatures is reviewed. Rapid crystallization through laser-induced melt-regrowth has an advantage of formation of crystalline silicon films at a low thermal budget. Solid phase crystallization techniques have also been improved for low temperature processing. Passivation of SiO_2/Si interface and grain boundaries is important to achieve high carrier transport properties. Oxygen plasma and H_2O vapor heat treatments are proposed for effective reduction of the density of defect states. TFTs with high performance is reported.

1. Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs) have been widely applied to fabrication of electronic devices. Low temperature fabrication is attractive for introducing poly-Si TFTs to a device application, such as liquid crystal flat panel display or organic electroluminescence displays [1-3]. Many technologies have been developed for low temperature fabrication. There is for example laser crystallization of silicon films formed by plasma enhancement chemical vapor deposition (PECVD). It allows us to form poly-Si films at temperature of about 300°C [4-7]. Formation of large crystalline grains is attractive for TFT with high performance [8-10]. Metal induced crystallization has reduced crystallization temperature to 400°C [11-13]. However, inevitable grain boundaries among crystalline silicon grains can have electrically active defect states because of lattice disordering and dangling bonds. The defect reduction is therefore one of most important problems on low-temperature fabrication of poly-Si TFTs. We have recently reported improvement of electrical properties of laser crystallized silicon films by oxygen plasma treatment as well as heat treatment with high-pressure H_2O vapor [14-18]. Defect states are changed to electrically inactive through the treatment.

In this paper, crystallization technologies are first reviewed for low temperature processing. Structural and electrical properties of poly-Si films are argued. Passivation of SiO_2/Si interface and grain boundaries is also discussed. Fabrication of TFTs with a high mobility and a low threshold voltage is reported. Analysis of defect reduction is finally discussed.

2. Crystallization of silicon films

Laser crystallization is one of most attractive methods for polycrystalline films formation. Pulsed UV-laser light is effectively absorbed in the silicon surface because of the high absorption coefficient $\sim 10^6$ cm^{-1} of silicon at wavelength lower than 350 nm. The absorbed light simultaneously excites the electronic states of silicon. The energy of the excited states is relaxed to lattice vibration states within the time on the order of 10^{-12} s [19]. In the case of ns-order pulsed laser irradiation, lattice heat is therefore the most important interaction. The heat energy generated at the surface region caused by light absorption diffused into interior regions of silicon films. The high heat diffusion coefficient of silicon results in heat diffusion into the underlying substrates. The heating characteristics of silicon films therefore depend on thermal properties of substrates. Thin silicon films are effectively heated to when SiO_2 glass substrates is used because heat diffusion coefficient of glass is low at ~1.4 W/mK [20]. The system of silicon film/glass substrate gives an essential advantage of low required energy for crystallization in order to apply the laser heating method to electric devices.

Crystallization of 50-nm-thick silicon films formed on glass substrates occurred when silicon films were heated by pulsed XeCl excimer laser with a pulse width of 30 ns, a wavelength of 308 nm and a laser energy density above 160 mJ/cm^2. Silicon films are melted by laser irradiation and then solidified to crystalline state. The transient conductance measurements revealed that the rapid liquid/solid interface-controlled solidification occurred with a velocity of 0.6 m/s for the partial melting condition below 450 mJ/cm^2 [21]. Crystalline grains with sizes of 50-200-nm were successfully formed with no serious disordered region, as shown by a photograph obtained by transmission electron microscope in Fig.1.

Large grain growth to the lateral direction is attractive for single crystalline TFTs. If crystalline silicon with a grain size around 5 µm is fabricated, it is possible to form the channel region of TFTs in a single crystalline grain to avoid grain boundary effect which may disturb carrier transport. Im *et al.* have reported a rapid lateral grain growth ~5 µm by a single pulse irradiation with an energy just below the microcrystallization threshold energy without heating the substrate [8]. At the condition, the density of the crystalline nucleation is reduced and rapid crystallization in the lateral direction is caused by a large

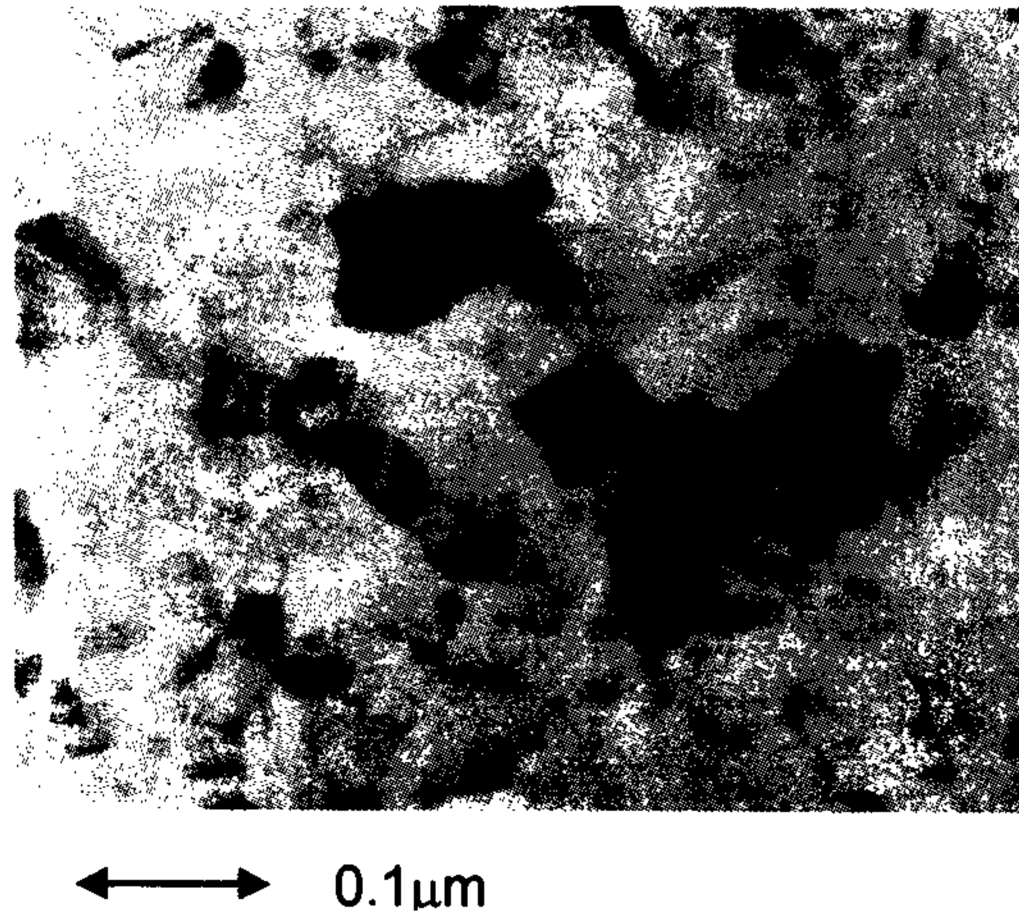

Fig.1. Plan-view bright field TEM image of 30-nm-thick poly-Si films crystallized at 300 mJ/cm^2.

difference of the free energy between the liquid silicon and the solid silicon. P.Ch.van der Wilt *et al.* reported grain filtering method for grain location control using combination of local buried crystalline seeds with laser-induced-complete melting of silicon films [22]. Crystalline grains with a size of 6 μm were well formed. OH *et al.* reported large crystalline grain growth ~5 μm using phase shift mask in order to make spatial distribution of laser intensity for generation of temperature distribution [9].

A high-power-diode-pumped solid state CW laser (Nd:YVO4) has been recently applied the laser to crystallization of silicon films [10.23]. The long dwell time laser beam about 100 μs resulted in long melt duration of silicon films and caused lateral crystallization with a large grains ~10-20 μm. Light absorption coefficient for silicon is low of ~ 10^4 cm^{-1} at 532 nm, which is much lower than that of 10^6 cm^{-1} at 308 nm. Although a green CW laser requires high laser energy consumption and long tact time for crystallization of silicon films because of low absorption coefficient, its very stable characteristics on laser emission is attractive for crystallization of selective area for TFT fabrication.

Crystallization methods with no laser are also attractive for low cost formation of crystalline films. We have recently developed the electrical-current-induced joule heating as a simple and rapid thermal annealing method [24-26]. Crystallization of silicon films has been achieved through melt-regrowth by micro-second rapid heating caused by electrical-current-induced joule heating with an energy threshold of 0.6 J/cm^2. High quality polycrystalline silicon has been formed with the grain size from 0.2 to 5 μm. Activation of impurity atoms has also been demonstrated. Heavily doped silicon with a carrier concentration of ~10^{21} cm^{-3} has been formed. High efficiency of transformation from electrical energy to heat energy is important for simple TFT processing at low cost.

Metal induced crystallization or metal induced lateral crystallization have been widely investigated for simple crystallization [11-13, 27, 28]. $NiSi_2$ crystallites reduced crystallization temperature below 400°C because of lattice matching between $NiSi_2$ and Si. Large crystalline grains above 10 μm have been demonstrated.

3. Structural and Electrical Properties of Polycrystalline Silicon Films

Rapid melt-regrowth technique results in formation of high density of crystalline grains. Measurement of Raman scattering spectra has revealed that there is a significant tensile stress ~8.0×10^8 Pa in thin silicon films on glass substrates because of initial stress at silicon/substrate interface [29]. Kitahara *et al.* characterized spatial distribution of film stress of the laser crystallized silicon films using micro-Raman spectroscopy with a highly spatial resolution [30]. The tensile stress is accumulated in grain. The stress is relaxed at grain boundaries. The tensile stress is estimated to be 1×10^9 Pa at the central region and 7×10^8 Pa at grain boundaries. Tensile stress reduces the effective mass of electron and hole [31]. It will be an advantage of that the carrier mobility can be large in tensile strained silicon films.

Crystallographic analyses using TEM suggest that pulsed laser crystallized silicon films have crystalline grains with few defects. The free carrier optical absorption analysis makes it possible to investigate electrical properties in crystalline grains. An analysis of optical reflectivity or transimissivity spectra of doped silicon films gives the average carrier mobility and the carrier density in crystalline grains because free carrier optical absorption occurs via excitation induced by the electrical field of incident photons followed by energy relaxation in the crystalline grains [32,33]. The analysis of free carrier absorption gave a large carrier mobility about 20 cm^2/Vs for samples annealed at 160 mJ/cm^2, although the average grain size was small. about 10 nm. The carrier mobility increased to 40 cm^2/Vs as the laser energy density increased. Irradiation with a single pulse and five pulses for each energy density step resulted in approximately the same carrier mobility. These results indicate that laser irradiation formed crystalline grains with good electrical characteristics even for lower energy densities near the crystallization threshold energy. On the other hand, the Hall effect measurements provide the effective carrier mobility of the electrical current which traverses many grain boundaries in polycrystalline silicon films. It strongly depends on grain boundary properties. The carrier mobility obtained by the Hall effect measurements increased from 3 cm^2/Vs to 28 cm^2/Vs as the laser energy density was increased. This result is interpreted as improvement of the grain boundary properties by laser irradiation with high energy densities because the carrier mobility obtained by Hall effect measurements is the drift mobility which is affected by carrier trap states and a high potential energy barrier at the grain boundaries. We recently estimated disordered region of electronic states at grain boundaries with analysis of transmission electron microscope and optical reflectivity spectra [34]. Our analysis resulted in the average width of electrical disordered states at grain boundaries was 5 nm for silicon films laser crystallized at 360 mJ/cm^2. 10 lattice layers had electrically disordered states at grain boundaries. It is interesting that Ge incorporation reduced the disordered states. In the case of $Si_{0.4}Ge_{0.6}$ film, the width of disordered states was less than 1.9 nm. SiGe films has a possibility of formation of low-disordered grain boundaries.

4. Defect Passivation and SiO_2/Si Interface Formation

In spite of good electrical properties of crystalline grains, ESR study revealed pulsed laser crystallized silicon films had a high density of dangling bonds above 10^{18} cm^{-3}, which were localized at grain boundaries [18]. The defects caused by the dangling bonds trapped of free carriers so that they affect carrier transport in polycrystalline films. Reduction of defects by post annealing is important for fabricate high performance TFTs. The properties of the gate insulator/silicon interface is also important because carriers generate just near the interface in TFTs by gate voltage application.

Hydrogenation has been widely used to terminate defects in poly-Si, such as dangling bonds [35-39]. Plasma hydrogenation is especially effective to improve electrical properties of laser crystallized silicon films. Hydrogen atoms effectively incorporated into silicon films and terminated dangling bonds. For 50nm-thick films, plasma hydrogenation at 250°C only for 30 s markedly reduced the density of defect states. However, hydrogen may not be the only specie that can terminate the trap states. In addition, the thermal stability of Si-H bonds in not very good because the Si-H bonds are easily broken at temperatures around 400°C. Actually, it is reported that the self-heating of TFT induce disorption of hydrogen results in the increase of trap states and degradation of TFT performance during operation.

We have developed oxygen plasma treatment and H_2O vapor heat treatment for passivation of grain boundaries. For investigation of defect reduction using oxygen plasma, 7.4×10^{17}-cm^{-3}-phosphorus-doped amorphous silicon films 50 nm-thick formed on quartz substrates were used. The films were crystallized by irradiation of a 30 ns pulsed XeCl excimer laser at 400 mJ/cm^2 in vacuum at 10^{-4} Pa at 250°C by crystallization case [15]. Immediately after the crystallization, oxygen at 100 sccm was introduced at a pressure of 130 Pa into the chamber and an electrode was positioned in front of the samples; then, oxygen plasma at 30 W was generated by applying a 13.56 MHz rf voltage to the electrode. For as-crystallized silicon films, the electrical conductivity was very low 10^{-5} S/cm. It rapidly increased with the activation energy of 0.4 eV as the temperature increased. After oxygen plasma treatment, the electrical conductivity increased to 10 S/cm and the activation energy decreased. Oxygen plasma treatment made the defects electrically inactive and changed localized electron states to extended states. Defect states localized at grain boundaries were oxidized by incorporating oxygen atoms into silicon films with the help of plasma heating. The dangling bonds of silicon atoms were eliminated and Si-O bonds were formed.

Heat treatment with high-pressure H_2O vapor is also effective for defect reduction of polycrystalline silicon films [18]. 7.4×10^{17}-cm^{-3}-phosphorus-doped crystallized silicon films were also used for investigation of change in the electrical conductivity. The films were annealed with 1.3×10^6-Pa-H_2O vapor from 190 to 310°C for 3 h. The electrical conductivity increased to 6 S/cm as the annealing temperature increased to 310°C. This result means that the free carrier density increased after the treatment. ESR measurements revealed that undoped-laser crystallized 400 mJ/cm2 silicon films a high spin density of 5×10^{18} cm^{-3}. The spin density was reduced to 1.2×10^{17} cm^{-3} by the high pressure H_2O vapor heat treatment at 310°C. The dangling bond was effectively passivated by heat treatment with high-pressure H_2O vapor. Defect states at grain boundaries reacted with H_2O molecules. H2O molecules at defect sites would be chemically dissociated with the help of heating energy. The dangling bonds of silicon atoms were probably eliminated through the formation of Si-O, Si-OH or Si-H bonds.

The changes in the electrical conductivity with temperature were analyzed with the numerical method with finite element method in order to estimate the density of defect states. Although the as- crystallized silicon films had a defect density of 4×10^{17} cm^{-3}, the density of defect states were reduced to 2×10^{16} cm^{-3} with oxygen plasma treatment for 30 min, as shown in Fig.2 (a). In the case of H_2O vapor heat treatment, the initial density of defect states was 8.4×10^{17} cm^{-3} for the room temperature crystallized films, as shown in Fig. 2(b). The room temperature crystallized films had a higher density of defect states than the 250°C crystallized film. The silicon films were rapidly cooled to room temperature with a high cooling rate during crystallization. Rapid formation of grain boundary probably resulted in high density of dangling bonds. The density of defect states was reduced to 4×10^{16} cm^{-3} at 310°C for 1.3×10^6 Pa-high-pressure H_2O vapor annealing for 3 h, as shown in Fig.2 (b). When the density of defect states was reduced by present heat treatments, the number of electrons trapped at defect states was also reduced so that the space charge effect decreased. This resulted in an increase of the average carrier density in crystalline grains.

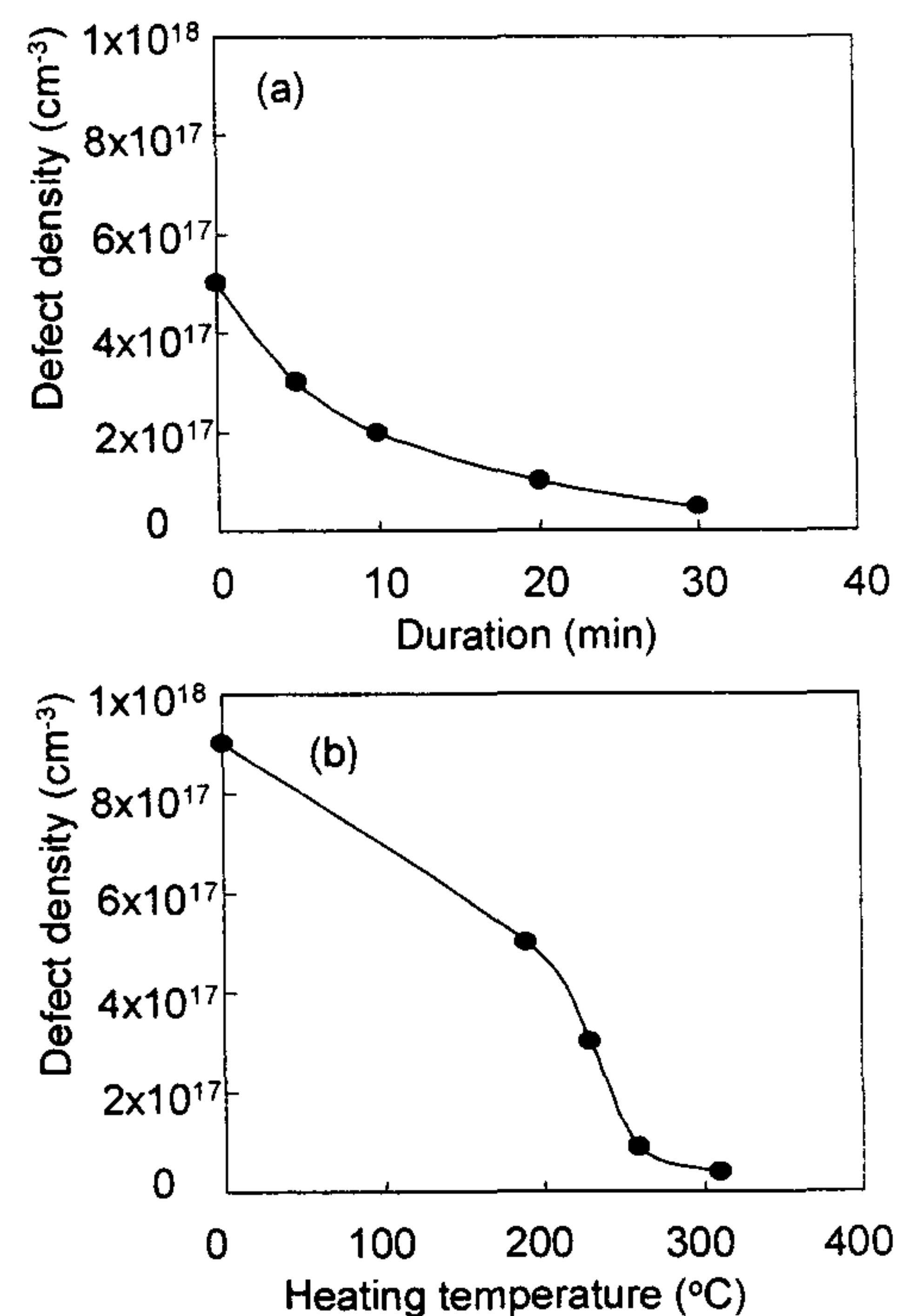

Fig.2 Density of defect sates of poly-Si fabricated at 400 mJ/cm^2 as functions of oxygen plasma duration at 250°C and 30W of RF power (a) and temperature of 1.3×10^6-Pa-H_2O vapor heat treatment

The high pressure H_2O vapor heat treatment is also useful for gate insulator/Si interface passivation at low temperature. Si-O bonding network can be relaxed states by hydrolysis reaction with H_2O molecules with a help of thermal energy below 300°C. Figure 3 shows capacitance-vs-voltage (C-V) characteristics at a frequency of 100kHz and quasi static for Al gate metal-oxide-semiconductor capacitors with 100-nm-thick SiO_2 films formed by plasma enhanced chemical vapor deposition. The samples were heated in $1.3x10^6$-Pa-H_2O vapor at 260°C for 9h. Sharp change in the capacitance with low gate voltages were observed. The analysis of the C-V curves revealed that the density of interface trap states was $3x10^{10}$ $cm^{-2}eV^{-1}$. The high-pressure H_2O vapor annealing improved SiO_2/Si interface properties to a stable state.

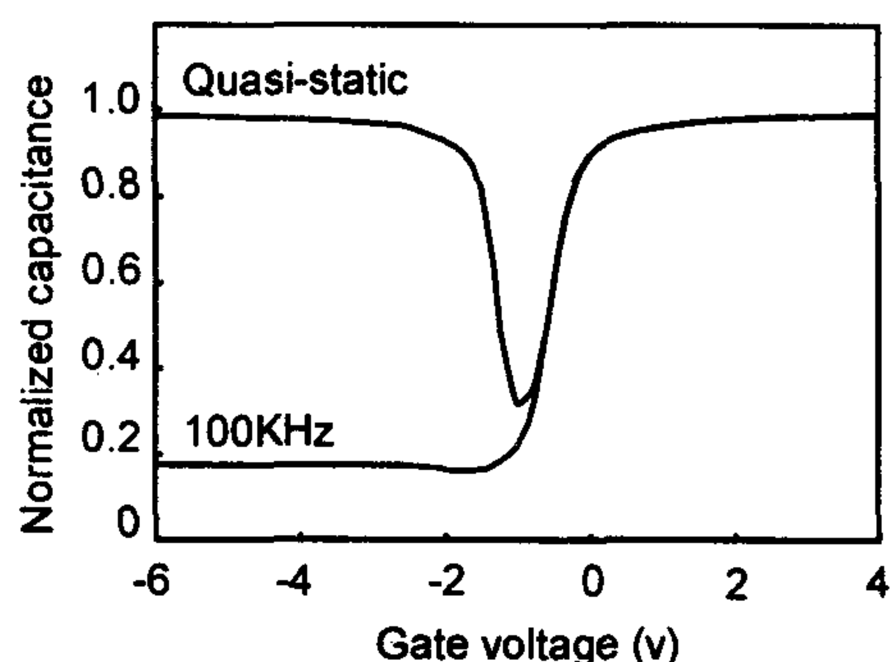

Fig.3 Capacitance responses as a function of gate voltage with 100 kHz and quasi-static frequency for Al Gate MOS capacitors with 100-nm-thick SiO2 films formed on N-type silicon substrates using PECVD.

5. Poly-Si TFTs fabrication and their characteristics

Many important researches for developing TFT fabrication processes have been done. Method of large crystalline grains formation through lateral growth using pulsed laser and CW laser annealing has been well applied to increase TFT performance. High carrier mobility of 400-600 cm^2/Vs and low threshold voltage less than 2 V have been reported [6,10,22,23,40]. These technologies are promising for TFT circuits with a high operation speed. Fabrication of TFTs with MIC, MILC and joule heating is also important for low cost processing. The carrier mobility higher than 400 cm^2/Vs and the low threshold voltage less than 3 V have been reported [26, 41, 42].

It is also important to solve the problem of interface and grain boundary passivation. Simple thermal relaxation processes such as high temperature annealing and thermal oxidation can not be used for low temperature processing. We have applied oxygen plasma and H_2O vapor heat treatments to TFT fabrication [43]. Those methods have a possibility of interface and boundary passivation at low temperatures.

25-nm-thick undoped and phosphorus doped amorphous silicon films were crystallized in vacuum at $3x10^{-4}$ Pa by 30ns-pulsed XeCl excimer laser in order to form the undoped channel region and the doped source and drain regions. After laser crystallization, some silicon films were treated with oxygen plasma at 250°C for 5 min at a 13.56-MHz-RF power of 100 W at a gas pressure of 130 Pa in order to reduce defect density in polycrystalline silicon films. Some samples were also annealed at 250°C with $1.3x10^6$ Pa H_2O vapor for 3 h for further defect reduction. The molecular beam deposition method was used for formation of the gate insulator. 55-nm-thick SiO_x layers were formed using Knudsen cell in oxygen radical at $1x10^{-2}$ Pa. Contact holes were then opened in the SiO_x layer on the source and drain regions. Gate, drain and source electrodes were formed with Al metals. After fabrication of the TFT structure, TFTs were heated at 200°C with $1.3x10^6$ Pa-H_2O vapor for 3 h for improvement SiO_2 properties. The specific dielectric constant of the SiO_2 layer, the densities of interface traps and fixed oxide charges were estimated to be 4.9, $2.0x10^{10}$ $cm^{-2}eV^{-1}$ and $3.4x10^{10}$ cm^{-2}, respectively, after H_2O vapor heat the treatment at 200°C with $1.3x10^6$ Pa H_2O vapor for 3 h.

If TFTs were fabricated with no oxygen plasma or no H_2O vapor heat treatments, TFTs had very low drain current with a high threshold voltage because of high density of defect states in silicon films, as shown by transfer characteristics (a) in Fig. 4. The H_2O vapor heat treatment applied to TFTs increased the drain current 10^3 times compared with no treatment case, as shown by (b) in Fig.4. This means that H_2O molecules incorporated into silicon and SiO_2/Si interface and effectively reduced the density of defect states through Al gate metals and SiO_2 gate insulators. When polycrystalline silicon films were annealed in H_2O vapor, the drain current further increased and had sharp subthreshold characteristics with 0.17 V/decade in the case of H_2O vapor annealing after TFT fabrication as shown by (c). Combination of oxygen plasma treatment followed by H_2O vapor heat treatment to polycrystalline silicon films further increased drain current shown by (d) in Fig.4. The high carrier mobility resulted from reduction of tail-type defect states as well as deep level type defect states. These experimental results show the importance of interface and

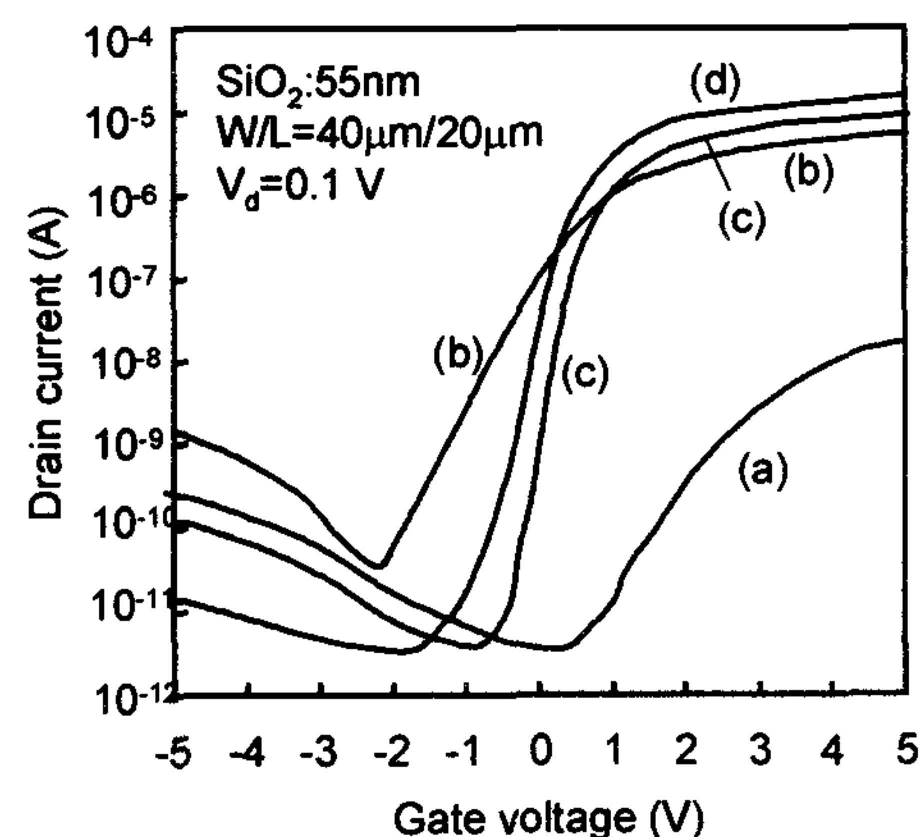

Fig. 4 Transfer characteristics for TFTs fabricated with no oxygen plasma or no H_2O vapor heat treatments (a), H_2O vapor heat treatment after TFT fabrication (b), H_2O vapor heat treatment applied to poly-Si and after TFT fabrication and additional H_2O vapor heat treatment (c), and oxygen plasma and H_2O vapor heat treatment applied to poly-Si and H_2O vapor heat treatment applied after TFT fabrication (d).

boundary passivation for fabrication of TFTs with a high carrier mobility and a low threshold voltage in polycrystalline silicon films with small crystalline grains.

Figure 5 shows the threshold voltage of the drain current and the maximum transconductance (G_m) as a function of laser energy for crystallization from 265 to 295 mJ/cm^2 for combination of oxygen plasma and H_2O vapor heat treatment applied to poly-Si and H_2O vapor heat treatment applied after TFT fabrication. The threshold voltage of the drain current distributed between 1.1 and 1.3 V. The low threshold voltage resulted from the low density of defect states. A high G_m of 5.2x10^{-6} S/sq was obtained for 285 mJ/cm^2 laser crystallization at a drain voltage of 0.1 V. The high Gm gave an effective carrier mobility of 650 cm^2/Vs.

The density of defect states in polycrystalline silicon films in the channel region was analyzed using a numerical calculation program used with finite-element method combined with statistical thermodynamical conditions. The best agreement of calculated transfer characteristics to experimental ones resulted in the defect states. The H_2O vapor heat treatment to silicon and after TFT fabrication reduced the density of defect states to 4.2x10^{11} cm^{-2}.

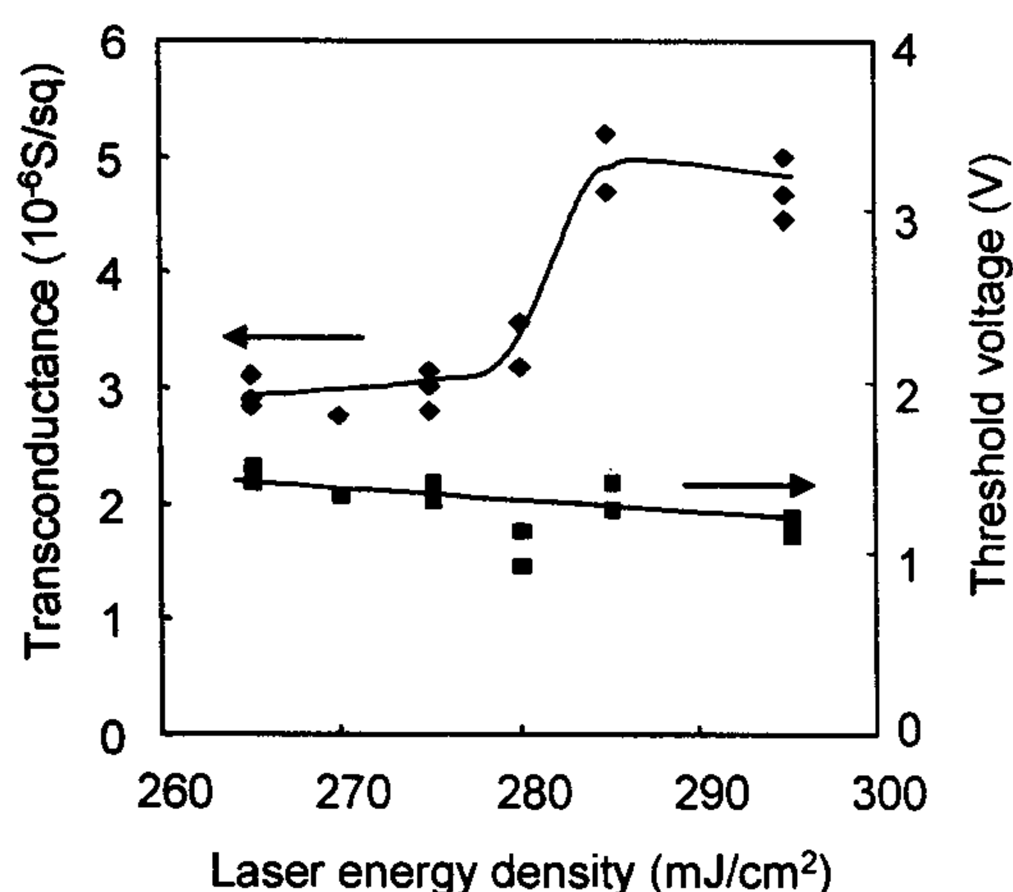

Fig. 5 The threshold voltage of the drain current and the maximum transconductance (V_d=0.1V) as a function of laser energy for crystallization from 265 to 295 mJ/cm^2 for combination of oxygen plasma and H_2O vapor heat treatment applied to poly-Si and H_2O vapor heat treatment applied after TFT fabrication.

6. Summary

Crystallization of silicon films at low processing temperature was reviewed. Rapid melt followed by solidification resulted in crystallization with low energy irradiation. This is an essential advantage of laser crystallization method for its application to TFT fabrication at a low temperature. Metal induced crystallization and joule heating crystallization are also interesting for low cost processing. Structural and electrical properties of laser crystallized poly-Si were characterized. Although crystalline grains were small 50~200 nm in pulsed laser crystallized silicon films, free carrier optical absorption analyses revealed that they had few defects and a high carrier mobility. Disordered region of electronic states were concentrated at grain boundaries. SiGe has a possibility of reduction of disordered region at grain boundaries. The crystalline silicon films had a high density of defects ~10^{18} cm^{-3} at grain boundaries. Oxygen plasma at 250°C and 1.3x10^6-Pa H_2O vapor heat treatments at 260°C effectively reduced the density of defect states to on the order of 10^{16} cm^{-3}. TFTs with a high mobility have been reported in many technical papers. We demonstrated poly-Si TFTs with high performance using defect reduction methods. A high carrier mobility of 650 cm^2/Vs and a low threshold voltage of 1.1 V were achieved by 260°C processing with oxygen plasma and high pressure H_2O vapor heat treatment. .

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8. References

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