A New High-Voltage Generator for the Semiconductor Chip

Phil Jung Kim*, Dae Sung Ku**, Sin Young Choi*, Lae Seong Jeong**, Dong Hyun Yang**, and Jong Bin Kim**

* Dept of Internet Information, Sunghwa College, Chunnam, 527-812, Korea
Tel : +82-61-430-5239 Fax : +82-61-430-5001 E-mail: philjung@sunghwa.ac.kr
**Dept of Electronic Engineering, Chosun University, Kwangju, 501-759, Korea
Tel : +82-62-230-7062 Fax : +82-62-232-3369 E-mail: kds-999@orgio.net

Abstract: A high-voltage generator is used to program the anti-fuse of the semiconductor chip. A new high-voltage generator consists of PN diodes and new stack type capacitors. An oscillator supply pulses to the high-voltage generator. The pulse period of the oscillator is delayed by controlling gate-voltage of the MOS. The pulse period is about 27ns, therefore the pulse frequency is about 37MHz. The threshold voltage of PN diode is about 0.8V. The capacitance of new stack type capacitor is about 4pF. The output voltage of the new high-voltage generator is about 7.9V and its current capacity is about 488μA.

High-voltage, Generator, Anti-fuse, Semiconductor Chip, PN Diodes, Capacitor, Oscillator, MOS

1. INTRODUCTION

Over the last years, the semiconductor chip has evolved into a high-density device, but it has required high technology and it has increase area of chip per a wafer, also the total cost has increased by decreasing yield. The yield of the semiconductor chip is decreasing by the increased area and the defected cells. The chip operation is unstable by defective cell and than disused all.

To solve this problem, a repair method used to replace some defective cell by redundant one. As conventional repair method, a poly-fuse cutting method using the laser is ease and simple circuit construction.[1,2] This method can repair at the wafer level but can't at the package or the module.

An electrical repair method also can repair at the package or the module, An electrical repair method also can repair at the package or the module, and it use anti-fuses that constructed with electrode/insulator/ electrode.[1] This method is generated rupture of insulator by supplying high voltage to an anti-fuse. Anti-fuse rupture voltage is called program voltage, generally its voltage is about 7-12V.[3]

In this paper, A new high-voltage generator consist of the isolated well PN diodes and the stack type capacitors to supplies high voltage to the anti-fuse electrodes without special pin and pad.[4,5] An oscillator supply pulse to a high voltage generator.

2. CIRCUIT DESIGN

Figure 1 is oscillator to supply periodical clock pulse to high voltage generator. This oscillator consisted of 3 parts. The first part is voltage divider and second part is main oscillation circuit and the last part is output buffer. When pgm, anti-fuse program signal, is logic 'high', oscillator start operation.

The voltage divider supply below source-voltage (Vcc) to PMOS gates and supply upper ground-voltage (gnd) to NMOS gates at main oscillation part to increase period of clock pulse. Voltage of MOS gate control current velocity and control period of oscillation. If pgm signal is logic 'low', than PMOS is off and NMOS is on. Thus, the voltage of refb node is Vcc-Vtp and ref node is 0V. Vtp is threshold voltage of PMOS. If pgm signal is logic 'high', than the voltage of refb node is below Vcc-Vtp and ref node is upper Vtn(threshold voltage of NMOS).

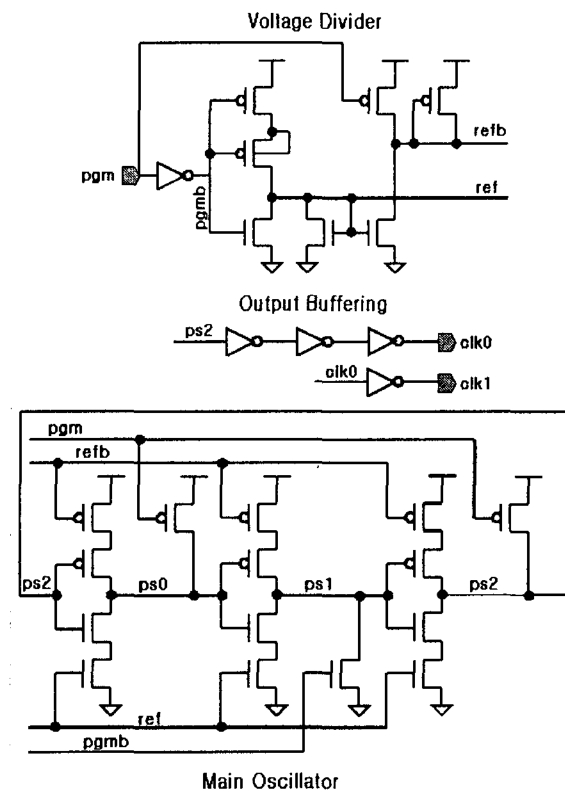

Fig. 1. Oscillator.

At main oscillation part, period is controlled by ref

voltage, refb voltage and MOS size. The number of Inverter is odd and the last output (ps2 node) feedback to input of the first inverter. Thus, output repeat 'high' and 'low' level. Width of MOS transistors are small size, therefore can't supply enough charge to high voltage generator. Thus, it is necessary that output buffered to increase drivability. Buffer size is each of 2.5 to 3 times. Output signals of clk0 and clk1 are phase difference of 180°.

Figure 2 is high voltage generator. The voltage generator consists of isolated-well PN diode and stacked comb-type capacitor. When pgm signal is logic 'high', source voltage (Vcc) through pass Vcc-Vtn to n01 node, and this voltage through pass Vcc-(Vtn+Vtd) to n02 node, and Vcc through pass Vcc-Vtd to output (Vpgm) by diode d4. When clk0 pulse and clk1 pulse of oscillator alternately input between logic 'high' and 'low', charges are pumped to each nodes by capacitor c1, c2. Each of node voltage is added as much as Vcc and it pass to next node by diode. Vtd is threshold voltage of diode.

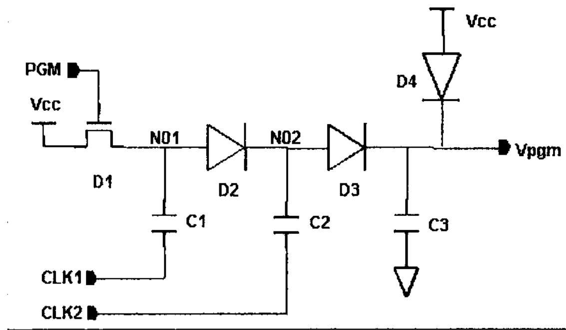

Fig. 2. The new high-voltage generator.

$$n01 = Vcc - Vtn \sim 2Vcc - Vtn \quad (1)$$
$$n02 = 3Vcc - (Vtn + Vtd) \sim 3Vcc - (Vtn + Vtd) \quad (2)$$
$$Vpgm = 3Vcc - (Vtn + 2Vtd) \quad (3)$$

Figure 3 is structure of PN diode. Size of p-type junction (p+) and n-type junction (n+) is $2\times1um^2$, p-well size is $5\times5um^2$, n-well width is 2.5um. Breakdown voltage of MOS diode is below PN diode's and Vtn is increasing in operation.

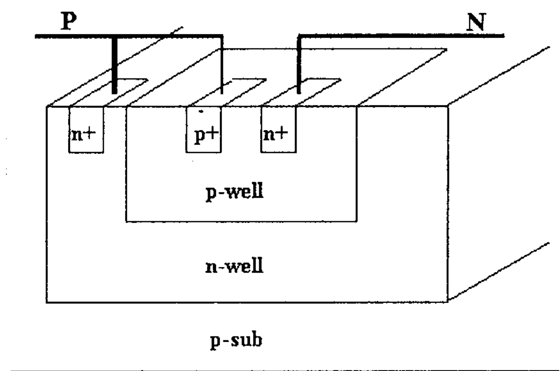

Fig. 3. Cross-sectional view of isolated-well PN diode.

Figure 4 is stacked comb-type capacitor. Electrodes of capacitor consist of n-well, poly1, poly2, metal1, and metal2. Insulator between electrodes are FOX(field oxide), IPO(inter-piranha oxide), BPSG(boro-phospho-siliciate glass), IMO(inter-metal oxide), and SOG(spin-on-glass).

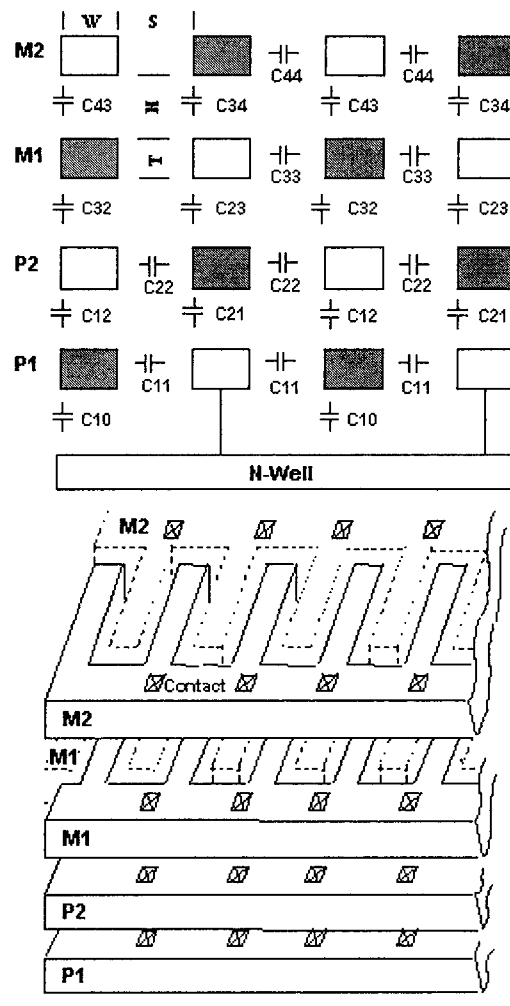

Fig. 4. Cross-sectional view of stack type capacitor.

Capacitances of designed capacitor are counted using J-H Chern's equation. Capacitance per area is given below:

$$CT = n \times l \times Ct \quad (4)$$

Where n is the number of branch of capacitor, l is length of branch. Ct is total capacitance of the sum of line-to-ground capacitance and line-to-line capacitance. Area of capacitor is given below:

$$Ac = a \times b$$
$$= [2 \times n \times W + (2 \times n - 1) \times S] \times (l + 2W + 2S) \quad (5)$$

Where a, b are length and breadth. W is width of metal line, S is space between parallel metal lines, H is thickness of dielectric layer between layers and T is thickness of metal line. If n = 100 and l = 50um, than CT is about 4pF. If W = 0.5um and S = 0.54um, than Ac is about $208 \times 52um^2$.

Loading capacitor is connected between output and gnd, it is necessary to decrease the amplitude of output Vpgm. Output current capacity of high voltage

generator is given below:

$$I = CT \times V \times f \quad (6)$$

Where CT is capacitance of capacitor, V is voltage of clock pulse and f is frequency of clock pulse.

3. RESULTS

In simulated results of oscillator, ref node voltage is 2.15V, refb node voltage is 0.99V, and its period is 27ns for condition with Vcc = 3.3V and temp. = 25°C. Thus clock frequency is about 37MHz. Figure 5 shows the simulated results of oscillator with temperature variation.

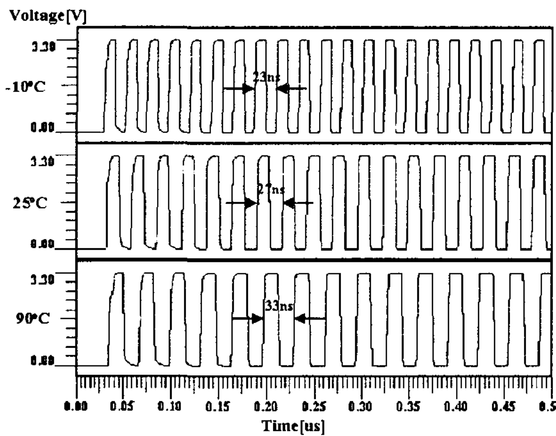

Fig. 5. Simulated results of oscillator with temperature.

The measurement voltage of PN diode sweep 0V to 3V, and the current compliance is 20mA. The threshold voltage is measured as about 0.8V, shown in figure 6. In the results, the threshold voltage of PN diode upper MOS diode's one with 0.65~0.7V because of p+ junction and n+ junction directly connected not and the resistance of p-well are comparatively high. If expression (1)~(3) substitute 0.8V by Vtd, than each of node voltage be shown below :

$$n01 = 2.65V \sim 5.95V \quad (7)$$

$$n02 = 5.15V \sim 8.45V \quad (8)$$

$$Vpgm = 7.65V \quad (9)$$

Where Vtn is 0.65V, Vcc is 3.3V.

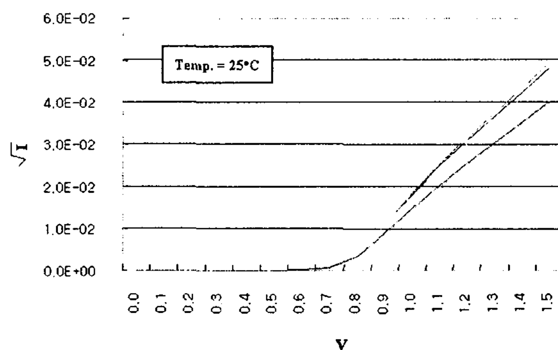

Fig. 6. I-V characteristics of PN diode.

In the simulated results of high-voltage generator, n01 node voltage is 2.17V~5.48V, n02 voltage is 5.03~8.33V, Vpgm is 7.93V. This results almost same as expected voltage within the range of 0.5V. Current capacity of the voltage generator be shown below by expression (6) ;

$$I = (4 \times 10^{-12}F) \times 3.3V \times (37 \times 10^{6}Hz) = 488.4uA \quad (10)$$

Figure 7 shows the simulated results of high-voltage generator.

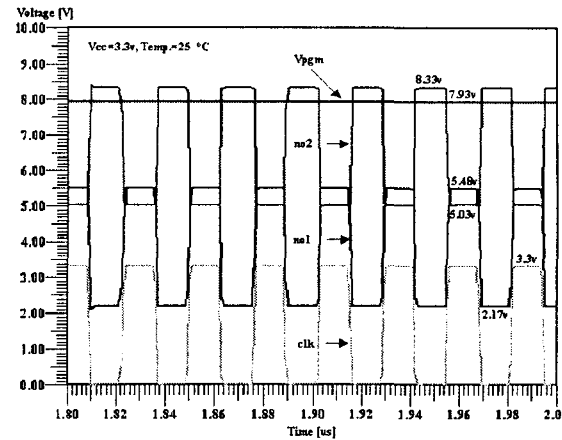

Fig. 7. Simulated results of oscillator with temperature.

Table 1 shows the simulated results of high-voltage generator with temperature variation. The difference of output voltage is about 0.6V with temperature.

Table 1. Simulated results of high-voltage generator with temperature (Vcc=3.3V).

Temp.	N01 node[V]	N02 node[V]	Vpgm[V]
-10°C	2.14~5.45	4.93~8.23	7.75
25°C	2.17~5.48	5.03~8.33	7.93
90°C	2.21~5.53	5.28~8.58	8.34

Figure 8 shows the measured output voltage of the new high-voltage generator. The Vpgm voltage is about 7.3V for the measured region with Vcc=3.3V.

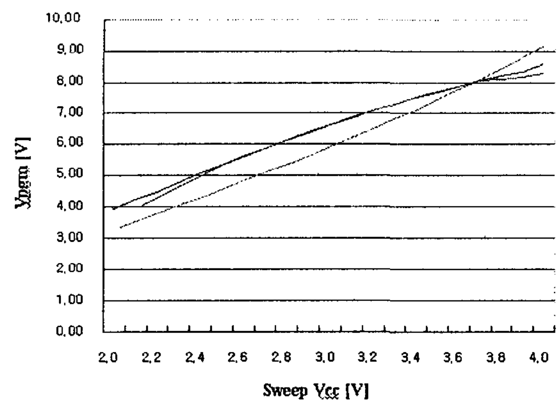

Fig. 8. Measured results of high-voltage generator.

4. CONCLUSIONS

The new high-voltage generator for anti-fuse program

does not require any modification to the DRAM process. The actual area penalty incurred by the use of this circuitry is small. The output voltage is enough to program anti-fuse and it is demonstrated in 64Mb SDRAM. Thus yield of chip will be increased by the use of electrical repair method with this circuitry. We believe that the new high-voltage generator will apply to SOC (System On Chip) and another semiconductor chip.

References

[1] G. Zhang, C. Hu, and et al., "Reliable Metal-to-Metal Oxide Antifuses", IDEM 94, pp. 281-284, 1994.

[2] Zheng Cui, Philip D. Prewett, and John G. Watson, "Focused ion beam biased repair of conventional and phase shift masks", J. Vac. Sci. Technol. B, Vol. 14, No. 6, pp. 3942-3946, Nov. 1996.

[3] Todd A. Merritt, Kevin Duesman, "On-Chip Program Voltage Generator for Antifuse Repair", U.S. patent, No. 5604693, Feb. 1997.

[4] Jue-Hsien Chern, Jean Huang, and et al., "Multilevel Metal Capacitance Models For CAD Design Synthesis Systems", IEEE Electron Device Letters, Vol. 13, No. 1, pp. 32-34, Jan. 1992.

[5] Phil-Jung Kim, Joo-Sun Choi, and et al., "Antifuse EPROM Circuit for Field Programmable DRAM", IEEE Solid-State Circuits Conf., Vol. 43, pp. 406~ 407, Jan. 2000.