Design of High Efficiency CMOS Class E Power Amplifier for Bluetooth Applications

Seung-Hwan Chae*, Young-Shig Choi*, Hyuk-Hwan Choi*, Sung-Woo Kim*, Tae-Ha Kwon*
*Dept of Electronic, Computer and Telecommunication Eng., Pukyong National University,
Busan, 559-1, Korea
Tel : +82-51-620-6469 Fax : +82-51-620-6450 E-mail: siniso@hanmail.net,

Abstract: A two-stage Class E power amplifier operated at 2.44GHz is designed in 0.25-μm CMOS process for Class-1 Bluetooth application. The power amplifier employs class-E topology to exploit its soft-switching property for high efficiency. A preamplifier with common-mode configuration is used to drive the output-stage of Class-E type. The amplifier delivers 20-dBm output power with 70% PAE (power -added-efficiency) at 2-V supply voltage.

Keywords: Bluetooth, CMOS, Class E, High efficiency, Common-mode, Power amplifier.

1. INTRODUCTION

Commensurate with the proliferation of wireless communication systems is a constantly increasing demand for compact, low-cost, and low-power portable devices. This demand has promoted the pursuit of single-chip radio transceivers realized in a low-cost CMOS technology[1]-[3]. Today's power amplifiers are implemented in GaAs, HBT, LDMOS, BiCMOS, etc.,. However, more and more signal processing is done in CMOS. For this reason a single chip transceiver demands an integrated CMOS power amplifier. This paper describes a two-stage power amplifier with 20dBm output power for Bluetooth Class 1 applications. The power amplifier employs class-E topology to exploit its soft-switching property for high efficiency. Proposed power amplifier is two-stage configuration with a pre-amplifier and an output amplifier. The pre-amplifier and the output stage are a common-mode and a parallel configuration, respectively. In the proposed pre-amplifier configuration, transistors are used to increase its impedance for driving the output stage. The class-E topology is used as the configuration of output stage.

2. CLASS-E POWER AMPLIFIER

Switching-mode power amplifiers can theoretically achieve efficiency as high as 100%. A typical configuration of a class-E power amplifier is shown in Fig. 1. L1 acts as either a RF choke(RFC) or a finite dc-feed inductance[1]. C2 and L2 are designed to be a series LC resonator plus an excess inductance Lx at the frequency of interest. Resonator delivers fundamental signal of operating frequency as a sine waveform. Jx of reactance element changes output voltage and phase of voltage at the switch. C1 and Lx are designed so that the following conditions for a class-E power amplifier with high efficiency as shown in Fig 2.[1]

- voltage across the switch is kept low when the switch turns off;

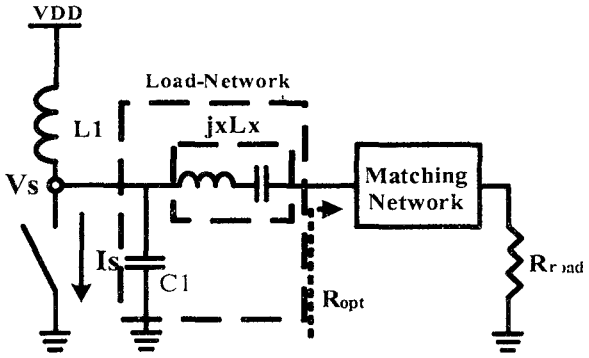

Figure 1. Typical schematic of a class-E power amplifier

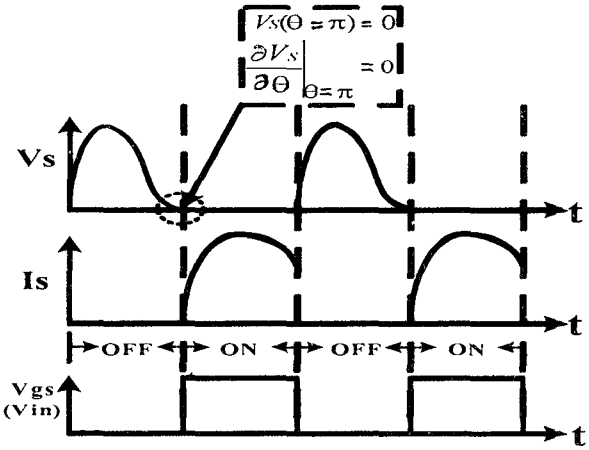

Figure 2. Voltage and current waveforms showing the soft switching characteristics in class-E power amplifier

- voltage across the switch is zero when the switch turns on;
- the first derivative of the voltage is zero when the switch turns on.

Component values shown in Fig 1. can be calculated using the following[2]:

$$Lx = \frac{\pi\, VDD^2(\pi^2 - 4)}{2\omega(\pi^2 + 4)} \qquad (1)$$

$$C1 = \frac{Pout}{\pi\omega VDD^2} \quad (2)$$

$$Rout = 0.577\frac{VDD^2}{Pout} \quad (3)$$

If the output network matches with 50 of load, power amplifier can not get desired output power. To get desired output power, output network should be matched with optimum R(Ropt).

3. PROPOSED POWER AMPLIFIER

Proposed common-mode power amplifier is shown in Fig 3. Proposed preamplifier of common mode configuration provides amplified signal to the output stage of parallel configuration. Common-mode configuration has the advantage of easy input matching due to the increased input impedance. Therefore, common-mode preamplifier is used as an input stage. In proposed structure, transistors(M5 and M6) are used to connect M2 and M3, and same phase input signal is applied to M1 and M4. This structure minimizes power loss in preamplifier and also makes its output signal as square wave as possible. It increases the overall efficiency of power amplifier. The transistors of M5, M6 with relatively small size of M1, M2, M3 and M4 compared to conventional preamplifier transistors increase the output impedance large enough to drive output stage. As the size of M5 and M6 becomes smaller, power loss is decreased in preamplifier. The size of transistor in preamplifier is M1~M4 : 196μm/0.25μm, M5~M6 : 210 μm/0.25μm. M5 ~ M6 operate as an on/off switch according to the drain voltage of M1 and M4. With the common-mode preamplifier, minimum voltage at drain of M1, M4 is larger than Vt of transistor in output-stage. L1 and L2 are used to lower minimum voltage at drain of M1, M4 than Vt of transistor in output-stage. The signal provided from the preamplifier switches the large output transistors close to ideal switching mode. Ldc1 and Ldc2 are RFC(RF choke inductor).

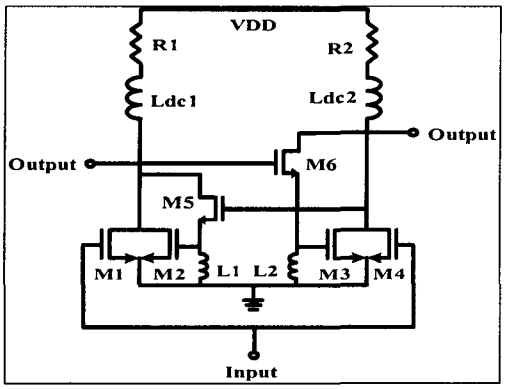

Figure 3. Proposed common-mode preamplifier.

R1 and R2 are used to suppress the possibility of oscillation and keep its output voltage lower than gate oxide breakdown voltage. Power consumption at R1 and R2 is small and does not degrade the overall power efficiency because their value is small. The whole circuit are parallel connected as shown in Fig 4.

This parallel configured output stage shows higher output power than single configured one. It makes the size of output transistors become smaller for the wanted output power, 20dBm, in comparison with other configurations. The size of both M1 and M2 is 1225μm. The input impedance of the whole power amplifier is 50 at 2.44GHz. Output matching network transformed into 11 to get output power of 20dBm. The frequency of X1 resonator is designed for Bluetooth which is operated at 2.44GHz.

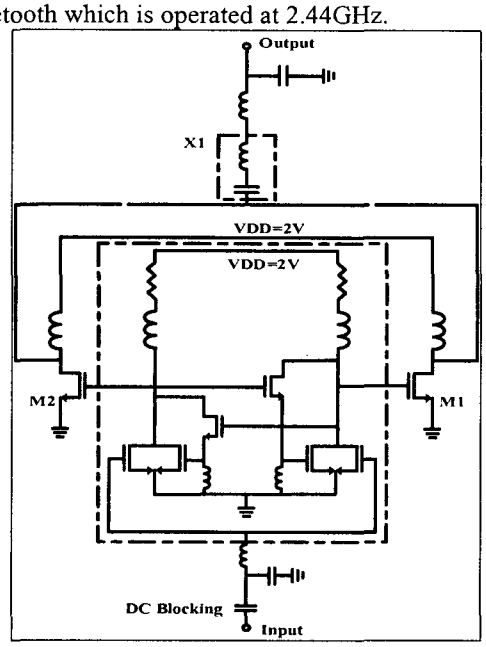

Figure 4. Complete schematic of the proposed power amplifier.

Fig 5 and Fig 6 are voltage and current waveforms of the designed two-stage power amplifier.

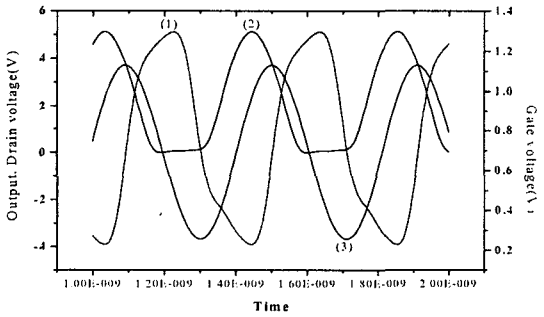

Figure 5. Simulated voltage waveforms of proposed power amplifier. (1) Gate voltage of M1. (2) Drain voltage of M1. (3) Output voltage of power amplifier.

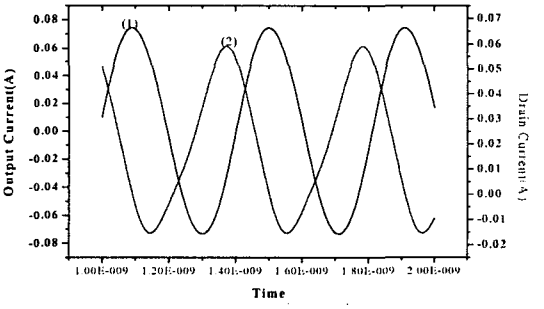

Figure 6. Simulated current waveforms of proposed power amplifier. (1) Output current of power amplifier (2) Drain current of M1

4. SIMULATION RESULTS

Fig 7 shows the simulated results of output power and power gain in the frequency range of the Bluetooth specification with 3dBm-input power. The power amplifier achieves 21dBm-output power and 18dB power gain at 2.44GHz. The simulated results of PAE (Power-Added-Efficiency) and DE(Drain-Efficiency) with input power of 3dBm are available in Fig. 8. The power amplifier achieves 70% PAE and 71% DE at 2.44GHz. The output power is kept at least 20dBm over the Bluetooth operating frequency range from 2.4 to 2.48GHz. The lowest PAE over the frequency range from 2.4 to 2.48Ghz is 65%. Fig 9 represents the simulated output power and power gain versus input power.

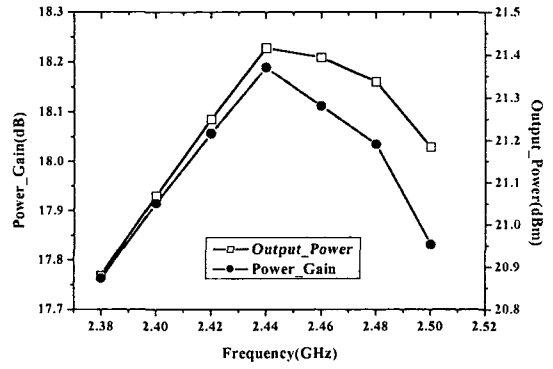

Figure 7. Output power and power gain(Gp) versus frequency.

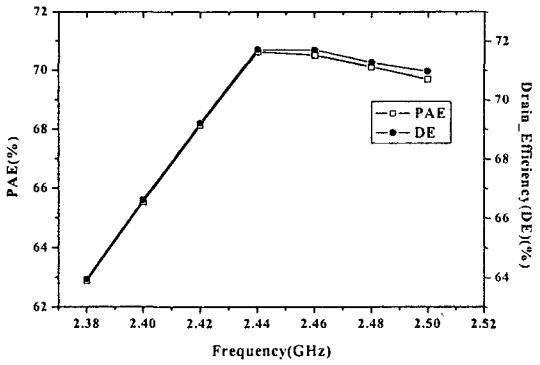

Figure 8. PAE and DE versus frequency.

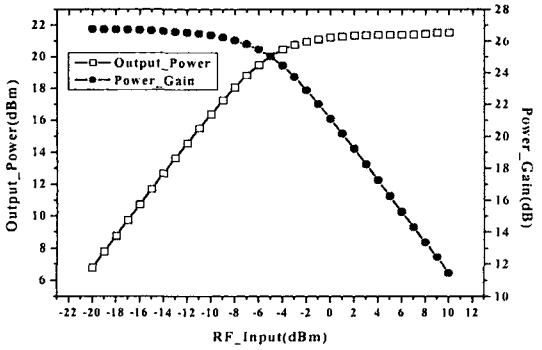

Figure 9. Output power and power gain versus input power.

Fig 10 shows how the PAE and DE changes with RF input power. A two-stage power amplifier with a new configuration is designed by using ADS simulator with 0.25um CMOS process parameters. Table 1 shows the key performances of the previously reported Bluetooth power amplifier with this work.

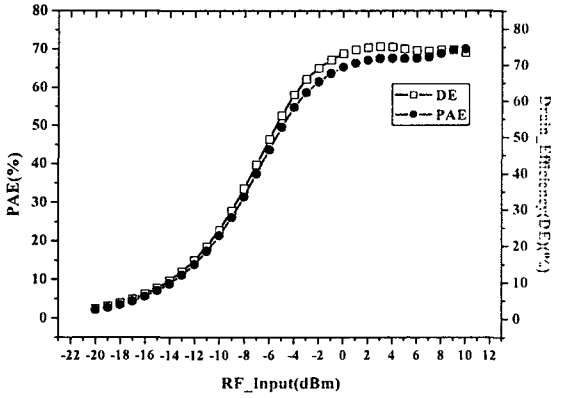

Figure 10. PAE and DE versus input power.

Table 1. Compares the key performance of the previously reported Bluetooth PA

Ref.	Tech.	VDD	Power	PAE	Class
[4]	0.25um	2.5	24dBm	48%	AB
[5]	0.18um	2.4	23dBm	42%	AB
[6]	0.24um	2.5	20dBm	31%	AB
[7]	0.35um	2.5	20dBm	59%	E
[8]	0.35um	1.2	20dBm	35%	E
This work	0.25um	2	21dBm	70%	E

5. CONCLUSIONS

A two-stage Class-E power amplifier operated at 2.44GHz is designed in 0.25-um CMOS process for Class-1 Bluetooth application. Proposed power amplifier with a new configuration achieves very high PAE over the Bluetooth operating frequency range from 2.4 to 2.48GHz. The power amplifier achieves 20dBm to 21dBm output power with PAE ranged from 65% to 70%, and power gain at 17dB to 18dB in the frequency range.

References

[1] Ka-Wai Ho; Luong, H.C."A 1-V CMOS power amplifier for Bluetooth applications" Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems A1 and A2, Conference name, p.780 (1999).

[2] Sokal, N.O., Sokal, A.D." Class E-A new class of high-efficiency tuned single-ended switching power amplifiers" Solid-State Circuits, IEEE Journal of , Volume: 10 , Issue: 3 , Jun 1975 Pages:168 – 176

[3] Steve Hung-Lung Tu and Chris Toumazou, "Highly Efficient CMOS Class E power amplifiers for Wireless Communications" Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on , Volume: 3 , 31 May-3 june 1998 Page(s): 530 -533 vol.3

[4] V. R. Vathula, T. sowlati and D. Leenaerts, "Class 1 Bluetooth Power amplifier with 24 dBm Output power and 48% PAE at 2.4GHz in 0.25um CMOS," Philips Research-USA.

[5] T. Sowlati and D. Leenaerts, "A 2,4 GHz 0.18um CMOS Self-Biased Cascode Power amplifier with 23dBm Output power" Philips Research-USA.

[6] Y. Emary Chen, Yong kyn.Yoon, Joy Laskar, and Mark Allen, "A 2.4 GHz Integrated CMOS Power Amplifier with Micromachined Inductors" IEEE MTT-S international, Vol. 1, 2001.

[7] Chen, E.; Heo, D.; Hamai, M.; Laskar, J.; Bien, D." 0.24-um CMOS technology for Bluetooth power applications" Radio and Wireless Conference, 2000. RAWCON 2000. 2000 IEEE , 10-13 Sept. 2000 Pages:163 - 166

[8] Ho, K.W.; Luong, H.C. "A 1V CMOS power amplifier for Bluetooth applications" Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 2 , 4-7 Aug. 2002 Pages:II-457 - II-460 vol.2