dB-Linear Function Circuit Using Composite NMOS Transistor

Hoang-Nam Duong(*) and Quoc-Hoang Duong(**)

(*) Hanoi University of Communications and Transports, Hanoi, Vietnam.
Email: duongnamgt@yahoo.com

(**) Information and Communication University, 119 Mujiro, Yuseong-gu, Daejeon, South Korea
Email: Hoang@icu.ac.kr Tel. (82-42) 866 6293

Abstract: In this paper, the design of a CMOS exponential V-I converter (EVIC,) based on Taylor's concept, is presented. The composite NMOS transistor is used for realizing the exponential characteristics. In a 0.25 μm CMOS process, the simulations show more than 20 dB output current range and 15 dB linear range with the linearity error less than ± 0.5 dB. The power dissipation is less than 0.3 mW with ± 1.5 V supply voltage. The proposed EVIC can be used for the design of an extremely low-voltage and low-power variable gain amplifier (VGA) and automatic gain control (AGC).

1. INTRODUCTION

Power consumption is a key limitation in many high-speed and high-data-rate electronic appliance systems today, ranging from mobile telecom to portable and desktop computing systems, especially when moving to nanometer technologies where leakage power starts to dominate. Power is also a showstopper for many emerging applications like ambient intelligent and sensor networks, some of which are powered autonomously. With the advances in the CMOS VLSI technology and CMOS digital signal processing technique, CMOS became a main fabrication process for analog and mixed signal processing circuitry. Consequently, new design techniques and design methodologies are needed to control and limit this power consumption.

The dB-linear V-I converter is the key component for the design of VGAs and AGCs, which are widely used in analog signal processing; such as in hearing aids, disk drive, and telecommunication applications [1-3]. This converter is not available in CMOS technology since CMOS transistors follow a square-law characteristic in strong inversion. Although CMOS transistors exhibit exponential characteristics in weak inversion, except the very low-speed application, the circuit could be too slow. Differently, the bipolar transistors are presented by exponential characteristics such that bipolar transistors are suitable candidates for the design of dB-linear function generators. Unfortunately, the bipolar techniques for VGAs and AGCs are not compatible for monolithic low-voltage CMOS-based analog and mixed-signal circuits. Moreover, good performance bipolar transistors are not readily available in the conventional technology, while BiCMOS solution may not be cost effective. Therefore, to generate exponential characteristics, two following methods are used. The first one is based on a "pseudo-exponential" generator [1-4] in which the exponential characteristics can be approximated as

$$e^{2ax} \cong \frac{1+ax}{1-ax} \qquad (1)$$

where a and x are the coefficient and the independent variable, respectively. The second method uses Taylor series expansion for realizing the exponential characteristics [5-7] in which the exponential characteristic can be expressed as

$$\exp(ax) = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \ldots + \frac{a^n}{n!}x^n + \ldots \qquad (2)$$

By applying the Taylor concept, the dB-linear V-I converter (EVIC) can be implemented by using the composition of a V-I squarer circuit, a linear V-I converter and a constant bias current [5,6], or by using composite NMOS transistors [7]. However, these previously reported EVICs tend to show very small dB-linear variation of the output current (less than 15 dB with a linearity error less than ± 0.5 dB) while consumes very high power (≅ 0.9 mW) [6,7]. Although the circuit in [7] is rather simple, the reported dB-linear range is limited to only 15 dB range, and the input voltage dynamic ranges are critically restricted.

In this paper, the circuit as in [7] is used. However, with some new modifications, the new circuit can increase the output dynamic range from 15

dB to nearly 25 dB, and the input dynamic range is widen drastically. Moreover, with the use of new approximation method, the dB-linear range is extended. The Simulation results will be given to verify the validity of this approach.

2. BASIC CONCEPT

From the Taylor's series expansion as expressed in Eq. (2). It is obviously that for $|ax| \geq 1$ the exponential function cannot be implemented by a low-order polynomial. The exponential function can be approximated with small deviation from the ideal exponential function by eliminating the higher order terms for $|ax| << 1$. By neglecting the terms higher than second-order in Eq. (1), the approximation equation can be given as.

$$\exp(ax) = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \qquad (3)$$

for $|ax| \leq 1$, Eq. (2) provides 14 dB variation and 12 dB-linear variation with the error less than ± 0.5 dB. Fig. 1 show the comparison between the two methods stated above and the ideal exponential function for $a = 1$.

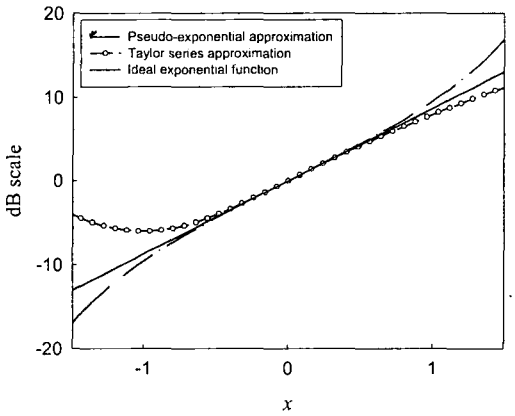

Figure 1. Comparison between the Ideal exponential function and the approximation function in Eq. (1) and (3).

Typically, the "pseudo-exponential" generator is of particular interest since it provides larger dB-linear range (about 15 dB with the error < ± 0.5 dB as shown in Fig. 2 by the diamond's symbol line) compared to that of the other one. Unfortunately, the "pseudo-exponential" method in which the exponential function is expressed as: $\exp(2x) \cong (1+x)/(1-x)$ is difficultly implemented due to the requirement of division function. Differently, the approximation function based on Taylor series expansion follows a squaring function and comprises only additive functions as shown in Eq. (2). Moreover, the CMOS transistors have square-law characteristics in strong inversion. Consequently, the approximation based on Taylor series expansion can be easily implemented in CMOS technology. Although this method results in small dB-linear output current range, its simplicity is still attractive to CMOS circuit designers. This paper used the new modified Taylor series approximation as follows [5]:

$$\exp(ax) \cong k + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \qquad (4)$$
$$= k\left(1 + \frac{a}{k1!}x + \frac{a^2}{k2!}x^2\right)$$

For k = 1, Eq. (3) actually becomes Eq. (2). Using Matlab simulation tool for simulating Eq. (3), the results show that for k slightly less than 1, the approximation in Eq. (3) shows higher dB-linear range than that of Eq. (2). As shown in Fig. 2 by the o'symbol line for $k = 0.95$, the dB-linear range is extended to about 15 dB with linearity error less than ± 0.5 dB which is almost the same as the performance of the "Pseudo-exponential" approximation. While k decreases, the dB-linear ranges can be extended to even much higher values as depicted in Fig. 2 for $k = 0.9$ and 0.8.

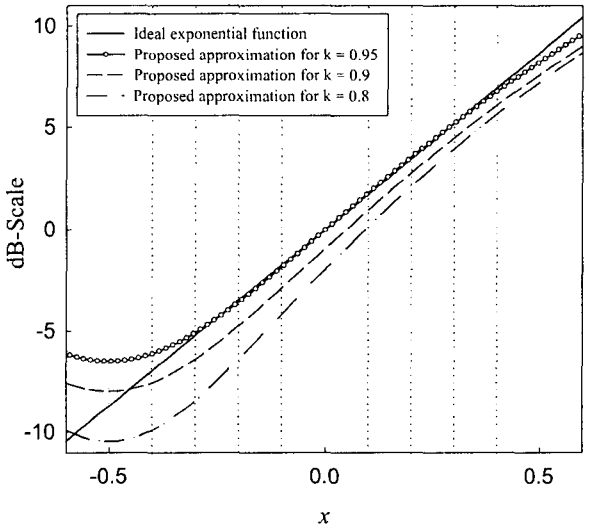

Figure 2. Plot of various functions on a decibel scale

3. CIRCUIT DESCRIPTION:

The circuit design is based on the composite NMOS transistor [8] as shown in Fig. 3 with the assumption that transistors M1 and M2 are identical

and operating in saturation region without body effects. The drain currents of M1 and M2 follows the below equations:

$$I_{d1} = \frac{K_n}{2}(V_{in} - V_Y - V_{tn})^2$$

$$I_{d2} = \frac{K_n}{2}(V_Y - V_1 - V_{tn})^2$$

where $K_n = \mu C_{ox} W/L$ is the process parameter and V_{tn} is the threshold voltage, V_{in} is the input voltage. The sum of these two currents leads to the following equation

$$I_{d1} + I_{d2} = \frac{K_n}{2}(V_{in} - V_Y - V_{tn})^2 + \frac{K_n}{2}(V_Y - V_1 - V_{tn})^2 \quad (4)$$

as reported in [4], if $V_Y = V_1/2$, then Eq. (4) can be written as

$$I_{d1} + I_{d2} = \frac{K_n}{2}\left(\frac{-V_1}{2} - V_{tn}\right)^2 \times \left(1 + \frac{V_{in}}{\left(\frac{-V_1}{2} - V_{tn}\right)} + \frac{V_{in}^2}{2\left(\frac{-V_1}{2} - V_{tn}\right)^2}\right) \quad (5)$$

Obviously, the output current, I_{out}, can be realized as an exponential approximation function of the input voltage, V_{in}, where the coefficient, a, is given as

$$a = \frac{1}{\left(\frac{-V_1}{2} - V_{tn}\right)} \quad (6)$$

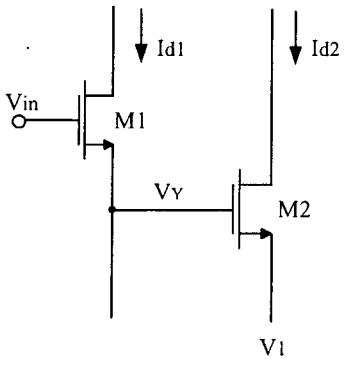

Figure 3. Composite NMOS transistor

The dB-linear V-I converter for realizing Eq. (5) is shown in Fig. 4 [7]. In Fig.4, the transistors M1 and M2 form the composite NMOS transistor, the two current mirrors, formed by transistors M3-M4 and M5-M6, insure that the drain current of M6 is equal to that of M5. Therefore, no current flows from node X to node Y. And, the gate voltage of M2, V_Y, is stabilized by two transistors, M7-M8. As in [7] two PMOS transistor with the aspect ratios of 100μm/1μm is used such that the power consumption is high. Differently, this paper uses one PMOS transistor, M8, with the aspect ratio of 40μm /1μm and another NMOS transistor, M7, with the aspect ratio of 2μm /1μm as shown in Fig.4 and Table. 1. The M7 has very small size so that the current flowing through these two transistors is very small. Consequently, the total power consumption is reduced extremely.

For the proposed converter to operate properly, all of the transistors should be biased in the saturation region. Theoretically, the input range of this circuit should be

$$V_Y + V_{tn1} \le V_{in} \le V_{dd} - |V_{tp4}| + V_{tn1} \quad (7)$$

where V_{tn1} and V_{tp4} are the threshold voltage of transistors M1 and M4. As shown in Eq. (7), the smaller the V_Y the lager the input voltage swing is. Therefore, the V_Y is chosen closely to $V_{ss} + V_{tn1}$ so that very wide input dynamic range is achieved.

4. SIMULATION RESULTS

The aspect ratios of all transistors in Fig. 4 are listed in Table 1. The simulation results are shown in Fig. 5. In Fig. 5, as V_{in} varies from –0.55 to 1 V, and I_0 = 14 μA, the approximation as in Eq. (2) is achieved with 12 dB range and the linearity error is less than ± 0.5 dB. By reducing I_0, the dB linear ranges are increased as depicted in Fig. 5 by the dash-dotted, dash-dot-dotted, and o'symbol lines. The o'symbol line which corresponding to I_0=6 μA, shows 17 dB linear range with linearity error less than ± 0.5 dB over large input voltage range from –0.55 V to 0.8 V. When Vin > 0.8 V, the simulation result deviates from the ideal line due to neglecting the higher order terms in Eq. (1).

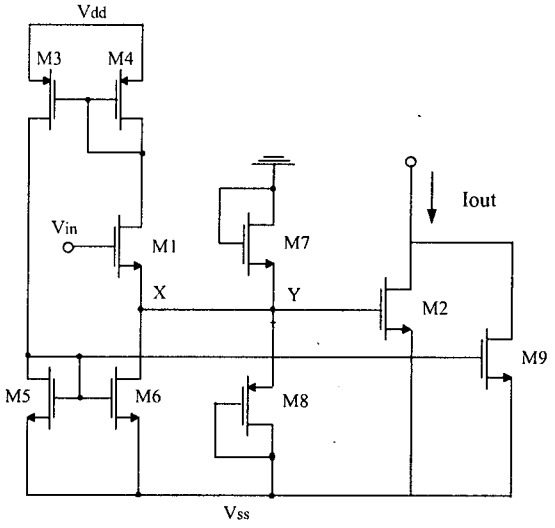

Figure 4. The proposed exponential V-I converter

5. CONCLUSION

A new dB-linear V-I converter based on the proposed modified Taylor series expansion is presented with the use of composite NMOS transistor. High dB-linear range (17 dB) over large input voltage swing (from –0.55V to 0.8V) is obtained with extremely low power consumption. The proposed circuit can operate at rather low supply voltage less than 3 V. However, the input voltage swing is proportional to the supply voltage. The circuit is compact and power-efficient. It could be used in the design of extremely low-voltage low-power VGA and AGC.

Table 1: Aspect ratios of transistors in Fig. 4.

Transistors	Aspect ratios μm/μm
M1, M2	1/4
M3, M4, M5, M6, M9	4/1
M7	2/1
M8	40/1

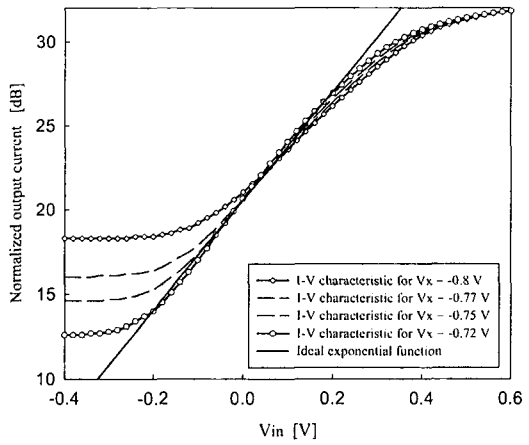

Figure 5. The I-V performance of the proposed EVIC shown in Figure 4

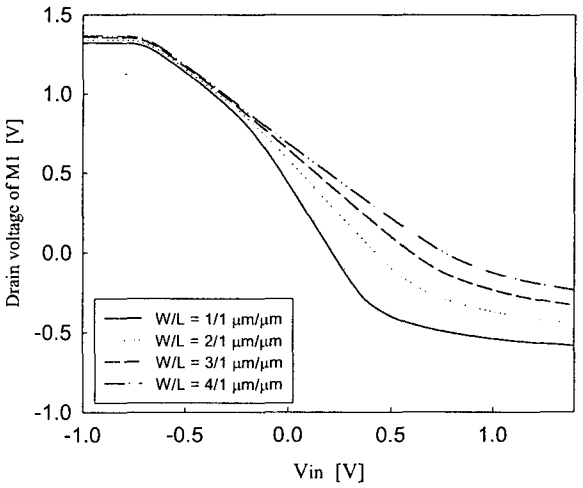

Figure 6. The I-V performance of the proposed EVIC shown in Figure for different W/L

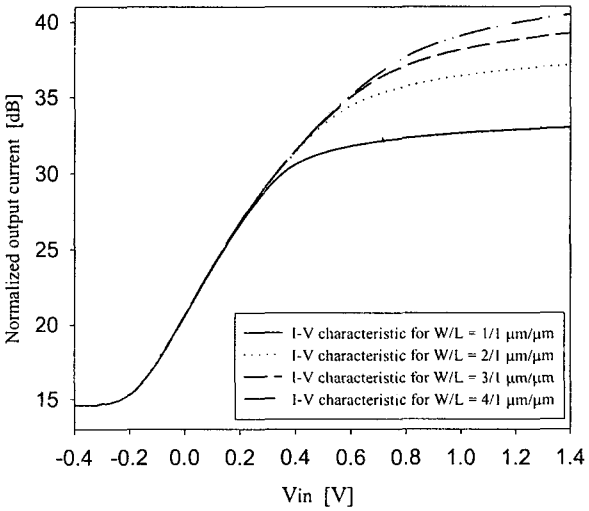

Figure 7. The I-V performance of the proposed EVIC shown in Figure for different W/L

References

[1] R. Harijani, "A Low-power CMOS VGA for 50 Mb/s Disk Drive Read Channels," *IEEE Trans. Circuits and Syst.* vol. 42, no. 6, pp. 370-376, June, 1995.

[2] K. M. Abdelfattah and A. M. Soliman, "Variable Gain Amplifier Based on a New Approximation Method to Realize the Exponential Function," *IEEE Trans. Circuits Syst.*, vol. 49, no. 9, Sep 2002.

[3] H. Elwan, A. M. Soliman, and M. Ismail, "A. digitally controlled dB-linear CMOS variable gain amplifier," *Elect. Lett.*, vol. 35, no.20, pp. 1725-1727, 1999.

[4] A. Motanemd, C. Hwang and M. Ismail, "CMOS exponential current-to-voltage converter," *Elect. Let.*, vol. 33, no. 12, pp. 998-1000, 5th June, 1997.

[5] Quoc-Hoang Duong, T.Kien N, and Sang-Gug Lee, "Low-Voltage Low-Power High dB-Linear CMOS Exponential Function Generator Using Highly-linear V-I Converter," will be presented at *IEEE International symposium on Low Power Electronics and Designs*, August 2003, South Korea.

[6] Lin, C., Pimenta, T., and Ismail, M., "Universal exponential function implementation using highly-linear CMOS V-I converters for dB-linear (AGC) application". *Proc. 1998 IEEE Midwest symp. Circuits and Systems*, 1999, pp. 360-363.

[7] W. Liu, C. Chang, and S. Liu, "Realisation of Exponential V-I Converter using composite NMOS transistors," *Elect. Let.*, vol. 36, no. 1, pp. 8-10, 6th Jan, 2000.

[8] K. Bult and H. Wallinga, "A Class of Analog CMOS Circuits Based on the Square-Law Characteristic of an MOS Transistor in Saturation," *IEEE J. of Solid-State Circuits*, vol. sc-22, no. 3, June 1987

Acknowledgement

The author would like to thank Mr. Quoc-Hoang Duong who is currently a Ph.d student at Information and Communications University; south Korea.