The design of a 32-bit Microprocessor for a Sequence Control using an Application Specification Integrated Circuit(ASIC) (ICEIC'04)

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Abstract: Programmable logic controller (PLC) is widely used in manufacturing system or process control. This paper presents the design of a 32-bit microprocessor for a sequence control using an Application Specification Integrated Circuit (ASIC). The 32-bit microprocessor was designed by a VHDL with top down method; the program memory was separated from the data memory for high speed execution of 274 specified sequence instructions. Therefore it was possible that sequence instructions could be operated at the same time during the instruction fetch cycle. And in order to reduce the instruction decoding time and the interface time of the data memory interface, an instruction code size was implemented by 32-bits. And the real time debugging as single step run, break point run was implemented. Pulse instruction, step controller, master controllers, BIN and BCD type arithmetic instructions, barrel shit instructions were implemented for many used in PLC system. The designed microprocessor was synthesized by the S1L50000 series which contains 70,000 gates with 0.65um technology of SEIKO EPSON. Finally, the benchmark was performed to show that designed 32-bit microprocessor has better performance than Q4A PLC of Mitsubishi Corporation.

Keyword: PLC, ASIC, VHDL, Sequence control, microprocessor, program memory, data memory, BCD, BIN, Q4A

1. INTRODUCTION

Sequential control is an elementary technology for manufacturing systems, and the development of programmable logic controllers is under the influence of computer's hardware and software technology. Recently, the models of personal computers are improved very fast and very frequently according as the progress of technology of Very Large Scale Integrated Circuit (VLSI) [1]. Because of the advancing VLSI technologies, both processors with fast and powerful numerical operation unit and large scale function network components can be easily designed and fabricated [2].

Programmable logic controllers have progressed rapidly since their insertion in the 1960's, and are nowadays widely used for process control in manufacturing facilities [3]. One key feature of the important industrial success of PLC's is high speed execution of sequence instructions. For this purpose, a new architecture for high performance programmable logic control was designed in [4].

Studies on the performance improvement of PLC have been carried out in the architecture of processor. Specific processors for the PLC have been developed to raise its performance using parallel processing methods or Application Specific Integrated Circuit (ASIC) [5, 6].

In this paper, we propose the design of a 32-bit microprocessor for a sequence control using an Application Specification Integrated Circuit (ASIC). The 32-bit microprocessor was designed by a VHDL with top down method; the program memory was separated from the data memory for high speed execution of 282 specified sequence instructions. Therefore it was possible that sequence instructions could be operated at the same time during the instruction fetch cycle. And in order to reduce the instruction decoding time and the interface time of the data memory interface, an instruction code size was implemented by fixed 32-bits with Harvard architecture.

And the real time debugging as single step run, break point run was implemented. Pulse instruction, step controller, master controllers, BIN and BCD type arithmetic instructions, barrel shit instructions were implemented for many used in PLC system.

The designed microprocessor was synthesized by the S1L50000 series which contains 100,000 gates with 0.65um technology of SEIKO EPSON.

Finally, the benchmark was performed to show that the designed 32-bit microprocessor has better performance than the Q4A PLC of Mitsubishi Corporation.

2. ARCHITECTURE OF A 32-BIT MICROPROCESSOR

As the basic architecture, the combination of a Harvard architecture, instruction cache, and RISC structure is considered. Because of the no latency of memory access caused by the simple bus interface, the microprocessor must separate the program memory bus from the data memory bus of the PLC system. For this reason bus confliction between instruction fetch and data access be avoided. To achieve effective data access, we adapt Harvard architecture with a 32-bit program memory bus and a 16-bit data bus in order to access at same time.

Fig. 1 shows the internal block diagram of the designed 32-bit microprocessor for a sequence logic controller.

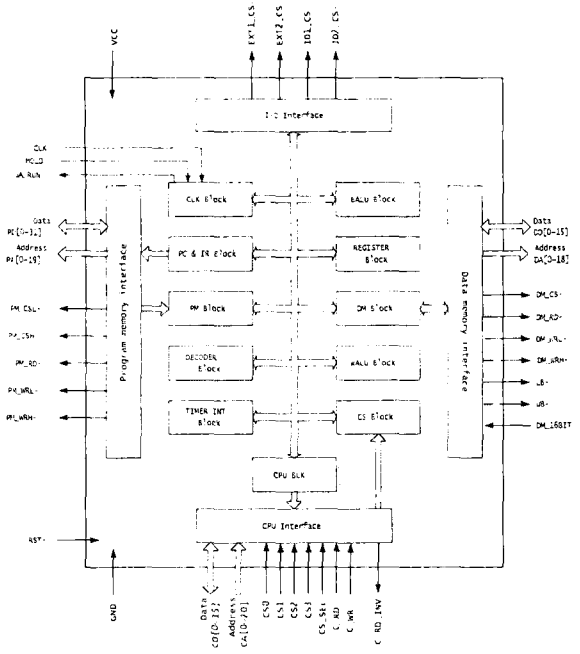

Fig. 1. The internal block diagram of the designed 32-bit microprocessor

As shown in Fig. 1, in the register block, registers include 16 general registers and 2 stack registers, MCS, MPP, MRD, Flag registers. The address buses of a general purposed processor are connected in CS block and these address buses are used to make selection signals in sequence controlling processor. In a PM block, to organize instruction register in 32-bit, two 16-bit memories are used and for this a write signal is divide to two signals. One is for high 16-bit access and the other for low 16-bit access.

In a DM block, DM_16BIT selects interface bus with 0 for 8bit and 1 for 16-bit memory interface. When an 8-bit interface is selected, to control high address and low address separately in write operation, two write signals DM_WRH and DM_WRL are used.

When 16-bit interface is selected, LB- and UB- are used to control high 8-bit and low 8-bit interface. In a CPU block, CS_SEL selects CS0, CS1, CS2 and CS3 that are decoded directly in a general purposed signal or CA that is not decoded. Timer interrupt block controls timer interrupt registers and makes jump to interrupt service routine when an interrupt is requested. In a CLK block, HOLD and GA_RUN that control bit and word processor are connected. When the HOLD is driven low, the bit and word processor when executes instructions driving GA_RUN high but if instructions are not executive, it hands over control to a general purposed processor with driving GA_RUN low. The processor shown in Fig. 1 has 20-bit PC basically and is stopped when HOLD is derived high. In this paper, the designed microprocessor is cooperated with a Super Hitachi MPU (SH7055-40MHz) in order to operate the advanced operations such as a communication to host computer, floating point calculations.

Also the external clock of 40 MHz is applied to generate internal clock and it has two ALUs. One is for bit processing and the other is for word processing.

A. Specification of instruction sets

The implemented instructions have two kinds, the one is Boolean instructions and the other is word type instructions. Each instruction has fixed 32-bit in order to simplify and reduce decoding time of instructions of Programmable Logic Controller.

31	30~23	22~4	3~0
p	Instruction kind	Bit address	Bit position

(a) Bit instruction format of direct addressing

31	30~23	22~4	7~4	3~0
p	Instruction kind	Don't care	Rd	Rs

(b) Bit instruction format of indirect addressing

31	30~24	23~20	19~0
p	Instruction kind	Reg.(R0~R15)	Addr.

(c) Word instruction : load/store of direct addressing

31	30~24	23~20	19~16	15~0
p	Instruction kind	Rs	Rd	*Ins. sub*

(d) Word instruction : arithmetic of register addressing

31	30~24	23~20	19~0
p	Instruction kind	Reg.(R0~R15)	Address

(e) Jump, call instruction

Fig. 2. Instruction formats of the designed 32-bit microprocessor

As shown in the Fig.2, p denotes multifunction bit which is used parity bit or step information of sequence instruction at compile codes. The *Ins. sub* in Fig.2 presents the subset of register type instructions. In case register address, the number of register are sixteen, and the size of all registers is 16-bit and also we can combine 32-bit from 2 registers. The data memory address range of bit or word instructions is one mega bytes.

B. Specification of the proposed processor

The specification of bit and word processor is shown in table 1. Bit instructions have 118-instruction and word instructions have 156-instructions respectively. And the internal bus of additions or subtracts and barrel shifts consist of 32-bit, but multiplier or divider instruction has 64-bit. The total memory size of program memory is 4 Mbytes and the data memory space has 1 Mbytes.

We have designed that the microprocessor well operated at 40 MHz. The execution time of internal basic operation such as ANB, ORB, MC, MCR, MPS,

MRD, MPP, INV is 75 ns, and the execution time for a memory interface instruction such as LD, ST is 100ns to 200ns according to data bus with 16-bits or 32-bits width.

There are needed a several debugging methods such as single step run that executes instructions step by step, PC break run that stops when PC equals to address where we want it to stop, and DM break run that stops when accessing data memory address where we want it to stop for high speed processing and debugging. These debugging methods have an advantage of actual state running it like real with debugging online.

Table 1. Specification of 32-bit micro processor

Bit operation instruction number		118
Word operation instruction number		156
Internal data BUS(add or sub/mul or div)		32/64
External program memory size		32bit x 1M
External data memory size		16bit x 512K
Access time of word instruction	Internal operation	75ns
	16bit external memory write	100ns
	32bit external memory read	125ns
	16bit external memory write	175ns
	32bit external memory read	200ns
Access time of bit instruction	Internal operation	75ns
	External data memory read or write of a 16-bit	100ns
	External data memory read and write of a 32-bit	175ns
Real time Debugger		1 Step run
		PC break
		DM break
Time driven interrupt		32bit Timer
Interface function of other MPU		RUN, STOP

3. SYNTHESIS AND IMPLEMENTATION OF ASIC

In this paper, such as program memory interface, data memory interface, decoder, I/O interface, bit ALU, word ALU, register blocks, and timer and real time debugging block, other MPU interface block, each module are described in VHDL. The designed microprocessor was synthesized by the S1L50000 series which contains 70,000 gates. The microprocessor has been fabricated using 0.65um CMOS technology of SEIKO EPSON.

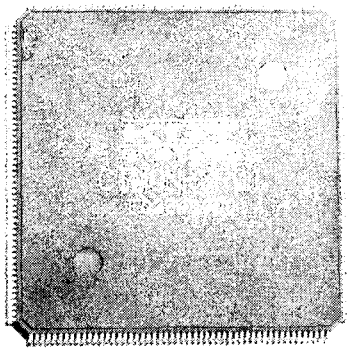

Fig. 3. Photograph of implemented ASIC.

The implemented chip is a QFP 208 pin, 0.5 mm pitch, and we also show a photograph of the ASIC in Fig. 3.

4. PERFORMANCE EVALUATION OF DESIGNED ASIC

We show the performance of the implemented 32-bit microprocessor in this paper. To evaluate the performance of bit and word processor through an experiment, we consist the system like that in figure 4. As shown in figure 4, the SH7055 is a general purposed 32-bit Super microprocessor of HITACHI company which executes floating point operation and digital input and digital output operation and is used to control ASIC and 40 MHz oscillator is used because it is appropriate to 38,400bps in serial communication.

A level shifting transceiver 74ALVC164245 is used to interface 3.3V with 5V as a buffer. The 55ns-CMOS SRAM is used as program memory and data memory with 1 to 5 uA backup current at power OFF. We respectively design input-output structure that read data from input card and output the processed data to output card after completing one scan of sequence control. And we also designed the assembler of microprocessor, debug tools with monitoring of internal variable in the C source.

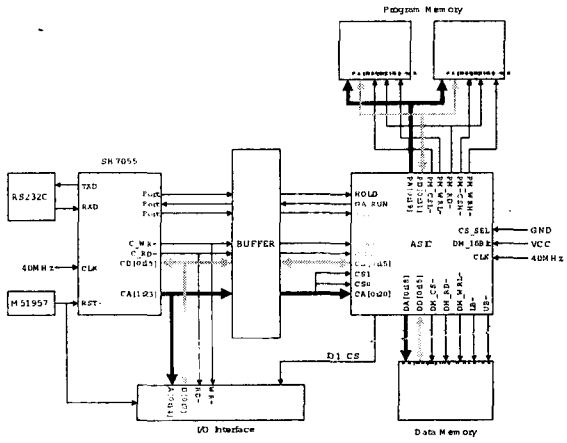

Fig. 4. Configuration for performance evaluation.

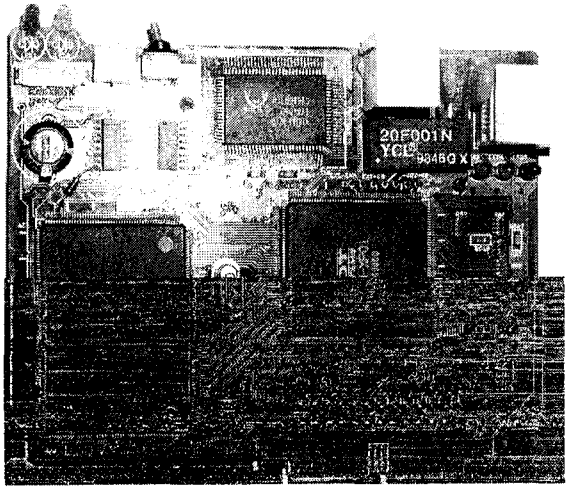

Fig. 5. Photograph for performance evaluation.

The result of experiment and comparing bit and word processor with Q4A of Mitsubishi is shown in table 2.

Table 2. Comparing designed processor with Q4A

Instruction kinds		Proposed processor	Q4A
ANB, ORB, MC, MCR, MPS, MRD, MPP, INV		75ns	75ns
LD, LDI, AND, ANI, OR, ORI, XOR		100ns	75ns
LDP, LDF, ANDP, ANDF, ORP, ORF, PLF, PLS		175ns	2.5us
MOV	16 bit	225ns	300ns
	32 bit	375ns	900ns
ADD, SUB	16 bit	600ns	1.0us
	32 bit	825ns	1.2us
MUL	16 bit	1.25us	1.1us
	32 bit	1.825us	7.5us
DIV	16 bit	1.25us	2.6us
	32 bit	1.825us	13.5us
BCD	16 bit	725ns	1.0us
	32 bit	1.05us	3.0us
BIN	16 bit	725ns	1.0us
	32 bit	1.05us	1.8uss
BCD ADD	16 bit	600ns	4.8us
	32 bit	825ns	1.2us
BCD SUB	16 bit	600ns	4.7us
	32 bit	825ns	1.2us
BCD MUL	16 bit	1.5us	3.6us
	32 bit	3.0us	23.0us
BCD DIV	16 bit	1.5us	3.6us
	32 bit	3.5us	26.0us
AND, OR, XOR	16 bit	600ns	3.6us
	32 bit	825ns	7.0us
ROL, ROR	16 bit	600ns	1.9us
	32 bit	825ns	3.9us
RCL, RCR	16 bit	600ns	1.5us
	32 bit	825ns	4.1us
JMP		300ns	3.0us

Successfully, to show the superiority of the processor proposed in this paper, we compared it with Q4A[7] of Mitsubishi PLC and verified that it is fast 14 times in pulse processing instruction and 2 times in word processing instruction.

5. CONCLUSIONS

In this paper, we designed bit and word processor for sequence control of PLC using ASIC. In design, we took Harvard Architecture to solve the problem of high speed processing, and RISC structure to fetch instruction and reduce a decoding time also for this we designed the logic with VHDL and simulated it with verilog XL.

The designed microprocessor was synthesized by the S1L50000 series which contains 70,000 gates with 0.65um technology of SEIKO EPSON. Finally, the benchmark was performed to show that designed 32-bit microprocessor has better performance than Q4A of Mitsubishi Corporation.

Specially, the BCD type and pulse type instruction instructions and the shift/rotate instructions have better high speed performance than Q4A of Mitsubishi Corporation.

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