SOI Image Sensor Removed Sources of Dark Current with Pinned Photodiode on Handle Wafer (ICEIC'04)

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Abstract: We fabricated a hybrid bulk/fully depleted silicon on insulator (FDSOI) complementary metal oxide semiconductor (CMOS) active pixel image sensor. The active pixel is comprised of reset and source follower transistors on the SOI seed wafer, while the pinned photodiode and readout gate and floating diffusion are fabricated on the SOI handle wafer after the removal of the buried oxide. The source of dark current is eliminated by hybrid bulk/FDSOI pixel structure between localized oxidation of silicon (LOCOS) and photodiode(PD). By using the low noise hybrid pixel structure, dark currents can be suppressed significantly. The pinned photodiode can also be optimized for quantum efficiency and reduce the noise of dark current. The spectral response of the pinned photodiode on the SOI handle wafer is very flat between 400 nm and 700 nm and the dark current that is higher than desired is about 10 nA/cm2 at a V_{DD} of 2 V.

SOI image sensor, pinned photodiode, APS, dark current

1. INTRODUCTION

In many imaging systems, integration of the image sensor with circuitry for both driving the image sensor and performing on-chip signal processing is becoming increasingly important. CMOS active pixel sensors (APS), fabricated using a standard CMOS process, have the advantage of low power consumption, low cost and a high level of integration. Due to intensive works over the past several years, the CMOS APS imagers are now considered as a visible alternative to charge-coupled device (CCD) in many application fields. Since they do not achieve the high quality image of CCD image sensors, however, they can be used only in applications that do not require high quality. They have difficulty in suppressing the dark current of the photodiode and fixed pattern noise (FPN).[1-2]

As the CMOS technologies are downscaled to deep sub micron eras, it becomes more difficult to fabricate the low dark current imagers. Dark current is the photodetector leakage current and reduce the charge capacity dedicated for photo-carriers. Moreover, this current component varies with the sensor location and time, producing the spatially varying and temporal variation of the output signals. The dark current levels reported for CMOS APS imagers in current technologies are still more than an order of magnitude larger than those of the CCD sensors with the optimal fabrication process.[3]

Silicon-on-insulator (SOI) technology has been proven to be advantageous in many applications. The sources of increased SOI performance are the elimination of area junction capacitance and that of body effect in bulk CMOS technology. As a result, image sensors that are built on SOI will find a useful application. To integrate image sensors on SOI substrate, however, suffers from low quantum efficiency (QE). Due to the limited depth of silicon available on the top film, most of the photons can pass through the sensing regions without being absorbed.[4] In this paper, we fabricated a hybrid bulk/fully depleted silicon on insulator (FDSOI) complementary metal oxide semiconductor (CMOS) active pixel image sensor (APS). The pixel circuit is a conventional four-transistor structure. The active pixel comprises of reset and source follower transistors on the SOI seed wafer, while the pinned photodiode, readout gate, and floating diffusion (FD) are fabricated on the SOI handle wafer. The source of dark current is eliminated by hybrid bulk/SOI pixel structure between localized oxidation of silicon (LOCOS) and photodiode (PD). Figure 1 shows sources of dark current. The employing pinned photodiode as a photodetector is also an easy and effective way of reducing the noise of dark current. The pinned photodiode on the SOI handle wafer can be optimized for quantum efficiency, because low handle wafer doping yields a large depletion width. The elimination of wells on the SOI seed wafer allows for the use of pMOSFET without increasing the pixel size.

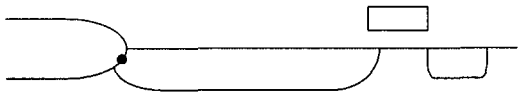
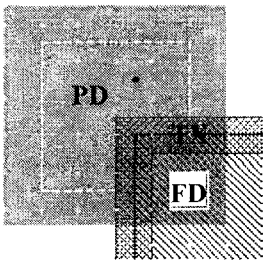


Fig. 1. Sources of dark current in general photodiode of CMOS active pixel image sensor (between photodiode and surface of silicon, between photodiode and local oxidation of silicon, between photodiode and bulk of silicon).

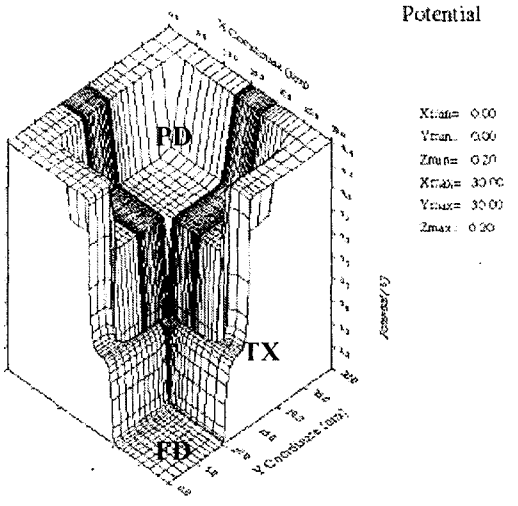
2. DESIGN AND EXPERIMENT

The hybrid bulk/FDSOI CMOS active pixel image sensor is fabricated on UNIBOND wafer with a seed wafer thickness of 0.1 μm and a buried oxide (BOX) thickness of 0.2 μm. The active pixel comprises of reset and source follower transistors on the SOI seed wafer, while the pinned photodiode, readout gate, and floating diffusion (FD) are fabricated on the SOI handle wafer. The photodiode is formed by an extra etching step with one extra mask to remove the buried oxide layer (BOX) on the SOI handle wafer. Readout gate and FD is also fabricated on the SOI handle wafer..

It is well known that employing a pinned photodiode as a photodiode is an easy and effective way to reduce the noise of dark current. We applied a pinned photodiode to the CMOS image sensor to reduce the surface dark current. With regard to the charge transfer efficiency, the pinned photodiode pattern layout is designed with a readout gate and floating diffusion, as shown in Fig. 2.[1] A hole accumulated layer located on the surface of the sensor, suppresses the dark current which becomes a minimum source of noise. A pinned photodiode simulation has been performed in order to understand the charge transfer efficiency of the readout gate by spectra. Figure 2 shows the simulated potential profile under the condition of a 3 V readout gate bias. There is no potential barrier along the charge transfer path from a pinned photodiode to FD.



(a)



(b)

Fig. 2. (a)Pinned photodiode (PD) layout with readout gate (TX) (b)Simulated potential profile of a pinned photodiode under the condition of 3 V readout gate bias (FD : floating diffusion)

The photodiode is formed by an extra etching step with one extra mask to remove the buried oxide layer (BOX) on the SOI handle wafer. Readout gate and FD is also fabricated on the SOI handle wafer. The photodiode structure of p+/n-well/p-sub has a shallow junction with the depletion depth and the absorption depth. The p+ region on the surface suppresses the noise caused by the interface traps located on the surface of the photodiode. The depth is controlled by an implantation process and drive-in time. Placing the photodiode in the handle wafer enables independent optimization of readout and photodiodes without introducing significant process complexities because each is implemented in separate silicon layers. This allows imager designs with low handle wafer doping for excellent photo response and low cross talk. The channel stop of the p-implant around the pinned photodiode and FD eliminates the Si-SiO_2 interface related dark current generation. The pinned photodiode pattern layout is fabricated on $N_A=7\times10^{14}$ cm^{-3} of handle wafer and the structure is shown in Fig. 3. The photodiode has an effective active dimension of 20 μm by 20 μm. FD is formed with n doping.

The leakage current origins of CMOS imagers are surface damage and dislocations near isolation regions. The isolation region is made of LOCOS or shallow trench isolation (STI). In CMOS image sensors, to attain process compatibility with a standard logic process, LOCOS or STI isolation exists in pixels.[5] In this paper, by using hybrid bulk/FDSOI structure, the source of dark current is removed between LOCOS and photodiode. The hybrid bulk/FDSOI process needs not a LOCOS process and is simpler than bulk image sensor process. Figure 3 shows the cross-sectional view of fabricated hybrid bulk/FD-SOI CMOS active one pixel image sensor placing the photodiode on the SOI handle wafer.

A conventional four-transistor pixel has a readout gate, a reset transistor, an amplification transistor, and a row address transistor. Figure 3 shows a four-transistor pixel circuit with a pinned photodiode and a signal chain just before an output circuit block. A readout gate is controlled by M1 and it transfers signal charges from a pinned photodiode to FD on the SOI handle wafer. M2 is the reset gate for FD, M3 is the source follower transistor, and M4 is the row select transistor. This is the meaning the level to upgrade to become to come out this order is the active the M2 and M3 sis sequence is continued at minutes time is shorter than bulk silicon. The reset transistor and source follower is formed on the SOI seed wafer and is fabricated by the conventional FDSOI process. The FDSOI nMOSFET has a W/L of 12 μm/5 μm. The transistor is designed with a rectangular active area, a gate, and contact holes. FDSOI processing is simpler than bulk or partially-depleted (PD) SOI, that at least one mask step is saved, and can be scaled down without LOCOS process. FDSOI CMOS characteristically achieves low-power operation because of its very thin depleted channel and reduced device parasitic capacitances. The buried oxide isolation limits crosstalk between the bulk sensor and the

CMOS circuitry, and also permits the bulk wafer resistivity to be tailored to the imaging requirement.[4]

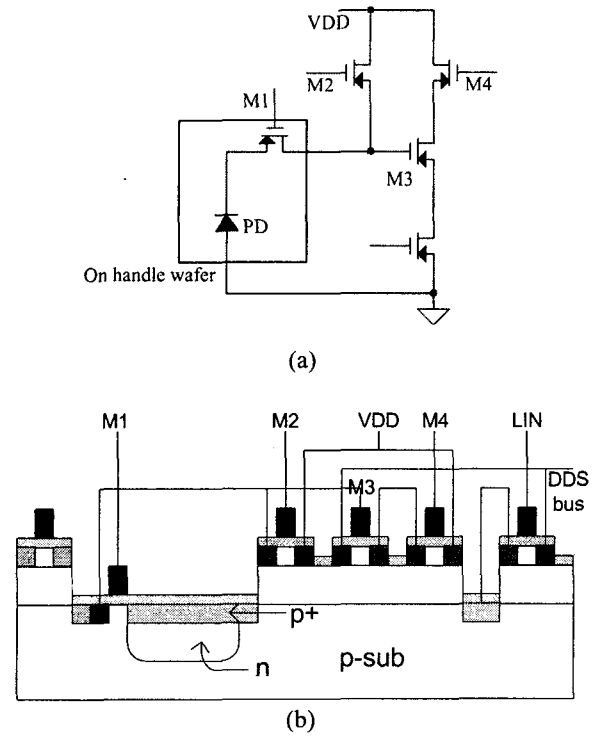


Fig. 3. A hybrid bulk/FD-SOI CMOS active one pixel image sensor placing the photodiode on the SOI handle wafer (a) cross sectional view of one pixel (b) equivalent circuit of one pixel (M1:Readout gate, M2:Reset transistor, M3:Source follower, M4:Row select transistor)

3. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 4 shows the I_D-V_{DS} characteristics of a FDSOI nMOSFET. The threshold voltage is 0.65 V and the characteristic is nearly ideal. Since the channel is fully depleted, the kink effect does not occur. The subthreshold slope of the FDSOI nMOSFET is about 70 mV/decade.

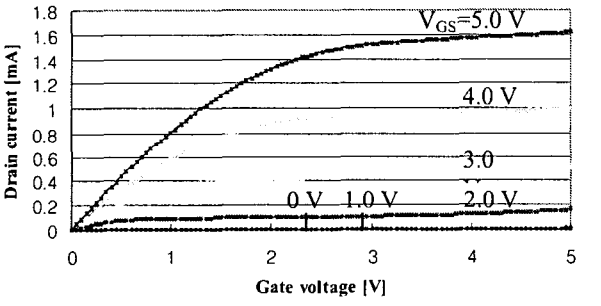


Fig. 4. I_D-V_{DS} characteristics of fabricated fully-depleted SOI nMOSFET. Channel length is 5 μm and channel width 12 μm. The threshold voltage of the nMOSFET is 0.65 V.

Dark current cannot be accurately determined analytically or using device simulation tools. The dark current can only be accurately determined experimentally. Figure 1 shows the sources of dark current. The leakage current between LOCOS and n-type region of the photodiode has been known as the main sources of junction leakage currents. By using Hybrid bulk/SOI pixel structure, the junction between LOCOS and n-type region of the photodiode can be eliminated and dark currents can be suppressed significantly. The photodiode has an effective active dimension of 20 μm by 20 μm. Signal charges are transferred by a readout gate voltage. Figure 5 shows the photodiode operation by a readout gate voltage. The dark current is not changed by readout gate voltage. When the light source (630 nm = 290 μw/cm^2, 520 nm = 370 μw/cm^2, 450 = 450 μw/cm^2) is illuminated, however, the output optical current is changed from 12 nA/ to 39 nA at 2 V of V_{DD}. The threshold voltage of the readout gate is 0.4 V in light. The graph shows a dark current of about 10 nA/cm^2 at the V_{DD} of 2 V. The dark current was higher than desired, and points toward the need for the optimization of the channel stop implants in order to reduce the surface electric field.

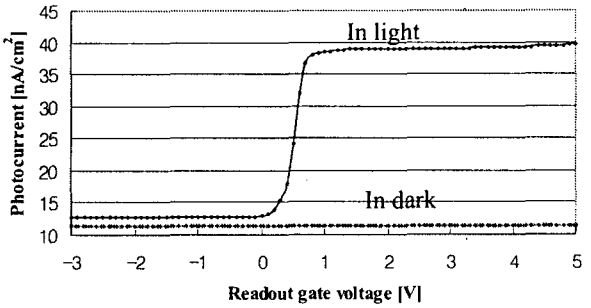


Fig. 5. Photocurrent versus a readout gate voltage with the reset transistor turned on at V_{DD}=2 V. The light source (630 nm = 290 μw/cm^2, 520 nm = 370 μw/cm^2, 450 = 450 μw/cm^2) is illuminated. The threshold voltage of the read out gate is 0.4 V.

We measured the spectral response of a pinned photodiode and observed very flat in the wavelength range from green to red, because low substrate doping yields a large depletion width for a field-aided carrier collection from a deep region in the handle wafer. The monochromator illuminates the fabricated chip from 300 nm to 700 nm by 50 nm steps. Figure 6 shows the measured quantum efficiency normalized with a peak value. The spectral response is very flat from 400 nm to 700 nm. The peak value is out of the detecting rage, however, quantum efficiency need for the optimization of the doping profile of pinned photodiode. As the absorption region is deep on the handle wafer, a photocurrent is low in the wavelength range of green.

The hybrid SOI CMOS APS configuration is shown Fig. 3. A series of pulses are applied to the gate of the source of the reset transistor to reset the gate voltage of M2 to a high voltage before the start of the current integration. The photodiode will then discharge the charge stored at the

gate of M2 and the resulting voltage is reflected by the source follower to the output and is measured. Figure 7 shows that the output voltage of the source follower changes linearly with the variation of FD voltage. Figure 8 shows the photograph of the fabricated chip that is packaged in a quad flat package (QFP).

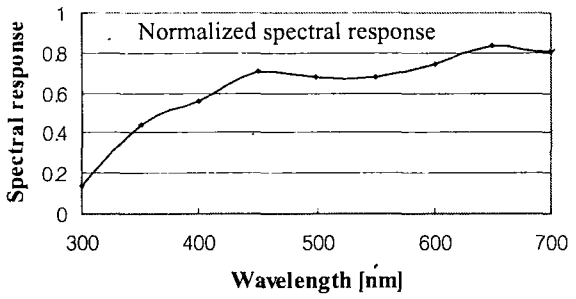


Fig. 6. Normalized quantum efficiency of a photodiode fabricated in the SOI handle wafer versus wavelength. The monochromator illuminates the fabricated chip from 300 nm to 700 nm by 50 nm steps.

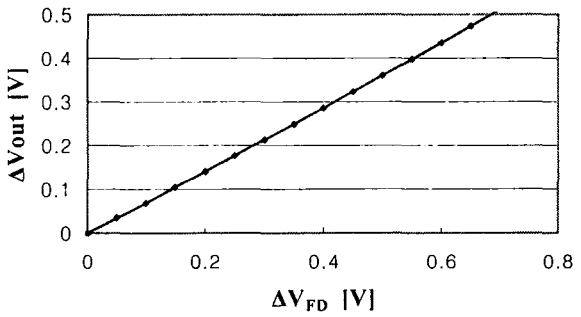


Fig. 7. The output voltage of the source follower changes linearly with the variation of FD voltage.

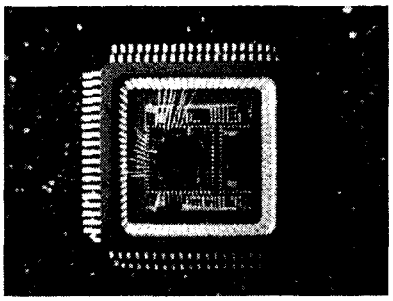


Fig. 8. The photograph of the fabricated chip that is packaged in a quad flat package.

4. CONCLUSION

The hybrid bulk/FDSOI CMOS active pixel image sensor is fabricated on UNIBOND wafers. The pinned photodiode, readout gate, and FD on the handle wafer are formed by an extra etching step with one extra mask to remove the BOX on the SOI handle wafer. By using the hybrid pixel structure, dark currents can be suppressed significantly. The spectral response of a pinned photodiode on the SOI handle wafer is very flat from 400 nm to 700 nm and the dark current is about 10 nA/cm^2 at the V_{DD} of 2 V. The dark current is higher than desired, and points toward the need for optimization of the channel stop implants. The output voltage of the I-V converter changes linearly with the variation of FD voltage. Therefore, our hybrid bulk/FDSOI CMOS APS has great potential in application such as mobile equipment, space and military.

References

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