Implementation of MDCT core in Digital-Audio with Micro-program type vector processor

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Abstract: High Quality CD, DAT audio requires that large amount of data. Currently, multi channel preference has been rapidly propagated among latest users. The MPEG(Moving Picture Expert Group) is provides data compression technology of sound and image system. The MPEG standard provides multi channel and 5.1 sounds, using the same audio algorithm as MPEG-1. And MPEG-2 audio is forward and backward compatible. The MDCT (Modified Discrete Cosine Transform) is a linear orthogonal lapped transform based on the idea of TDAC(Time Domain Aliasing Cancellation). In this paper, we proposed the micro-program type vector processor architecture a benefit in MDCT/IMDCT of MPEG-II AAC. And it's reduced operating coefficient by overlapped area to bind. To compare original algorithm with optimized algorithm that cosine coefficient reduced 0.5%, multiply operating 0.098% and add operating 0.58%. Algorithm test is used C-language then we designed hardware architecture of micro-programmed method that applied to optimized algorithm. This processor is 20MHz operation 5V.

MDCT, IMDCT, TDAC, MPEG-II AAC, Micro program, Vector Processor

1. INTRODUCTION

Mpeg is actually an acronym of the Moving Pictures Experts Group which was formed by the ISO (International Standards Organization) to set standards for audio and video compression and transmission. While on the other hand, MPEG-1 Layer III has been widely used as a high quality audio coding algorithm for portable audio device, PC software and Internet music distribution system. MPEG-2 Advanced Audio Coding(AAC) has already been standardized as a more sophisticated next generation technology. AAC provides an audio signal that has CD quality at 96-128Kbps, bitrate 30% lower than that of MP3. This AAC standard allows ITU-R 'Indistinguish- able' quality to data rates of 320 Kbit/sec for five full bandwidth channel audio signal[1][2].

The compression ratio is a factor of 1.4 better than compared to MPEG-1 Layer3. MPEG-2 AAC is composed of Huffman coding, Quantization, Scaling, MDCT, Gain control and Hybrid filter-bank. Among the most operation part is MDCT/IMDCT. MDCT technology is removed by aliasing of TDAC method that subband coding. MDCT is time domain data to frequency domain, reverse IMDCT is a frequency data to time domain[3]. MDCT have the advantage of time domain aliasing removed by windows that overlapped 50%. MPEG-2 AAC architecture is high-level representation of encoding closely parallel process described above all. The input audio stream passes through a psychoacoustic model that determines the SMR(Signal-to-Masking Ratio) of each subband[4]. The bit or noise allocation block uses the SMR decide how to apportion the total number of code bits available for the quantization of the subband signals to minimize the audibility on quantization noise. Finally, the last block takes the representation of the quantized audio samples and formats the data into a decodable bit stream. The decoder simply reverses the formatting, then reconstructs the quantized subband values and finally transforms the set of subband values into a time domain audio signal. The specified MPEG requirements and ancillary data not necessarily related to the audio stream could be fitted within the decoded bit streams.

2. MDCT/IMDCT

In this section, it's briefly discussed the concepts of MDCT/IMDCT algorithm, architecture operation and specifications based on the concepts. MDCT combines critical sampling with the good frequency resolution provided by a sine window and the computational efficiency of a fast FFT algorithm. Typically equally spaced bands of 128 to 512 are used. The MDCT makes an offered to also the possibility of changing the block length the dynamically transform[5]. For very dynamic input signals a short block length keeps the quantization error local in time, for a quasi-static signal to long block length provides a good frequency resolution. The MDCT and IMDCT were employed in a technique called TDAC. The equation of the MDCT is

$$X(i,k) = 2 \cdot \sum_{n=0}^{N-1} x(i,n) \cos\left(\frac{2\pi}{N}(n+n_0)(k+\frac{1}{2})\right) \quad (1)$$

$$for\ 0 \le k < \frac{N}{2}$$

The equation of the inverse MDCT is

$$X(i,k) = \frac{2}{N} \cdot \sum_{n=0}^{\frac{N}{2}-1} x(i,k) \cos\left(\frac{2\pi}{N}(n+n_0)(k+\frac{1}{2})\right) \quad (2)$$

$$for\ 0 \le k < N$$

To compare (1) with (2), it is equally method except for the length of coefficient and multiplexing 2, 2/N after accumulating[6]. Fig 1 shows that the MDCT windows transition between long and short block modes.

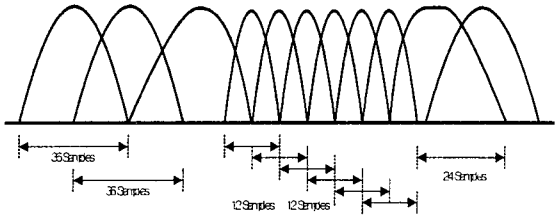

Fig. 1. The Arrangement of overlapped MDCT windows

The short block length is one third of that the long block. In the short block mode, three short blocks replace a long block so that the number of MDCT samples for a frame of audio samples remains unchanged regardless of the block size section[7]. The frame of audio samples, the MDCT able to have all the same block lengths(long or short) or the mixed-block mode. In the mixed-block mode the MDCT for the two lower frequency subband have long blocks, and the MDCT for the 30 upper subband have short block. This mode provides better frequency resolution for the lower frequencies, where it is needed the most without sacrificing time resolution for the higher frequencies. The switch between long and short blocks is not instantaneous. A long block is the specialized long-to-short or short-to-long data that windows serve transition between long and short block types. Because the MDCT processing of a subband signal provides better frequency resolution that consequently has the bad time resolution. The MDCT operates on 12 or 36 polyphase filter samples, so the effective time windows of audio samples involved 12 or 36 times in this processing. MDCT /IMDCT coefficients selected lookup table in block type of Long, Long-Short, Short, Short-long. Similarly, windows table is selected in this block type to improve the individual subband isolation. And we used to delay components of z^{-18} for 50% overlapped in time domain.

3. MDCT/IMDCT ALGORITHM OPTIMIZATION

Several MDCT/IMDCT algorithms are known as (1) and (2). (1) is applied to (2) of optimization. (3) Shows that Cosine coefficient to an exponential function.

$$\cos\left(\frac{2\pi}{N}(n+n_0)(k+\frac{1}{2})\right) = e^{j\frac{2\pi}{N}(n+n_0)(k+\frac{1}{2})} = C_N^{(n+n_0)(k+\frac{1}{2})} \tag{3}$$

Therefore, (3) is represent to (4)

$$X(i,k) = 2\cdot\sum_{n=0}^{N-1} x(i,n)C_n^{(n+n_0)(k+\frac{1}{2})} = C_N^{n_0(k+\frac{1}{2})}\sum_{N=0}^{N-1} x(i,n)C_N^{n(k+\frac{1}{2})} \tag{4}$$

(4) is possible to split each even and odd domain.

$$X(i,k)=C_N^{n_0(k+\frac{1}{2})}[\sum_{even} x(i,n)C_N^{n(k+\frac{1}{2})}+\sum_{odd} x(i,n)C_N^{n(k+\frac{1}{2})}]$$
$$=C_N^{n_0(k+\frac{1}{2})}[\sum_{r=0}^{(N/2)-1} x(i,2r)C_N^{2r(k+\frac{1}{2})}+\sum_{r=0}^{(N/2)-1} x(i,2r+1)C_N^{(2r+1)(k+\frac{1}{2})}]$$
$$=C_N^{n_0(k+\frac{1}{2})}[\sum_{r=0}^{(N/2)-1} x(i,2r)C_N^{2r(k+\frac{1}{2})}+C_N^{(k+\frac{1}{2})}\sum_{r=0}^{(N/2)-1} x(i,2r+1)C_N^{2r(k+\frac{1}{2})}] \tag{5}$$

The equation of (5) is converting N point MDCT into N/2 point MDCT.

$$X(i,k)=C_N^{n_0(k+\frac{1}{2})}[\sum_{r=0}^{(N/2)-1} x(i,2r)C_{N/2}^{r(k+\frac{1}{2})} + C_N^{(k+\frac{1}{2})}\sum_{r=0}^{(N/2)-1} x(i,2r+1)C_{N/2}^{r(k+\frac{1}{2})}] \tag{6}$$

(6) is possible to split each even and odd area.

$$E(i,k)=\sum_{r=0}^{(N/2)-1} x(i,2r)C_{N/2}^{r(k+\frac{1}{2})}$$
$$O(i,k)=\sum_{r=0}^{(N/2)-1} x(i,2r+1)C_{N/2}^{r(k+\frac{1}{2})}$$
$$X(i,k)=C_N^{n_0(k+\frac{1}{2})}[E(i,k)+C_N^{(k+\frac{1}{2})}O(i,k)] \tag{7}$$

To present of flowchart using (7) is shown in Fig 2.

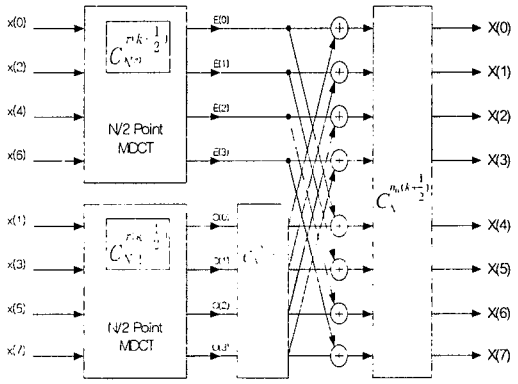

Fig. 2. N/2 point MDCT.

The use of this method, we have to split each even and odd area into E(i,k) and O(i,k).

$$E(i,r)=\sum_{r=0}^{(N/2-1)} e(i,r)C_{N/2}^{r(k+\frac{1}{2})}$$
$$=\sum_{m=0}^{(N/4-1)} e(i,2m)C_{N/2}^{2m(k+\frac{1}{2})}+\sum_{m=1}^{(N/4-1)} e(i,2m+1)C_{N/2}^{(2m+1)(k+\frac{1}{2})}$$
$$=\sum_{m=0}^{(N/4-1)} e(i,2m)C_{N/4}^{m(k+\frac{1}{2})}+C_{N/2}^{(k+\frac{1}{2})}\sum_{m=0}^{(N/4-1)} e(i,2m+1)C_{N/4}^{m(k+\frac{1}{2})}$$
$$=G(i,k)+C_N^{k+\frac{1}{2}}H(i,k) \tag{8}$$

But,

$$G(i,k)=\sum_{m=0}^{(N/4)-1} e(i,2m)C_{N/4}^{m(k+\frac{1}{2})}$$
$$H(i,k)=\sum_{m=0}^{(N/4)-1} e(i,2m+1)C_{N/4}^{m(k+\frac{1}{2})}$$

Also, it is representative of N/4 point MDCT when N/2 is odd.

$$O(i,k)=\sum_{r=0}^{(N/2)-1} x(i,2r+1)C_{N/2}^{r(k+\frac{1}{2})}$$
$$=\sum_{m=0}^{(N/4)-1} o(i,2m)C_{N/2}^{2m(k+\frac{1}{2})}+\sum_{m=0}^{(N/4)-1} o(i,2m+1)C_{N/2}^{(2m+1)(k+\frac{1}{2})}$$
$$=\sum_{m=0}^{(N/4)-1} o(i,2m)C_{N/4}^{m(k+\frac{1}{2})}+C_{N/2}^{k+\frac{1}{2}}\sum_{m=0}^{(N/4)-1} o(2m+1)C_{N/4}^{m(k+\frac{1}{2})} \quad (9)$$

The present of flowchart using (9) is shown in Fig 3.

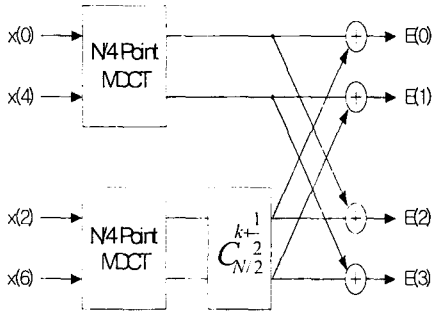

Fig. 3. N/4 point MDCT.

It is able to express N/8 point MDCT using N/4 point MDCT. N/8 point MDCT is shown in Fig 4.

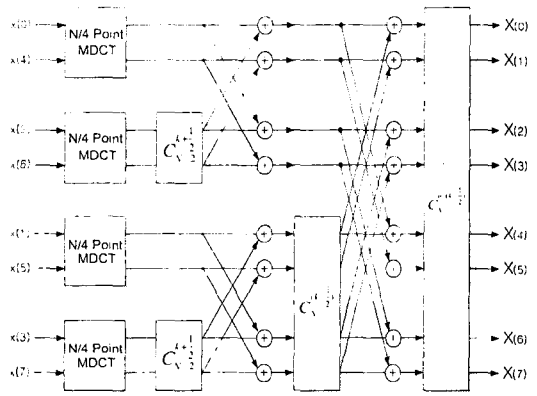

Fig. 4. N/8 point MDCT.

The operation course likes that a minimum operation element to be used multiplies the factor of the even domain on the 2 input additions. The scheduling of MDCT/IMDCT operation element is shown in Fig 5.

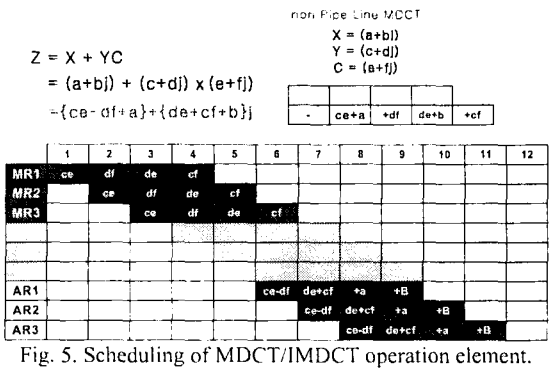

Fig. 5. Scheduling of MDCT/IMDCT operation element.

Fig 8 expresses the pipeline scheduler who removed pipeline hazard of operation element that using MDCT and IMDCT. Floating point multiplier and all inputs of add operation in rising edge of clock and output operation in falling edge of clock. When is operation that programmable delay does hazard control, and addition because multiplying 2 complex number input and 1 complex number coefficient have received all of real number calculation value and imaginary calculation value spending 4 cycles.

In case of MPEG-2 AAC, it performs to the maximum 2048 MDCT and number of necessary coefficient is 2048. But using this algorithm, 10 Memory words when hardware implementation of embodied structure. For example, N= 2048 k=2068 in 2048 point MDCT, consequently total multiplexing is 10,400 times. When calculating without optimization, could know that the operation amount decreases about 400 times when comparing with prospects of amount 4,194,304 times.

4. SYSTEM DESIGN USING VECTOR PROGRAMS

The MDCT requires many cumulative operations relatively high precision of about 96dB is desired to be compare with an image data. Therefore, the system that used to floating-point multiplier and adder of satisfying a precision 96dB maximum 2048 point MDCT. The multiplier has 6bit in exponent and 24bit in mantissa part. The adder used floating point addition, which has 6bit in exponent and 56bit in mantissa to cumulative addition could be chance of multiplication result. The exponent part has dynamic range and mantissa designed a plan sufficiently to reduce the error of mantissa operation. The mantissa part of adder has 56bit. This keeps throw a mantissa when cumulative addition is multiplication output from adder because it do not use MAC specially. The vector controller of micro program method is shown in Fig 6.

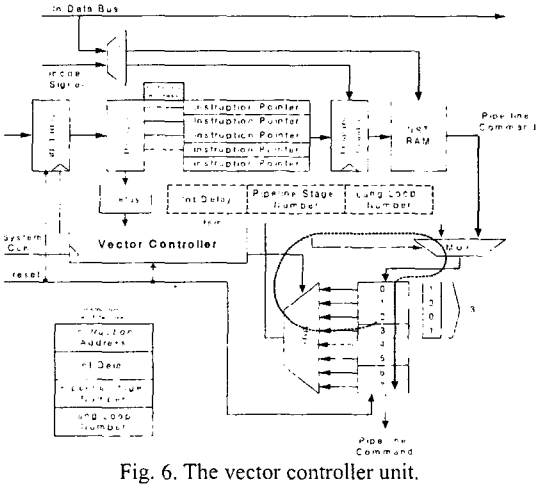

Fig. 6. The vector controller unit.

In this paper, multiplier and adder designed a plan all pipeline to operation speed optimization. The Addition architecture of mantissa multiplication of pipeline radix-4 booth multiplier, which is the desired adder of mantissa

input bit width that have double when parallel booth multiply. But in this paper, 24bit radix-4 booth multiplier consists of addition tree by 26bit adder, using last node 31bit adder of addition tree. And 56bit FP-Adder consist of CSA(Carry Save Adder). By reasons of CSA method uses, it is not consume pipeline stage. Pre-normalizer assumes that floating point number to become barrel shifter inputted pre/post-normalizer used each 46bit barrel shifter. Vector instruction is defined micro-program instruction as a basic operation element, which accomplishes with the multiplier of additions. The feature of such architecture, the operations that the user wants to accomplish as the defined micro-program instruction of the best suited taking the hazard into account. The vector controller unit consists of a pipelined micro program register, reason that use micro instruction register for very long instruction. This instruction architecture is a hardware macro with zero-overhead loop capability. The basic operation is a sequence of stream data block. And it's able to execute vector operation with external large memory instead of internal register files. The whole system consists of FP-Adder, FP-multiplier, In/Out buffer instead of Vector register, a hazard control programming delay controller, and Vector instruction controller of micro program method. Buffers that take the place of vector register away overhead in operation because it's interfaced with external synchronism RAM. The architecture of Vector-MDCT processor is shown in Fig 7.

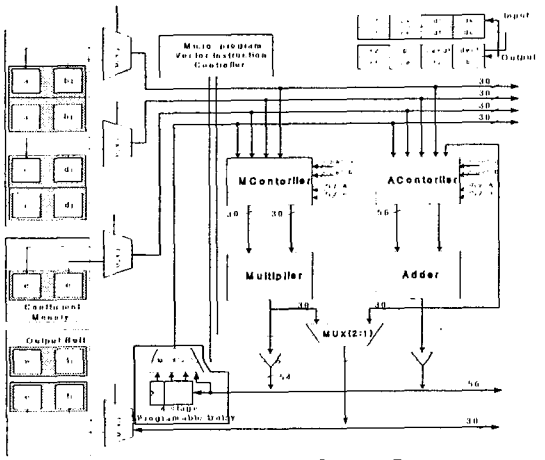

Fig. 7. The block diagram of Vector Processor.

This diagram is 96dB density benefit of floating point multiplier and adder, exponent is used 8bit and mantissa is used to 24bit. The scheduling above is the pipeline scheduler that an operative removal the pipeline hazard used to MDCT/ IMDCT. The FP-Adder and FP-Multiplier all input data operates in rising edge and output result has falling edge. The hazard is controlled by program delay. In this case, the addition of multiplied was inputted on 2unit complex number and 1unit complex number coefficient.

5. DESIGN IMPLEMENTATION AND EXPERIMENTAL RESULTS

In this paper, the system implemented by the user uses an external ROM at an initialization and defined vector instructions. It was the low operation mode so that an application program, which mixes could be executed. The controller is organized of an Instruction RAM, Instruction Pointer, Vector instructions ring buffer and Shifter. The multiplier and adder perform on the independent operation. In this case, one clock cycle has two outputs. Algorithm verification use C-language. This processor is designed through VHDL language and synthesis by Synplify Pro 7.2 of Synplicity Inc, rule checked by SADAS. The top block diagram of Vector MDCT is shown in Fig 8.

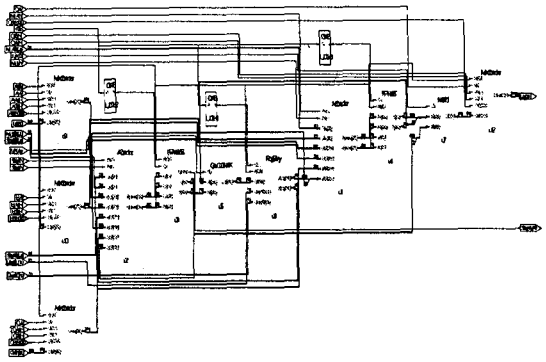

Fig. 8. The synthesis diagram of vector MDCT.

Verilog-XL of CADENCE performs on functional and timing simulation for pre/post layout simulation. The post layout simulation result is shown in Fig 9.

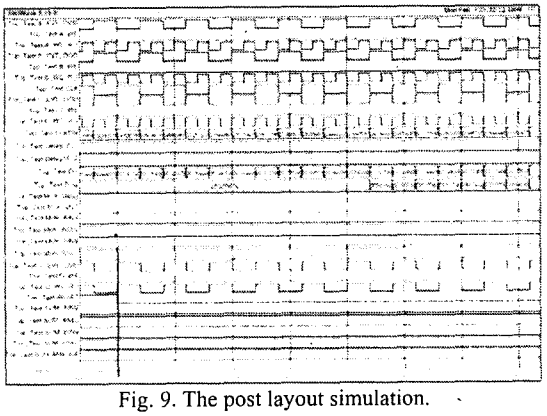

Fig. 9. The post layout simulation.

Fig 10 composed the Vector MDCT top block diagram using SYNOPSYS DA. ATS2 of IMS has verified the functional and SHMOO test of Vector processor.

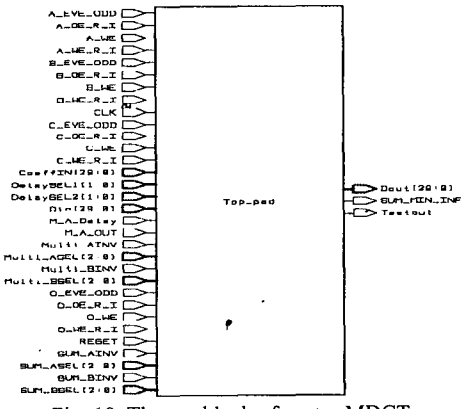

Fig. 10. The top block of vector MDCT.

The SHMOO test simulation result is shown in Fig 11. This processor has 20 MHz operation 5V.

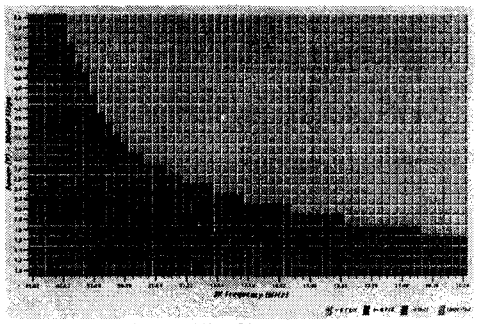

Fig. 11. The SHMOO test.

6. CONCLUSIONS

In this paper, the MDCT/IMDCT algorithm is an optimization of used MPEG-2 AAC and its designed using vector program method. We optimize a standard algorithm so that the processing was possible to a 0.25% operation. I.e., we showed efficiency in the 0.098% of multiplication and 0.58% of addition compared to previous optimization. 30bit FPU multiplier and 56bit FPU adder designed high precision and high speed to treat sufficiently until other operation of designed process in MPEG-2 AAC.

In this paper, the core has general DSP architecture that consists of 40000 gates. This processor is able to process 2048-point MDCT/ IMDCT of MPEG-2 AAC within 5000 cycles, TNS 38 tap filters of AAC within 10000 cycles and 2048 FFT within 12000 cycles. Designed system accomplished with pipeline method, a control unit design is much to situation of designer because pipeline instruction and scheduling defined a user of all system. Also, the situation of the users is used to application program by converting binary without development again application program by converting instructions. The designed MDCT/ IMDCT Vector processor is adapted to a core of digital broadcasting. The subject afterward causes to complete binary transform ability to other process of supplementation more an instructions controller. And we make the process load of cyber machine such as a JAVA processor.

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