Design of the timing controller for automatic magnetizing system

Yi, Jae Young*, Arit Thammano**, and Yi, Cheon Hee***
* Technical Univ. of Budapest, E-mail: yi_young@hotmail.com
** King Mongkut's Institute of Technology Ladkrabang, Thiland
*** Chongju Univ., Dept of Electronic Engineering, E-mail: yicheon@chongju.ac.kr

Abstract: In this paper a VLSI design for the automatic magnetizing system has been presented. This is the design of a peripheral controller, which magnetizes CRTs and computers monitors and controls the automatic inspection system. We implemented a programmable peripheral interface(PPI) circuit of the control and protocol module for the magnetizer controller by using a 0.8um CMOS SOG(Sea of Gate) technology of ETRI. Most of the PPI functions has been confirmed. In the conventional method, the propagation/ramp delay model was used to predict the delay of cells, but used to model on only a single cell. Later, a modified "Linear delay predict model" was suggested in the LODECAP(LOgic Design Capture) by adding some factors to the prior model. But this has not a full model on the delay chain. In this paper a new "delay predict equation" for the design of the timing control block in PPI system has been suggested. We have described the detail method on a design of delay chain block according to the extracted equation and applied this method to the timing control block design.

Key words :VLSI design, Magnetizing system. Timing controller, linear delay.

1. INTRODUCTION

The automatic magnetizing and inspection system consists of CPU, RAM, ROM, PPI, key-boards, Led displays, and input and output departments of the magnet force, etc.[1]

To control these various peripheral devices properly, 72th bidirectional interface ports is needed, and signals coming from the peripheral equipment such as a keyboard which considered to real time. Generally, the control method to control the interface ports is to control input and output signals using the 8 bit data bus structure. In this case, CPU has to check the status of the interface ports always and take a lot of time consuming. Especially, in case of controlling 12 to 16 bit structured peripheral devices, such a automatic magnetizing and inspection system, the load increased more and more. So, to lessen the CPU load there needs a controller which can request a interrupt to the CPU directly through the peripheral interface equipment, and this controller can control directly the other peripheral interface equipment by the interrupt enable response from CPU. Also, a PPI controller which can adapt bits of ports to the various port structure of the peripherals is needed.[2]

This paper analyzed the propagation/ramp delay modeling method on a CMOS inverter device, compared this results with the analysis results of the linear estimation model which was more advanced one. We also proposed a new "delay predict equation" for the design of the timing control block in PPI system, designed a new delay chain using this equation, and compared the designed delay values with the post simulation results obtained after the placement & routing(P&R).

Finally, we applied this delay chain to designing a edge detected clock generator of the timing control block, and described the design method of the timing controller block in detail.

2. CONFIGURATION OF AN EDGE DETECTED CLOCK GENERATOR

PPI has to clock at the rising edge of read or write signals coming from CPU. Edge detected clock generator detects this rising edge signal, and have to (1) store a control word to the register, (2) clear the output ports, (3) generate a signal that has contents of register come out through the bus line. This block requires a waveform and AC characteristics as shown in Figure 1.

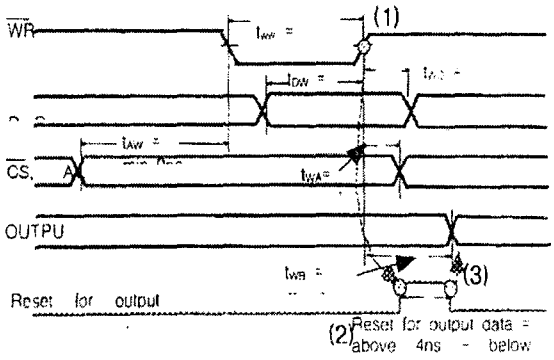


Figure 1. Waveform of an edge detected clock generator

A data signal has to be detected at the start of the rising time of write signal, and write into the control word register between at the rising edge of write signal and at the end of address hold time (t_{WA}). The previous output of the ports must be reset within the time (t_{WB}) while this output signal is maintained. And the contents of control word register must be outputted to the output port.

As a result, after detecting a rising edge of the read and write signal and delaying 20ns, the output reset signal of 20ns width must be generated from the edge detected clock generator. This signal is possible to design by constructing the delay chain.

In the front-end design procedure, it is not easy to decide what kind of devices and how many devices to be used in the delay chain having a delay of 20ns.

The simulator for the front-end procedure can not exactly predict a delay because it has a delay model which has not a sufficient consideration about a placement and routing process. But, in the back-end procedure the simulator can model exact delay values in the post simulation process, for it is a finished status about a placement and routing. Therefore, the exact delay value can be predicted after finishing the back-end and have a problem of doing the front-end and the back-end procedure repeatedly. To solve this problem, we have to obtain delay values of the basic cell at the start point of the design process.

The delay characteristics of CMOS gates can be modeled in the various methods.

Analytical expressions of the output waveform and the propagation delay, including the effect of the input waveform slope, was presented in,[3] which can model in the two-dimensional gate delay table model which has variables of the rising and falling time of the input waveform and variables of the load capacitance at the output.[4]

The effect of the interconnect circuit on the gate delay time can be represented through the effective capacitance concept,[5] and the effect of the gate[6] on the interconnect circuit delay time can be represented through the theoretic analysis of the driving characteristics of CMOS gates, and on each MOS consisting of an inverter a method predict the delay time which take the output voltage by the time was proposed.[7]

In this paper this VLSI was implemented using a 0.8um CMOS SOG technology. This COMS SOG technique starts from the finished status(state) of the layer process except contact, via, and metal layer process.

As a result, starting from the confirmed status of various parameters of the basic cells concerning the delay model with various techniques, we need only the analysis of the basic cell library which is provided from the fabrication companies.[8]

In this paper, analyzing the method of calculating a propagation delay predict time on inverters which was adapted to the library, and revising this predict model, we proposed a new "delay predict equation", and implemented a delay chain block according to the extracted equation.

Logic devices of the delay chain must be selected considering following conditions. That is, a available design rule must be selected, and lower power cells and longer delay cells must be also selected. In this paper, the delay chain is constructed using inverters, which are the simplest cells. And delay times of this delay chain composed of 0.5X and 1X inverters are compared considering the delay effect.

3. EXPERIMENTAL AND DISCUSSION.

The propagation delay time is called the time between the input transition and the output transition time of the logic, and usually calculated from the switching threshold level of the input to the switching level of the output.

In the o.8um SOG technology, propagation delay model has been adopted, and 50% of the edge rate using the ISM(Input Slope Modeling) technique has been modeled.

Total delay(tTOTAL) from the input pin to the output pin in a single basic cell without in and out connections was described as in equation (1). tTOTAL has two values, one is the rising transition value and the other is the falling transition value.

$$tTOTAL = tDELAY + tINT + tSLEW * Cld \rightarrow \quad (1)$$

The 0.8um CMOS inverter cell library adopted equation (1) had been well described in the data book.

IN01D0 is a inverter basic cell, has a driving capability of 0.5X and IN01D1 is also a inverter basic cell, has a driving capability of 1X. Symbol I is the input pin capacitance. had 0.043pF for 0.5X cell and 0.087pF for 1Z cell. Symbol ZN is the output pin capacitance. has 0.04pF for 0.5X and 0.043pF for 1X. These values are very important factors for the delay calculations.

Also, the performance equation at the rising transition of the IN01D0 shows 0.09ns of the internal delay of the cell(tDELAY), 0.13ns of the delay due to the intrinsic output capacitance(tINT), and 3.35ns/pF of the slew rate of the output(tSLEW). All of these values are expressed as the variables in the equation (1). These values of the delay can be modeled and described as in the figure2.

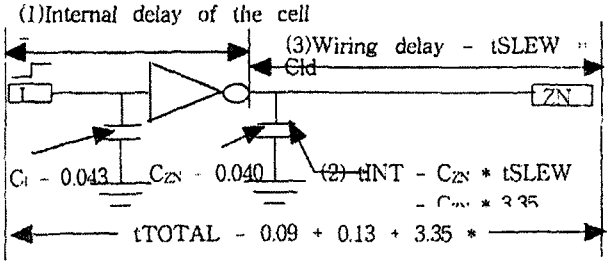


Figure 2. tTOTAL of a basic cell

Figure 2 is a example for the rising. Total delay the specified input to the specified output(tTOTAL) is expressed as the followings, (1) the internal delay of the cell (tDELAY), (2) the delay due to the intrinsic output capacitance (tINT), and (3) the wiring delay which is the slew rate of the output (tSLEW) multiplied by the load capacitance for each output (Cld). This total delay is expressed as the equation (1).

Similarly, the total delay at the falling transition can be expressed such as

$$tTOTAL = 0.07 + 0.06 + 1.43 * Cld$$

For 0.5X and 1X inverters, when the standard load is 0.43pF, propagation/ramp delay's value becomes 0.51ns at the rising and 0.25ns at the falling, so a tTOTAL of the inverter pair becomes 0.76ns.

As a result, the values of the propagation/ramp delay is shown in the chart 1 and chart 2 according to the number of cells composed of the delay chain for the o.5X inverter and 1X inverter.

The wire capacitance and the delay caused by the connections between the gates are no considered and in the library provided by the wafer fabrication companies, the load capacitance for each output (Cld) in the equation(1) is not defined. This is why Cld value varies as the process technology of the fabrication companies, a kind of the gate base array, the length of the interconnection, the number of the fanout. Therefore pre-defined standard loads can be available to calculate Cld, and there is a problem that we can't calculate the delay of the inverter only from the library provided by the fabrication companies.

4. ANALYSIS OF THE LINEAR DELAY PREDICT MODEL CONSIDERED A PROCESS PARAMETER, WIRE CAPACITANCE AND INTERCONNECTION CAPACITANCE

LODECAP(LOgic DEsign CAPture) uses all design information in the format of the VHDL language.[9]

So, Basic cells were made by the VHDL linear delay predict model. The LODECAP has a characteristic of applying the predict model to the pre-simulation procedure.

In this paper, we analyzed this predict model, proposed the "delay predict equation", and then adopted this equation to the design of the edge detected clock generator.

Total delay is calculated as the delay value in the equation (3) multiplied by the derating factor having between 0.0 and 1.0. The delay value in the equation (3) is composed of the internal delay (D_{int}) and the delay (D_{inc}) of the sum of the interconnection and wiring.

The derating factor is the modeling variables of the factors obtained from the chip derating temperature. power supply voltage, and the chip fabrication process conditions. And the fewer the derating factor is, the faster the circuit speed is. This value has a typical value of 0.5.

Total delay of the basic cell

$$= \text{Delay} * \text{Derating\_Factor} \quad (2)$$

$$\text{Delay} = D_{int} + D_{inc}$$

$$= D_{int} + [C_{linear} * (\text{sum of interconnection Cap.} + \text{sum of wire Cap.})] \quad (3)$$

sum of interconnection Cap.

$$= (\text{each connection Cap.}) \quad (4)$$

sum of wire cap.

$$= C_{estimation} * \text{number of connection} + Cap0 \quad (5)$$

Wile D_{int} is a fixed delay value which is decided during the cell layout design, D_{inc} is a delay value which is decided from the drive capability and intrinsic capacitance of the cell. Intrinsic capacitance is a total value which adds the wire capacitance in itself to the sum of the capacitance for the gate pins on the one net in the circuit.

Delay values becomes a linear function as an intrinsic capacitance shown in the equation (3). The slew rate and internal delay of the cell(D_{int}) which defines the linear function are the proper values decided during cell development procedure, and defined in VHDL program.

The sum of interconnection capacitance must be calculated by the number of interconnections, the length and shape of the poly and the metal connected at one net.

But, in the logic design step that a layout isn't completed, we don't have the information on the layout. This problem can be solved by using VHDL linear delay predict model considered a process parameter and wire and interconnection capacitance.

The LODECAP uses the interconnection capacitance predict model linearly proportional to the pin connected to the net for the basic cell's wire capacitance. Slew rate of this linear model and cell capacitance(Cap0) value of each device are different from according to the gate base array.

The gate base array model is named as "pred***" which is a kind of wide range variable names(ex. pred186) in the design flow manager. The value of the base array has been defined in the file "checkRamp Delay.Mcap" in each library directory on the file system in the LODECAP.

This delay model has been defined in the VHDL model of each basic cell, being simultaneously used for the VHDL simulation, the ramp delay check and the timing verification.

To design the delay chain accurately, for the inverter cell of the main configuration, the internal delay of the cell(D_{int})and the Slew rate(C_{linear}) and the capacitance in the IN01D0 and IN01D1 can be defined as in table1.

Table 1. The capacitances in the IN01D0 and IN01D1

	RISE		FALL		Capacitance	
	D_{int}	C_{linear}	D_{int}	C_{linear}	C_I	C_{ZN}
IN01D0	0.09 ns	3.35 ns/pF	0.07 ns	1.43 ns/pF	0.043 pF	0.040 pF
IN01D1	0.11 ns	1.68 ns/pF	0.06 ns	0.71 ns/pF	0.087 pF	0.043 pF

These values are only a single basic cell's ones, and can not be applied as the same value in the delay chain to implement in this paper. Some considerations of the interconnection delay between the gates must be added.

For this, the estimated slew rate($C_{estimation}$) of the linear model and the cell capacitance of each inverter

must be known, which are obtained from the values of the vgc400186 base array in the pvgc450(0.8um SOG) of the gate array base model defined in "check RampDelay.Mcap" file in the LODECAP. Values of the vgc400186 base array are 0.096pF and 0.029pF.

Using this value, Dint, the Slew rate(C_{linear}) and the capacitance value on the input and output, total delay value can be calculated by the equation (6) and (7), and the inverter chain model of figure 3.

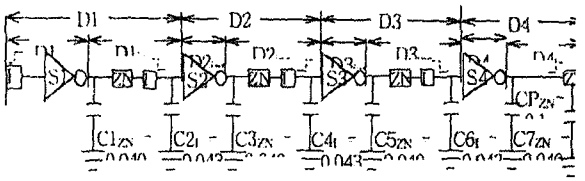


Figure 3. Cap. values of an inverter chain model

Total delay of the inverter chain model =

$$\sum Dx * Derating\_Factor \quad (6)$$

$$Dx = D_{Xint} + D_{Xinc}$$

$$Dx = D_{Xint} + \{C_{linear} * [\sum(\text{each pin Cap}) + (C_{estimation} * \text{number of pin} + Cap0)]\} \quad (7)$$

$D1 = D1int + \{C_{linear}$ 0f Rising * [(C1ZN +C2t) + ($C_{estimation}$ of vgc400186 * number of pin + Cap0)]} = 0.09ns + {3.35ns/pF * [(0.04pF +0.043pF) + (0.096pF * 2 + 0.029pF)]} = 1.1084 ns

$D2 = D2int + \{C_{linear}$ of Falling * [(C3ZN + C4t) + ($C_{estimation}$ of vgc400186 * number of pin + Cap0)]} = 0.07ns + {1.43ns/pF * [(0.04pF + 0.043pF) + (0.096pF * 2 + 0.029pF)]} = 0.5047 ns

D3 = same with D1

$D4 = D4_{int} + \{C_{linear}$ of Falling * [(C7ZN +CPZN) + ($C_{estimation}$ of vgc400186 * number of pin + Cap0)]} = 0.07ns + {1.43ns/pF * [(0.04pF +0.1pF) + (0.096pF * 1 + 0.029pF)]} = 0.44895 ns

Total delay of the inverter chain model

$$= \sum Dx * Derating\_Factor$$

$$= (D1 + D2 + D3 + D4) * 0.5$$

$$= 1.585225 \text{ ns}$$

As a conclusion, the delay value of the VHDL linear delay predict model which includes process parameters. wire and interconnection capacitances according to the interconnection number o the chain for 0.5X and 1X inverters is depicted in Figure 4 and 5. And these values are compared to the delay values after the post simulation.[10]

In this Figure, the propagation/ramp delay model and the VHDL linear delay predict model which considers process parameters, wire and interconnection capacitances have an accuracy of 15% and 5% of the relative error rate compared to the post simulation result. And the delay effect for the 0.5X chain are bigger than for the 1X chain.

5. PROPOSAL OF THE DELAY PREDICT EQUATION

The linear delay predict model considered process parameters, wire and interconnection capacitances can be expressed by equation (8) compared to equation (1).

$$tTOTAL(Rise) = \{tDELAY + tINT + tSLEW * [load\ Cap. + (C_{estimation} * \text{Relative fanout} + Cap0)]\} * Derating\_Factor \rightarrow \quad (8)$$

In the above equation when the design rule have been defined (0.8u SOG) and the base array have been also selected(vgc400186), tTOTAL(Rise) and tTOTAL(Fall) of the 0.5X inverter are become 0.5542 and 0.25235, as expressed in the previous section.
Finally, The delay value of the 0.5X inverter pair s a sum of tTOTAL(Rise) and tTOTAL(Fall), and a delay predict value can be calculated from equation (9,10,11)

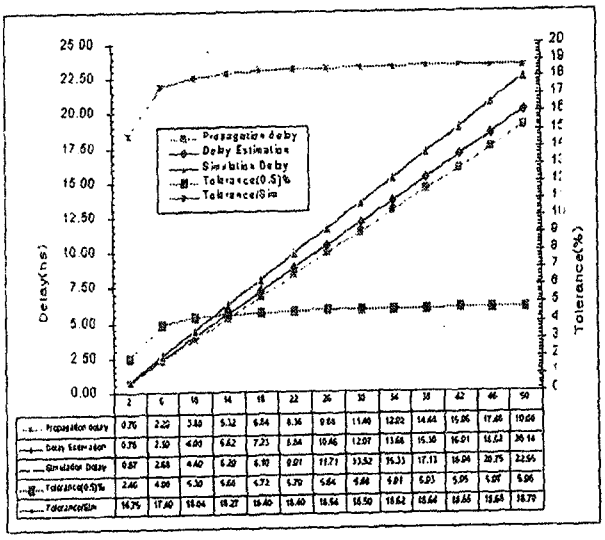
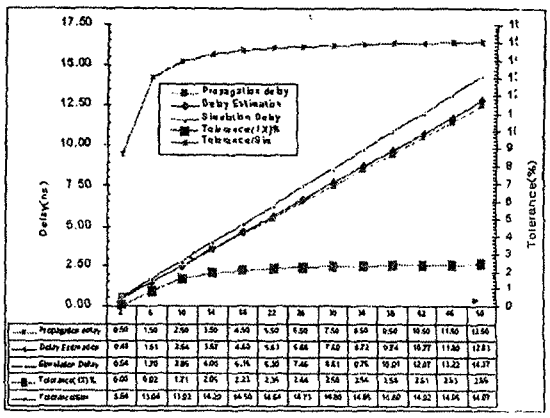


Figure 4. Delay of the 0.5X inverter chain

Delay predict value(D(x)) = (tTOTAL(Rise) + tTOTAL(Fall)) * number of pair(N) (9)

0.5X inverter pair's D(x) = 0.80655 * number of pair(N) (10)

1X inverter pair's D(x) = 0.514 * number of pair(N) (11)



6. DESIGN AND CONFIGURATION OF TIMING CONTROL BLOCK

We Designed the timing control block as the following procedure. (1) setting up the delay chain model as shown in figure 6. (2) making the timing diagram on "output data reset signal" in figure 1. (3) calculating the delay value of each device and connecting the cells as few as possible, (4) designing as S&S(Schematic and Simulation).

In this paper, after applying the delay predict equation, we connected 0.5.X inverters serially.

In Equation (1) supposed the target delay time [D(X)] is 20ns, the required pairs becomes 24 (= 20/0.80655). Therefore 51 inverters are connected for 24.5 pairs of 0.5X inverters and D1 and D4. The simulation result of the delay chain is shown in figure7. 1ns of the error in WRN and D2 resulted from the result of AND added. Equation (1) and the simulation results are well matched. Timing control block is designed as in figure 6 using S&S technique including the edge detected clock generator including the delay chain.

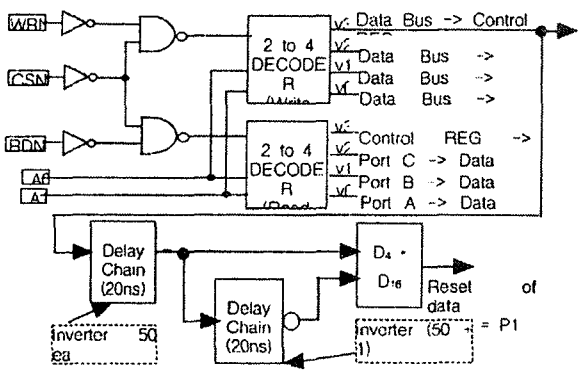


Figure 6. The timing control block diagram

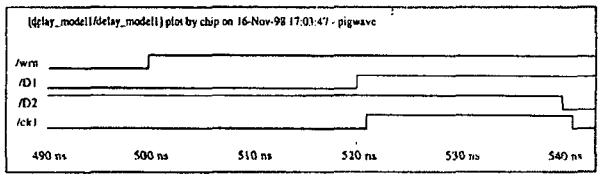


Figure 7. Wave form of the simulation result

7. CONCLUSION

We have designed and simulated ASIC for the programmable peripheral interface controller to control the input-output devices of the automatic magnetizing and inspection system, and after fabrication in ETRI confirmed the PPI function.

The final delay time of the designed delay chain, using the VHDL linear interconnection capacitance predict model is matched with the simulation results.

Implemented ASIC is perated at 50MHz, and consist of about 6000 gates. This chip equipped in the peripheral controller of the automatic magnetizing and inspection system, is supposed to be customized.

References

[1] Cheon-Hee, Yi, and Ki-Jong, Ha, "Development of Statistical Analizing Tool and System of Automatic Magnetizer", Journal of Korea Information. Processing Society. Vol. 3. No.4 P1014-1025, July 1996.

[2] Pic 16/17 Micro controller data book. Micro-chip Technology Inc. 1995.

[3] A.I. Kayssi, K.A. Sakallah, T.M. Burks, "Analytical transient response of CMOS inverters." IEEE Trans. Circuit and Systems -I, vol.39, pp. 42-45. Jan. 1992.

[4] E.Y. Chung, B.H. Joo, Y.K. Lee, K.H. Kim and S.H. Lee, "Advanced Delay Analysis Method for Submicron Asic Technology.". Proc. of IEEE ASIC Seminar, 471-474, 1992.

[5] J. Qian, S. Pullela and L.T. Pillage, "Modeling the Effective Capacitance for the RC Interconnect of CMOS Gates." IEEE Transactions on Computer-Aided Design. 13(12):1526-1535, Dec. 1994.

[6] N. Menezecs, S.Pullela and L.T. Pillage, " Simultaneous Gate and Interconnect sizing for Circuit-Level Delay Optimization." Proc. of 32nd ACM/IEEE Design Automation Conference. 690-695, Jun. 1995.

[7] Dong-Wook Kim, Tae-Yong Choi, and Byoung-Kwon Jung, "A Delay Model for CMOS Inverter" Journal of The Korean Institute of Electronic Engineers, vol. 34 C, No.6 P357-367, Jun. 1997.

[8] 0.8-Micron Gate Array Library, VLSI Technology, INC, April 1992.

[9] Y. H. Bae, etc, "VHDL Based ASIC Design CAD System Supporting Manual & Automatic Design", World Korean Scientist Workshop, July. 1996.

[10] Neil H. E. Weste, Kamran Eshraghian, "Principle of CMOS VLSI DESIGN", Addison-Wesley, 1993.