A Study On the Retention Time Distribution with Plasma Damage Effect

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Abstract: The control of the data retention time is a main issue for realizing future high density dynamic random access memory. There are several leakage current mechanisms in which the stored data disappears. The mechanisms of data disappear is as fóllow, 1)Junction leakage current between the junction, 2) Junction leakage current from the capacitor node contact, 3)Sub-threshold leakage current if the transfer transistor is affected by gate etch damage etc. In this paper we showed the plasma edge damage effect to find out data retention time effectiveness. First we measured the transistor characteristics of forward and reverse bias. And junction leakage characteristics are measured with/without plasma damage by HP4145. Finally, we showed the comparison TRET with etch damage, damage_cure_RTP and hydrogen_treatment. As a result, hydrogen_treatment is superior than any other method in a curing plasma etch damage side.

Key words : Plasma, Damage, Retention, Time Distribution, hydrogen treatment.

1. INTRODUCTION

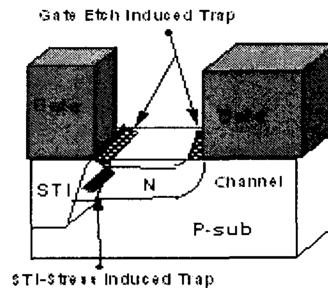
Improvement of the retention time distribution is a key problem for realizing future high density DRAM because the required refresh time doubles with each successive generation. Especially, electrical performance and data retention time may be significantly affected by damage introduced by plasma processed used in device manufacturing.[1][2]

Plasma etching technique is used mainly due to the reason that it can provide precise anisotropic etching. However, energetic atoms, ultraviolet photons, ions and electrons as well as large plasma-substrate potential difference can all have detrimental effects and potentially degrade the gate oxide in a device. There are two different types of damage resulting from plasma etching(oxide charging damage and plasma edge damage) which can degrade reliability of CMOS devices. Oxide charging damage, which arise due to electrical stress of thin gate oxide is the most widely known and studied type of damage. Since the effect of damage may be removed out by thermal annealing which removes the charge from the oxide and passivates the interface, damage becomes latent. Electrical parameters of fully processed devices do not show any degradation unless the gate oxide is broken due to plasma induced electrical stress and are similar for all processed devices, regardless of the amount of process induces charging damage. The other type of plasma damage, so-called plasma edge damage, which is due to direct exposure of device edges to plasma environment. Thus, edge damage may arise during poly-gate definition by plasma etching. In contrast to the charging damage, the edge damage dose not anneal even at high temperatures, leaving parameters of fully-processed devices significantly deteriorated.

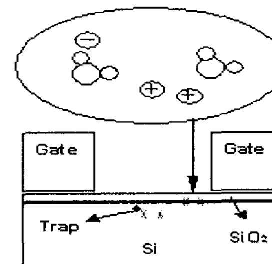
Therefore, the oxide charging damage is due to plasma induced Fowler-Nordheim current flowing through gate oxide,[3][4] while edge damage is due to direct plasma exposure during poly-Si overetch period.[5] It is therefore a major concern whether the damage can be removed during high temperature annealing and how the damage affects the device reliability.

Figure 1. shows the cross section of induced trap at gate etch. The effect of oxide electron trapping and interface state is enhanced trap density.

The nature of charging damage in the gate oxide of transistor is similar to that Fowler- Nordheim stress, when tunneling electron current is forced through the oxide.



(a)Cross section of the gate edge



(b)Electron or hole trap at gate oxide edge.

Figure 1. Plasma etch damage phenomena.

During the F-N current flow, several processes, responsible for oxide and transistor degradation, take place simultaneously. First, some of injected electrons are trapped on existing electron traps; at the same time holes generated by injected hot electrons are trapped on existing hole traps. Additionally, interface states are generated resulting in a high density of interface traps. In this paper we studied the plasma edge damage effect to find out data retention time effectiveness.

2. FABRICATIONS

After definition the field area and the active area. Shallow trench etching was performed after thin nitride layer was etched. Filling the trench gap with high density plasma oxide, and densification at high temperature, then CMP was carried out for planarization. Nitride and pad oxide were removed by wet etching. Channel ion implantation performed to control threshold voltage after high density plasma densification. The fabrication process of Cell nMOSFETs was based on L=0.18um with 7.0nm wet annealed oxide. The gate electrode was patterned by the KrF lithography. Then etched the gate electrode. And 65nm Si3N4 sidewall spacer was formed and then deep source /drain implantation(As) was carried out. The final process was RTA annealing at 1000 for 10seconds. And bit-line, capacitor, metalization, and annealing process performed (Skip, damage_cure_RTP, and hydrogen_ treatment).

3. EXPERIMENTAL AND DISCUSSION

Figure 2 shows the comparison Vgs vs Ids of the W/O(with out) and W/T(with) damage curve characteristic. W/O have no degraded along with forward and reverse forcing, but W/T damage have degraded along with forward and reverse forcing due to trap density. Also, we measured the junction leakage level as shown in Figure 3 Finally we measured data retention time at temp 87□. W/T damage data retention time is very poor than W/O damage as shown in Figure 4

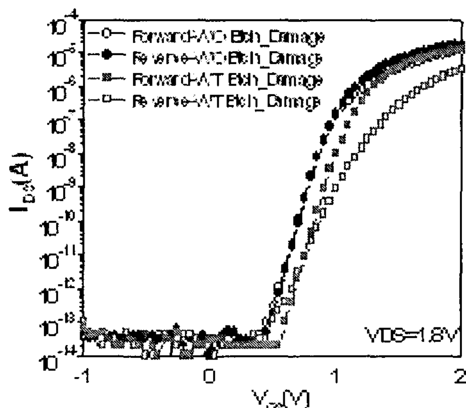


Figure 2. Forward and Reverse characteristics measurement by HP4145.

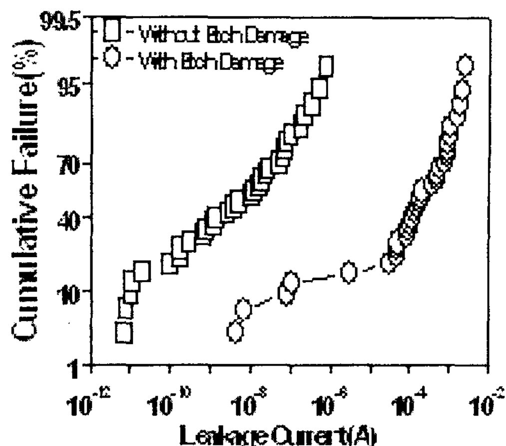


Figure 3. Comparison junction leakage characteristics measurement W/T and W/O plasma damage by HP4145.

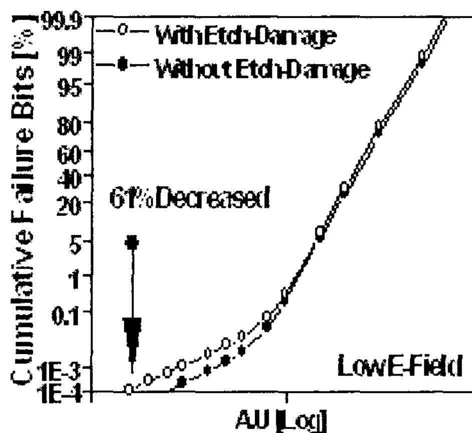


Figure 4. Comparison TREF W/T and W/O plasma damage effect.

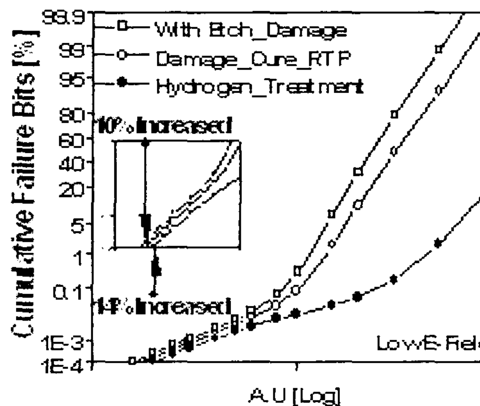
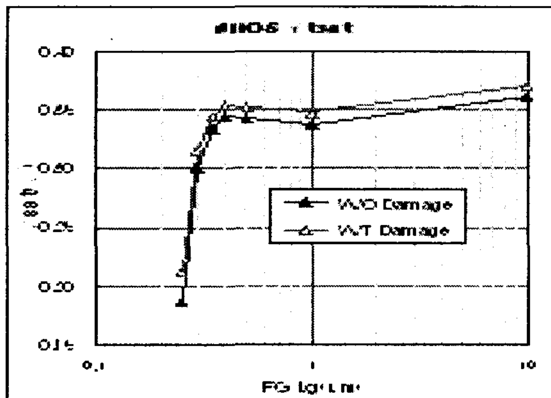
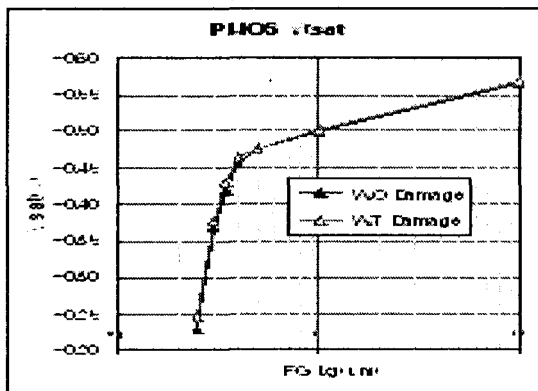


Figure 5. Comparison TREF W/T, damage_cure_RTP and hydrogen_treatment.

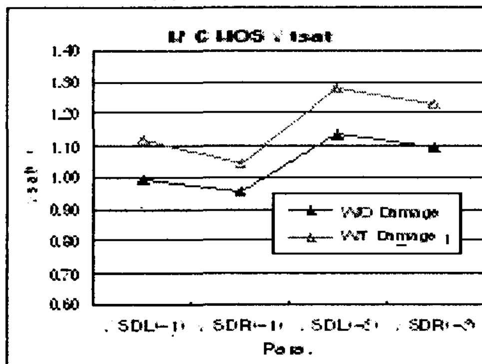
So, we added the damage_cure_RTP, or hydrogen_ treatment to compensate damage after PE-SiN deposition. As a result of curing process, data retention time is increased 10% (damage_cure_RTP), 14%(hydrogen_ treatment) than with plasma damage case(anneal skip) as shown in Figure 5 During the high temperature steps, following plasma processing in device manufacturing cycle, the charges trapped in the oxide(both electrons and holes) are removed, and broken interface bonds reconfigured(rebonded) and/or passivated.



(a) NMOS



(b) PMOS transistor.



(c) Main cell transistor.

Figure 6. The comparison with W/T and W/O plasma etch damage

Figure 6 shows the characteristic of NMOS, PMOS and Main cell transistor. In this Figure we can observed Vtsat lowering W/T plasma etch damage device than W/O. This is due to concentration segregation by plasma etch damage.

4. CONCLUSION

In this paper we showed the plasma edge damage effect to find out data retention time effectiveness. First we measured the transistor characteristics of forward and reverse bias. And comparison junction leakage characteristics are measured with/without plasma damage by HP4145.

Finally, we showed the comparison TRET with etch damage, damage_cure_RTP and hydrogen_treatment. As a result, hydrogen_ treatment is superior than any other method in a curing plasma etch damage side.

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