A Study on the Optimization of the Layout for the ESD Protection Circuit in 0.18um CMOS Silicide Process

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Abstract : Electrostatic discharge(ESD) is a serious reliability concern. It causes approximately most of all field failures of integrated circuits. Inevitably, future IC technologies will shrink the dimensions of interconnects, gate oxides, and junction depths, causing ICs to be increasingly susceptible to ESD-induced damage [1][2][3].
This thesis shows the optimization of the ESD protection circuit based on the tested results of MM (Machine Model) and HBM (Human Body Model), regardless of existing Reference in fully silicided 0.18 um CMOS process. This thesis found that, by the formation of silicide in a source and drain contact, the dimensions around the contact had a less influence on the ESD robustness and the channel width had a large influence on the ESD robustness [8].

1. INTRODUCTION

In recent year, the extensive use of VLSI device in high noise environments such as personal computers, automotive applications, and manufacturing control system has established the need for reliable ESD protection. However, advanced process development and increasing design complexity continue to provide new problems which often preclude the use of previous generation protection circuit technique.

Now, semiconductor devices are becoming more integrated, reliable, smaller as well as they are provided in various type of the packages. With this progress, the application field of VLSI products have been expanded significantly. On the other hand, the development of more sophisticated VLSI products makes the circuit design for protecting these semiconductor devices from the electro-static discharge (ESD) more difficult.

As the number of pins increases, the need for the reduction in size of the I/O circuit increase.

The protection circuit that can bypass the ESD stress efficiently while saving the space has been demanded.

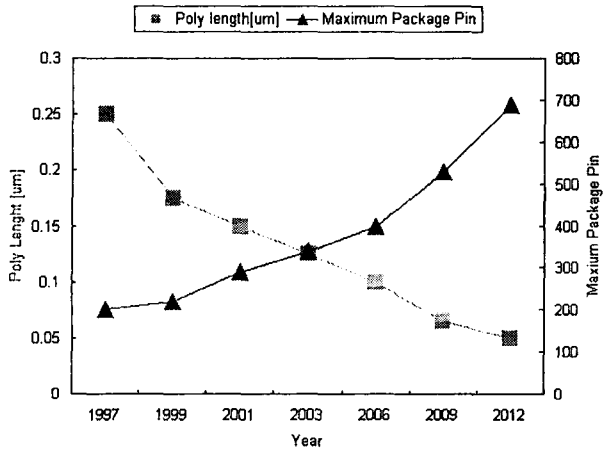


Figure 1. SIA Road Map

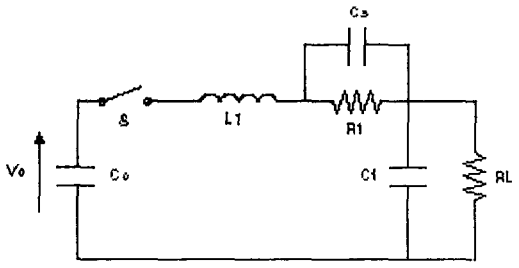
2. ESD TEST MODELING METHOD

2.1. Human Body Medel (HBM)

The HBM is the ESD testing standard, and is defined in the MIL-STD-883C method 3015.7.

The rise time is approximately 10 ns and the decay time is around 150 ns. The waveform is obtained by the discharge of a 100 pF capacitor with an initial voltage of 2 kV through a 1.5 resister. The HBM can be modeled using the RLC circuit shown in Figure 2 [11].

Figure 2. RLC circuit for HBM and MM



The discharge waveform of an HBM tester through a 0Ω load is shown in Figure 3.

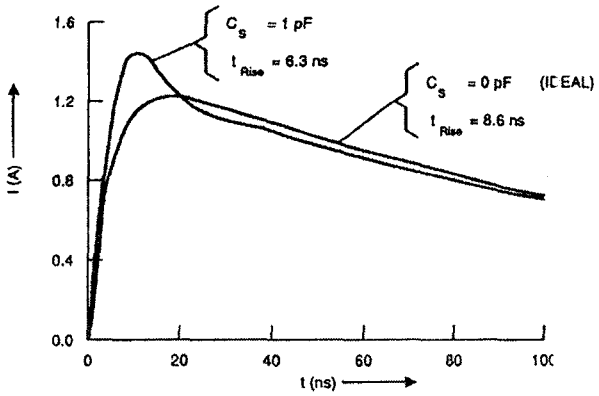


Figure 3. HBM discharge waveform through a 0Ω ESD voltage is 2 kV

The inductance and Parasitic capacitor are normally neglected in most of the models, However it does exist in all practical circuits, including the human individual, and has a limiting affect on the waveform rise time. The most commonly used RC components are 1.5 and 100 pF. We can simplify as Figure 4.

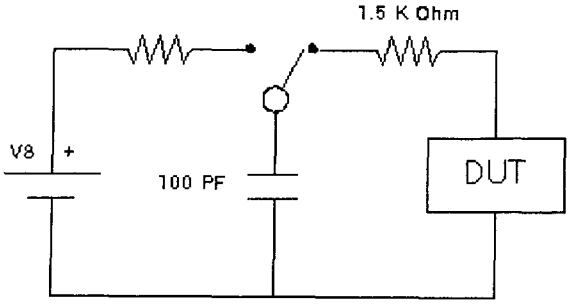


Figure 4. Simplified RC Circuit of HBM

2.2. Machine Medel (MM)

The machine model originated in Japan. The MM discharge circuit can be defined by the RLC network in Figure 2. is defined as 200 pF, while R1 is required to be 0 .

In practical circumstances R1 will be greater than 0 , during a discharge the dynamic impedance of the circuit can be much higher than 0. Hence, existing MM standards such as that presented by Philips[24] specify the output current waveform in term of peak current and oscillating frequency for a given discharge voltage.

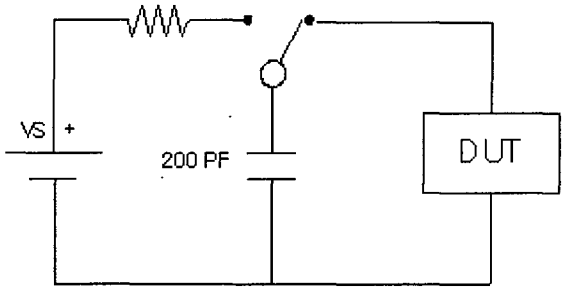


Figure 5. Simplified RC Circuit of MM

3. PROCESS CONDITION

The main feature on the process of the sample used in this experiment are shown below.

Main Parameter	
Channel Length	0.24 um
The gap of between Drain contact and Gate	0.5 - 2 um
The gap of between Source contact and Gate	0.5 - 2 um
The gap of between Source and Body	2 um
Silicide Process	Cobalt Silicidation
LDD Process	Y
Gate oxide film Tickness	5 nm
P/P+ epitaxial wafer (Epitaxial film tickness)	3 - 5 um
Shallow trench isolation (STI)	Y

4. EXPERIMENT

4.1. Contact-related Parameter

The following tree types of experiments were performed while varying the parameters related to the contact in drain region. An epitaxial substrate with a film thickness of 5 um was used in these experiments.

1. Variation of gate and contact
The distance between the gate and the contact was changed between 0.5 um and 2 um.

2. Variation of drain and contact
The distance between the contact and the drain side edge was changed between 0.5 um and 2 um.

3. Variation of the number of contact.
The number of contacts in the drain region was changed to 1/2 or 1/4

4.2. Channel width and Drain area Parameter

1. Variation of the channel width and Drain area
By deleting the drain contact partially, both channel width(W) and drain area(S) were changed to 1/3 the reference condition.

2. Variation of the Drain area
While keeping the channel width(W) at a constant value, only the drain area(S) was changed to 1/3 the reference condition.

.3. Variation of the Channel width
While keeping the drain area(S) at a constant value, only the channel width(W) was changed to 1/3 the reference condition.

5. RESULT AND CONSIDERATION

5.1. ESD result and consideration for 4.1

The MM results and the HBM result in Experiments of Chapter .a are shown in Figure 6 to 8 Figure 9 to 11, respectively. Each data is the average of five samples and the ESD application voltage limit of the equipment is 3000V. For the ESD robustness in the MM test (figure 6 to 8), the difference in ESD robustness was very little even if the distance between the gate and the contact, the distance from the contact to the drain side edge, and the number of contacts were changed within this condition variation. For the ESD robustness in the HBM test (Figure 9 to 11), an ESD robustness over 3000V was measured in all measuring points. It means that from the standpoint of the ESD, the size of a protection circuit can be reduced by using the minimum values of those contact related parameters.

Accordingly, as mentioned in the above, the ESD robustness is little dependent on the drain contact-related parameters. One of the causes is considered to be in the low contact resistance due to the use of silicide.

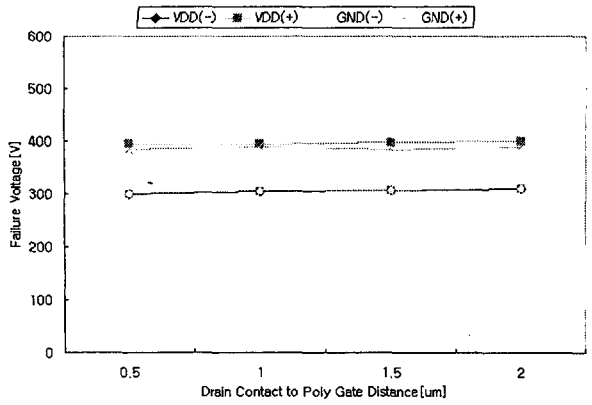


Figure 6. MM Result of the Dependency on the distance from gate to the contact

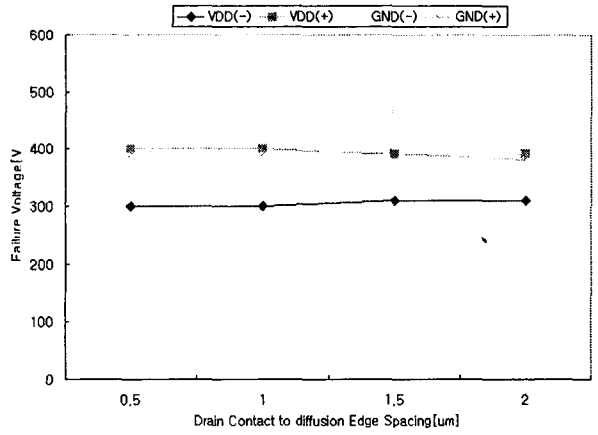


Figure 7.MM Result of the Dependency on the distance from the contact to the drain side edge

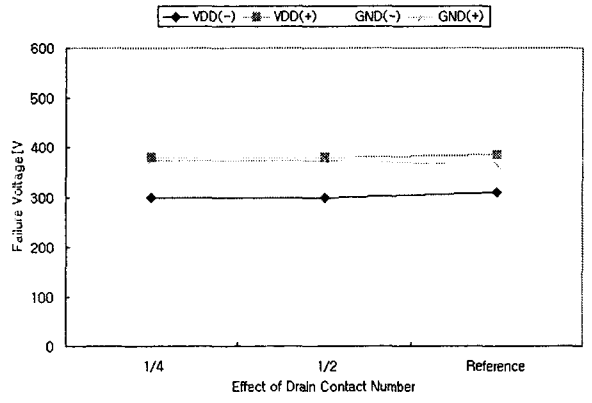


Figure 8. MM result of the Dependency on the number of contacts

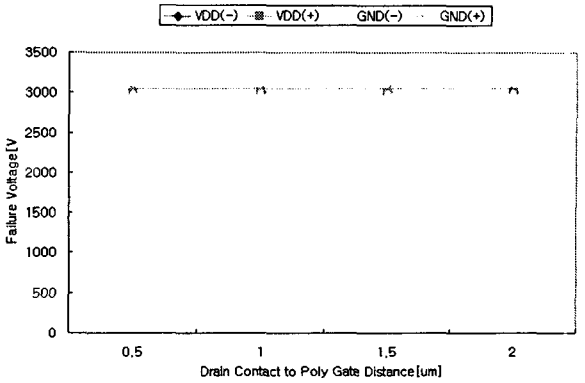


Figure 9. HBM result of the Dependency on the distance from the gate to the contact

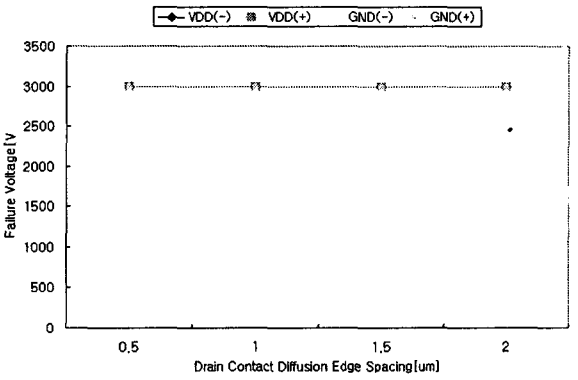


Figure 10. HBM Result of Dependency on the distance from the contact to the drain side edge

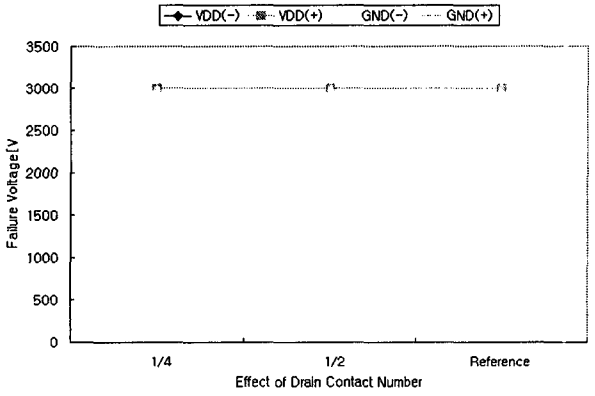


Figure 11. HBM Result of the Dependency on the number of contacts

5.2. ESD result and consideration for 4.2

5.2.1 Consideration of the MM result

The MM ESD robustness result (Take a look Figure 12 to 14) indicate that the ESD robustness indicated when both W(Channel width) and S(Drain area) were changed was equivalent to or higher than that indicated

when only S or W was changed, contrary to expectation that the ESD robustness indicated when both W and S were changed would be lower than that indicate when only S or W was changed. We consider that the cause of this result is in the structure of the circuit prepared for changing both W and S.

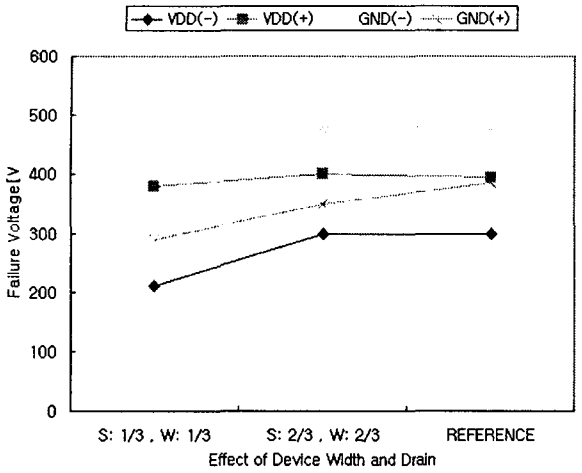


Figure 12. MM result of dependency on W&S

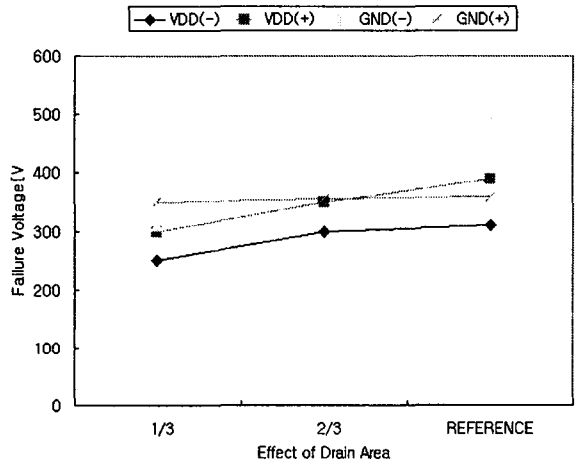


Figure 13. MM result of dependency on S

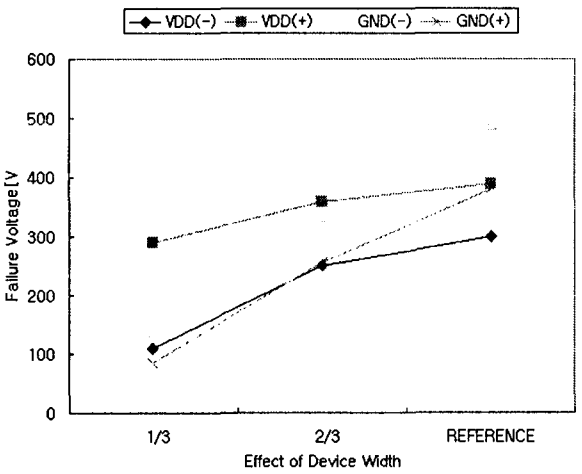


Figure 14. MM result of dependency on W

5.2.2 Consideration of the MM result

In all condition, the ESD robustness is 3000V or more up to 2/3 the reference except of VDD(-) in the W dependency test. In this condition variation range, the ESD robustness became low when the width is reduced to 1/3 the reference. From the test data obtained from the sample in which W is reduced to 1/3 reference, we know that the ESD robustness is largely influenced by the channel width W like the MM result.

Focusing on the W dependency result (take a look Figure 17), as indicated , the ESD robustness of GND(+) is reduced to 1500V abruptly when W is reduced to 1/3 the reference. As explained in the consideration of the MM results, the probable cause of this is that the LNPN is turned on less easily as W is reduced.

Next, let us focus on VDD(-). The slope in the graph reveals that VDD(-) is largely dependent on W. For VDD(-), the PMOS drain is reverse-biased due to the polarity of the application surge. Therefore, the LPNP us turned on and the ESD surge is by-passed.

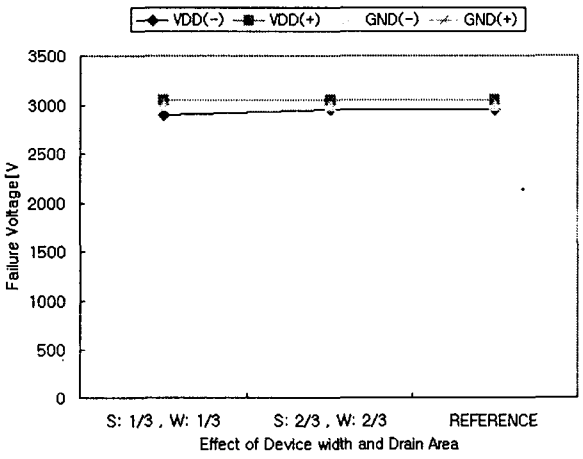


Figure 15. HBM result of dependency on W&S

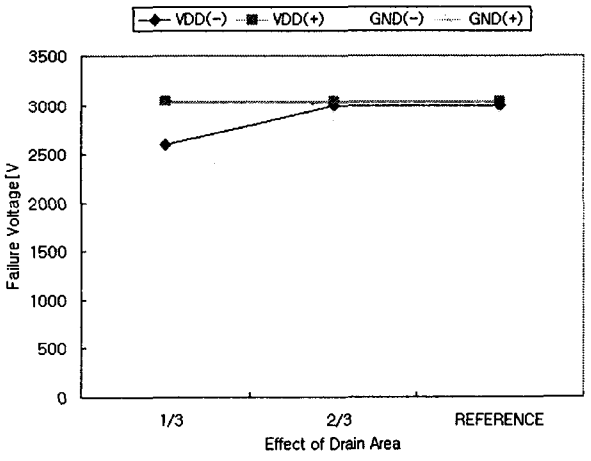


Figure 16. HBM result of dependency on S

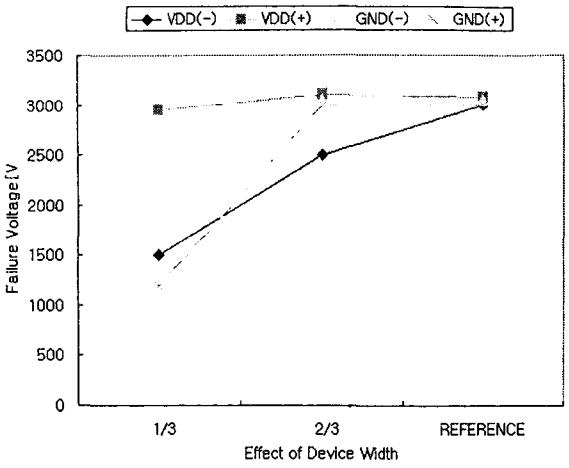


Fig. 17. HBM result of dependency on W

6. CONCLUSION AND FURTHER STUDY

We considered the optimization of a protection circuit from the result of this experiment. The test result shows the possibility of reducing the dimension around the contacts to sizes near the internal layout exceeding the condition variation in this test. This test also shows that there is no problem in ESD robustness even if the drain area S is reduced to 2/3 the reference. In addition, this test shows that it is difficult to reduce the channel with because the dependency of the ESD robustness on the channel width is the largest.

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