A Design of Analog Front-End for Noncoherent UWB Communication System

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Abstract:
In this paper, we propose a analog front-end (AFE) for noncoherent On-Off Keying (OOK) Ultra Wide Band (UWB) system based on power detection. The proposed AFE are designed using 0.18 micron CMOS technology and verified by simulation using SPICE. The proposed AFE consist of Sample-and-Hold block, Analog-to-Digital converter, synchronizer, delayed clock generator and impulse generator. The time resolution of 1ns is obtained with 100MHz system clocks and the synchronized 10-bit digital outputs are delivered to the baseband. The impulse generator produces 1ns width pulse using digital CMOS gates. The simulation results show the feasibility of the proposed UWB AFE systems.

Keywords: UWB (Ultra Wide Band), OOK(On-OFF keying), AFE(Analog Front End), S/H(Sample-and-Hold), A/D onverter, Impulse generator, Synchronizer. Flip-flop.

1. INTRODUCTION

The interest on wireless high-speed data communication with low power consumption is rapidly growing along with the development of various communication services. In order to satisfy the requirement of high-speed data rate and low power, UWB(Ultra Wide Band) is recently drawing the explosive attention. The official bandwidth allocation for commercial UWB system is processed by FCC(Federal Communication System) of United States in 2002[1]. And IEEE 802.15 Wireles Personal Area Network (W-PAN) Task Group 3a considers the UWB as transmission scheme for future W-PAN with high data rate over 100Mbps[2]. So the adoption of UWB system is accelerated.

For the realization of UWB system, low power consumption is essential. To meet this low power requirement, OOK modulation and noncoherent detection is one of good candidates in UWB system[3]. The noncohrent OOK UWB system may achieve degraded BER performance compared to the coherent system, but it could significantly relieve strict synchronization requirement in receiver part and provide the simplified transceiver structure with minimal power demand.

Typical wireless communication transceiver including UWB system consists of RF block, AFE(Analog Front End) and digital baseband block. The baseband block is implemented by single digital IC nowadays, however, RF block and AFE are implemented using discrete elements and a few ICs in many applications. Constructing a communication system using discrete elements or several ICs is not a good design approach in terms of power consumption. Because considerable power is dissipated in pad driving and signal amplification for external interface. Therefore, power consumption minimization requires the integration of all the analog blocks, RF blocks and digital baseband in a single chip. The single chip integration generally is carried out using CMOS process, but the performance of CMOS device could limit the RF block integration in high-speed communication system. On the other hand, current CMOS process increases the maximum operation speed of IC up to several GHz with reliable device performance. So designing UWB system using CMOS process is most probable approach in terms of power and integration.

In this paper, we propose the UWB AFE which plays an important role in bridging the RF block and baseband block and show the feasibility of the proposed UWB AFE with the results of simulation. The paper is organized as follows. The noncoherent architecture and AFE block description is explained in next section. In section 3, the simulation results of the proposed blocks are discussed. Finally, we finished with the conclusions.

2. ANALOG FRONT END DESIGN FOR UWB SYSTEM

2.1. AFE architecture for noncoherent UWB system

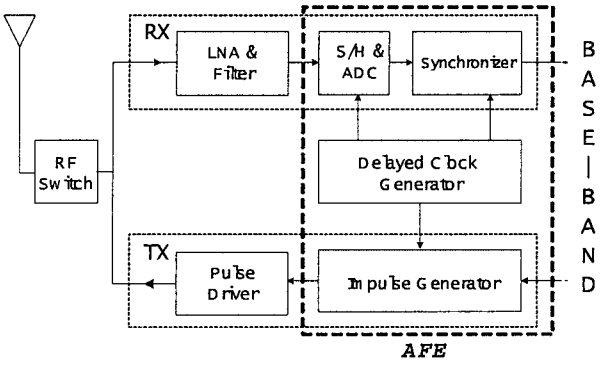

Fig. 1. Block diagram of typical analog sub-system for UWB communication

The impulse radio structure is suitable to UWB communication system[4]. The block diagram of typical analog sub-system for the impulse radio-type noncoherent UWB is shown in Fig. 1.

Typical wireless communication transceiver including the UWB consist of antenna, RF stage, AFE and baseband blocks. The AFE consists of Sample-and-Hold (S/H) circuit, A/D converter, synchronizer, delayed clock generator and impulse generator. The proposed design includes the RX part, TX part and delayed clock generator which makes several clocks for S/H block.

2.2. Impulse generator

The UWB communication system based on impulse radio architecture requires very narrow pulses whose width is below nanosecond typically. Simple and low power impulse generator is designed using current CMOS technology and pulse generation is carried out using several high performance digital gates. The block diagram of the proposed impulse generator is shown in Fig. 2.

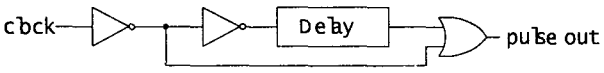

Fig. 2. Impulse generator

The proposed scheme generates impulses using the inverted signal and delayed signal from 100MHz system clock. The pulse width control is possible by controlling the delay of gate. The precise delay control is possible using the PLL block for system clock. The OR gate produces the final impulse from two signals and is composed of NOR and Inverter.

2.3. Sample-and-Hold and Parallelization

The data rate of UWB system is very high, so the parallelization is needed to interconnecting to baseband block. The parallelization reduces the speed of system clock and overcomes the limitation of current CMOS technology. The block diagram of parallelization block and S/H circuit are shown in Fig. 3.

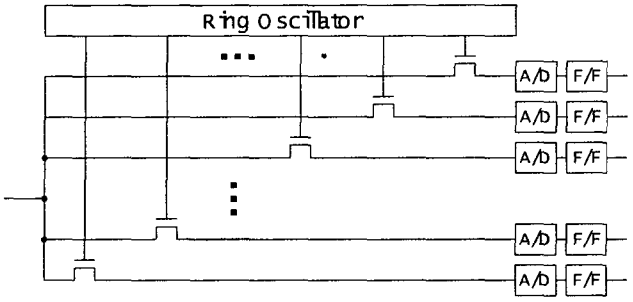

Fig. 3. Sample-and-Hold and Parallelization of high-speed RF-signal

The RF signal goes in from left port and is sampled by different clocks which are generated by the ring oscillator type delayed clock generator. As the parallelization row increase, the system clock speed goes down. But RF signal amplification should be considered for large number of parallelization, because the loading increases with the parallelization.

2.4. Delayed Clock Generator

Delayed clock generator is designed and its delay is controlled by the external voltage. Ring-oscillator architecture with frequency control is selected because the delay should be varied according to system clock. Total 10-stages are connected and differential signaling is used for oscillation. The delayed clock generator using ring oscillator architecture is shown in Fig. 4.

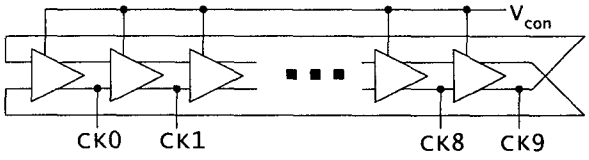

Fig. 4. Description is placed right below the figure.

The last stage output is crossed for ring oscillator operation, because the total stage number is not odd.

The delay cell used in the delayed clock generator is differential type and load PMOS are controlled by a voltage. The control voltage is not directly connected to "ctrl" and a few devices are used for voltage transferring from control voltage (V_{con}) to "ctrl". The schematic of delay cell is shown in Fig. 5.

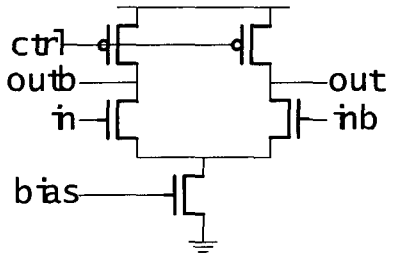

Fig. 5. The delay cell in the delayed clock generator

2.5. Analog-to-Digital Converter

The RF stage delivers analog signal, but most of baseband is processed in digital manner. So the Analog-to-Digital conversion is necessary for modern communication system. We propose a simple and appropriate 1-bit A/D converter with S/H circuit. The A/D converter and synchronizer is shown below. The A/D converter circuit is similar to a sense amplifier in memory, and signal comparison and amplification is carried out. Fig. 6. shows the schematic of 1-bit A/D converter and RF low pass filtering circuits.

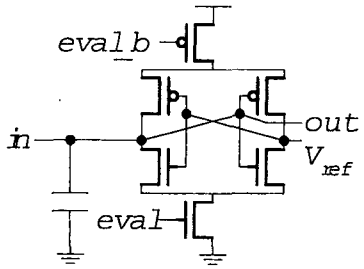

Fig. 6. A/D converter with low pass filtering

The capacitor which is connected to input port is for low pass filtering. The sampled RF signal is stored in capacitor and the stored value is used for digital conversion. The capacitor widens the width of short RF pulse, so the signal comparison and amplification is carried out with proper speed.

2.6. Synchronizer

The edge triggered D-type flip-flop is used for synchronizing the parallelized signals. The outputs of A/D converters are not synchronized, because the S/H blocks uses the different clocks for parallelization. Using the synchronizer, the 10-bit synchronized outputs are delivered to a baseband without the problem due to the delayed clocks which are used for parallelization. The schematic of D flip-flop used in this synchronizer is shown in Fig. 7.

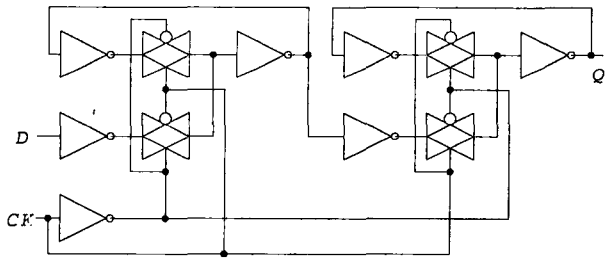

Fig. 7. Schematic of D-F/F for synchronizer

3. SIMULATION RESULTS

The proposed AFE is designed and verified using 0.18 micron CMOS technology. Simulations are performed using SPICE and assisted by ADS in case of high speed RF signals. The simulation result of each sub-block follows.

3.1. Impulse Generator Simulation

The simulation result of impulse generator is shown in Fig. 8. Using the schematic in Fig. 2, about 1-ns pulse is generated.

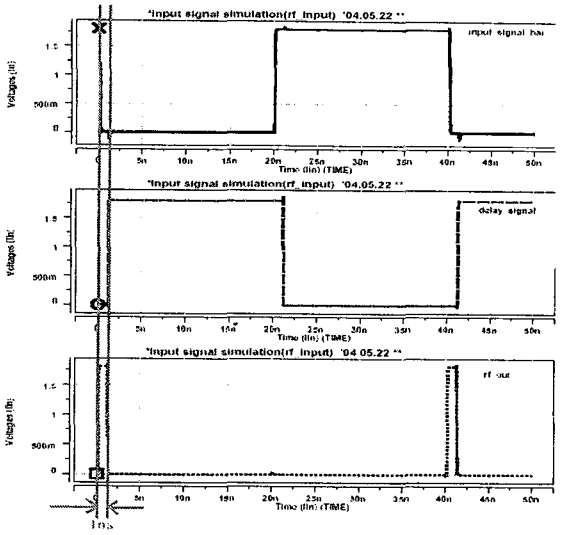

Fig. 8. Impulse generator simulation

3.2. Delayed Clock Generator Simulation

The simulation result of the delayed clock generator is shown Fig. 9. The 1st, 2nd and 3rd clocks are displayed and delay times between clocks are about 1ns. Ten clocks are generated and those clocks are used in S/H blocks. The time delay is controlled by the control voltage, and the control voltage could be cooperated with PLL for future implementation.

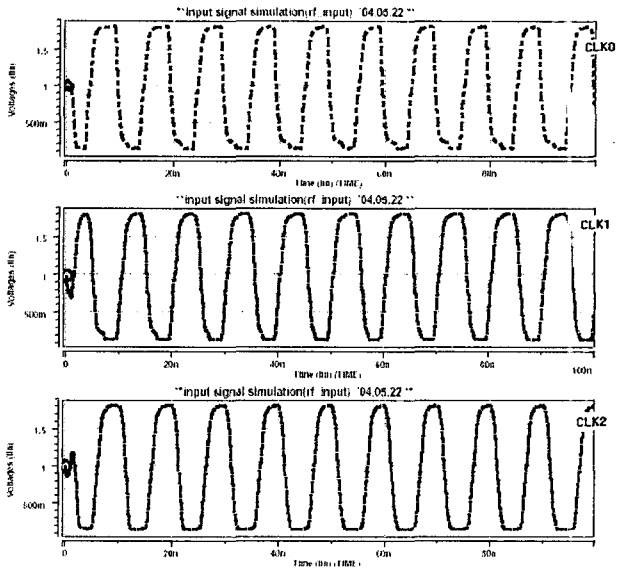

Fig. 9. Simulation result of delayed clock generator

The output of delayed clock generator is not strong enough to control sample-and-hold circuits, so inverter type buffers are inserted at the output of delayed clocks. The signal waveforms after passing buffers are shown Fig. 10. The 1st, 2nd and 3rd signal of ten clocks are also plotted.

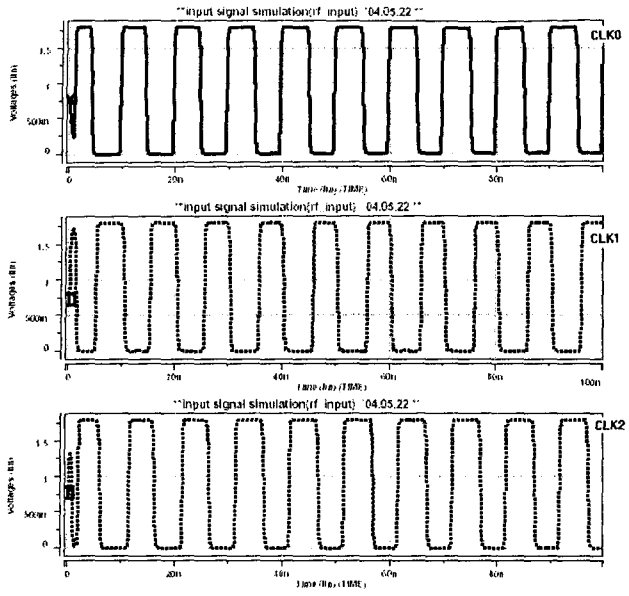

Fig. 10. Delayed clocks after passing buffers

3.3. Sample-and-Hold and A/D Converter Simulation

The result of the S/H block and 1-bit A/D converter is shown in Fig. 11 and four of 10 parallelized signals are plotted. The received pulse is compared to the reference voltage and converted to binary values. Low-pass filtering circuits are used to guarantee the enough time for the comparator of A/D converter. The time resolution of AFE is very important in noncohrent UWB system because the limitation of data rate and the accuracy of location are dependent on it. The high resolution in time is achieved by parallelization, so the desired resolution is dependent on the number of parallelization. But the hardware overhead and clock skew should be considered in parallelization

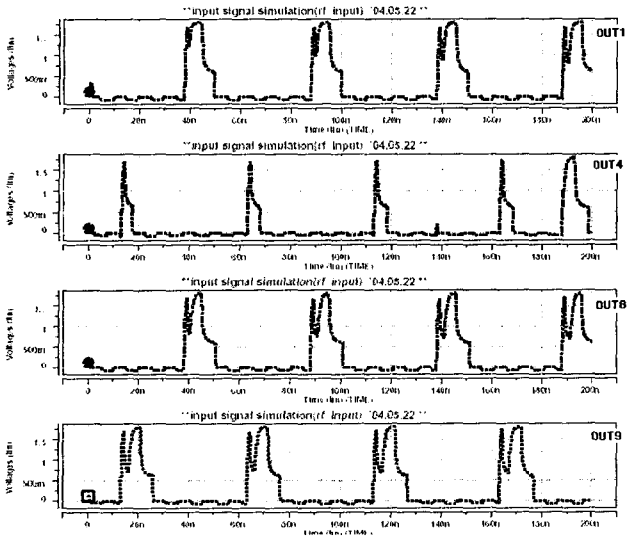

Fig. 11. Simulation result of S/H and A/D converters

3.4. Synchronizer Simulation

The parallelized outputs of A/D converters are not synchronized due to the delayed clocks for sampling, so the D-type flip-flop is used for the synchronization. The synchronized outputs of flip-flops are shown in Fig. 12.

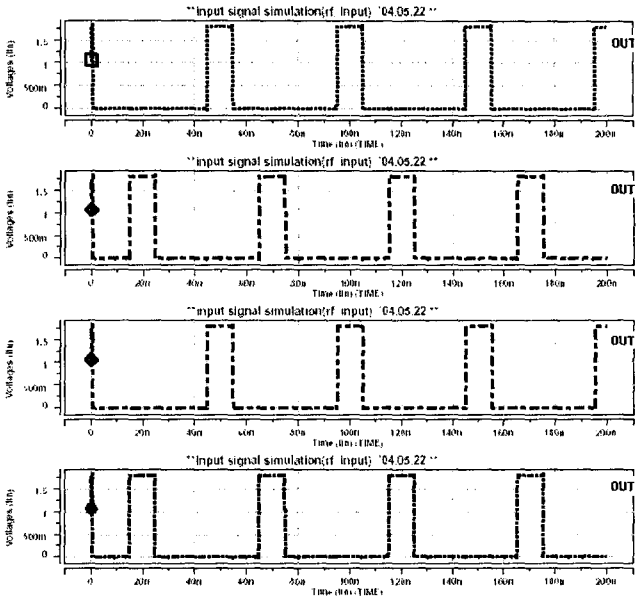

Fig. 12. The synchronized outputs using flip-flops

Four output signals (OUT1, OUT4, OUT8, OUT9) from the ten parallelized outputs are plotted above figure. The simulation result shows that the signals are properly synchronized and those are applicable to baseband interfacing.

4. CONCLUSIONS

In this paper, we proposed and verified the AFE for noncoherent UWB system based on power detection. It was observed that the proposed UWB AFE could generates 1ns duration impulse and receives RF signal with 1ns time resolution, so the 1Gbps data rate transfer is possible using the proposed AFE. The output parallelization is carried out using ten clocks which are delayed about 1ns one another. So the 1Gbps data could be processed by the baseband of 100MHz system clock. The RF signal is converted to digital binary value with the help of A/D converter and low pass filtering circuits.

The result shows that the proposed AFE is suitable for the noncoherent UWB system and its operation is verified with the output of the impulse generator which is proposed above as the input signal. Simulation including RF blocks will be required for more accurate verification.

The AFE blocks for noncoherent UWB transceiver are designed and verified by simulation using CMOS technology. Simulation results on the impulse generator, delayed clock generator, and 1-bit Analog-to-Digital converter with synchronizer show the feasibility of the proposed UWB AFE system.

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