A Half-VDD Voltage Generator for Low-Voltage DRAM

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Abstract

A Half-VDD Voltage(VHDD) Generator using PMOS pull-up transistor and NMOS pull-down transistor was newly proposed for low-voltage DRAMs. The driving current was increased and the power-on settling time was reduced in the new circuit. The newly proposed VHDD generator worked successfully at VDD at 1.5V and fabricated using 0.18um CMOS twin-well technology.

1. Introduction

Low voltage operation in high density, high speed and mobile DRAMs is essential to minimize the power consumption and to guarantee the reliability of the devices as critical dimension decreases. Supply voltage of recent low voltage DRAMs is 1.8V and is expected to migrate toward 1.5V or even further in the near future [1].

VHDD(Half-VDD) Voltage Generator is used as cell-plate and bit-line precharge voltage in DRAMs. Fig.1 shows conventional VHDD voltage generator. It consists of voltage driver, bias stage, push-pull current mirror amp and push-pull output stage.

When operation, at output stage, maximun pull-up current is directly proportional to $(VCORE/2-V_{TN})^2$ and maximum pull-down current is directly proportional to $(VCORE/2-|V_{TP}|)^2$. VCORE means core voltage for DRAM cell array.

As DRAM goes high density, total bit-line and cell-plate load capacitance increase. And NMOS pull-up driving current capacity dramatically decrease, so VHDD settling time takes longer during power on.

In this paper, we proposed new VHDD (Half-VDD)

Voltage Generator having high driving current under 1.5V as Fig.2. It use PMOS pull-up transistor and NMOS pull-down transistor, and it worked successfully under 1.5V in 0.18□ CMOS technology from simulation result.

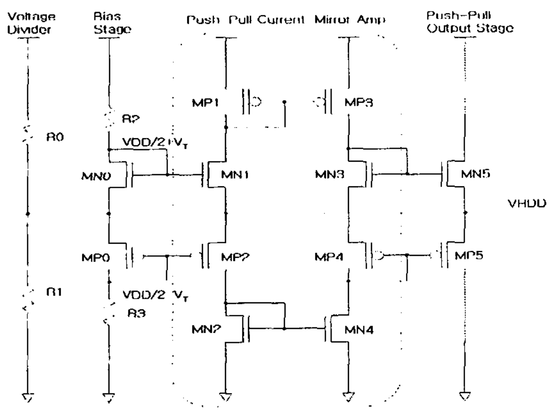

Fig.1. Conventional VHDD Voltage Generator

2. Circuit Design

Newly proposed VHDD(Half-VDD) Voltage Generator consists of Reference Voltage Generator, two Differential Amplifier (DIFF0, DIFF1), two inverter buffer (INV0, INV1, INV2, INV3), Short-Circuit current protection circuit, pull-up transistor (MP6), pull-down transistor (MN6) and high impedance voltage divider (MP7, MP8).

In this new VHDD(Half-VDD) Voltage Generator circuit, two inverter buffer make that gate voltage of pull-up and pull-down transistor swings as CMOS level.

Pull-up driving current is in proportion to $(VDD-|V_{TP}|)^2$ using PMOS pull-up transistor, pull-down driving current is also proportion to $(VDD-V_{TN})^2$ using NMOS pull-down transistor.

Reference voltage generator makes VREFU (VHDD+'V) and VREFL (VHDD-'V).

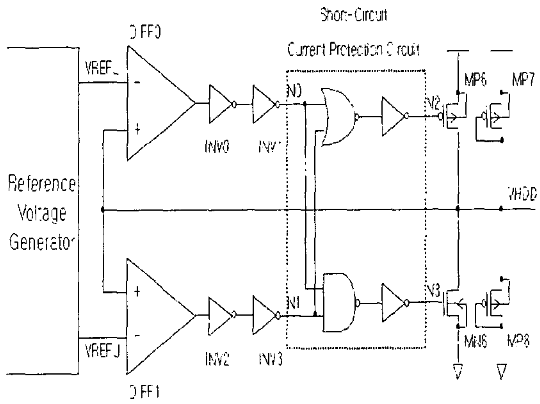

Fig.2. Newly proposed VHDD Voltage Generator

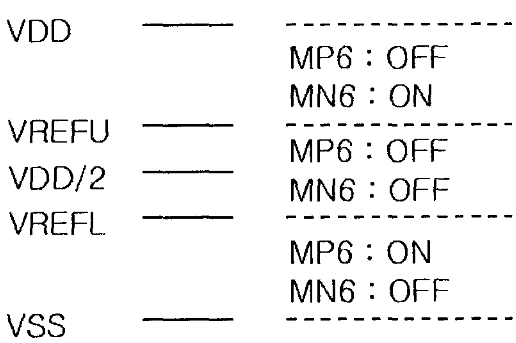

Fig.3. Switching state of VHDD pull-up/pull-down transistor.

Fig.3 shows switching stage of VHDD pull-up / pull-down transistor. When VHDD is lower than VREFL, pull-up transistor MP6 makes VHDD voltage level rise (MP6 transistor turns on and MN6 transistor turns off). When VHDD is upper than VREFU, pull-down transistor MN6 makes VHDD voltage level fall (MP6 transistor turns off and MN6 transistor turns on). If VHDD stay between VREFU and VREFL, MP6 and MN6 turn off, VHDD level is settled as VDD/2 with voltage divider (MP7, MP8).

Logic gate is added to prevent short circuit current caused by offset voltage in Differential amplifier.

N0	N1	N2	N3	MP6	MN6
0	0	0	0	ON	OFF
0	1	1	0	OFF	OFF
1	0	1	0	OFF	OFF
1	1	1	1	OFF	ON

Table 1. Truth table of N0, N1, N2, N3 node

Table 1 shows logic levels of N0, N1, N2 and N3 nodes. When VHDD is lower than VREFL, output states of DIFF0 and DIFF1 is "Low" level, N0, N1, N2 and N3 is 0V. Since MP6 turns on and MN6 turns off, gate and source voltage gap of pull-up transistor is VDD, driving current of pull-up transistor is in proportion to $(VDD-|V_{TP}|)^2$.

When VHDD is upper than VREFU, output stage of DIFF0 and DIFF1 is "High" level, N0, N1, N2 and N3 is VCORE. Since MP6 turns off and MN6 turns on, gate and source voltage gap of pull-down transistor is VDD, driving current of pull-down transistor is in proportion to $(VDD-V_{TN})^2$.

When VHDD stay between two levels, N0 is "High" and N1 is "Low", N2 is "High" and N3 is "Low", both MP6 and MN6 transistors turn off.

But, sometimes it could happen that output level of DIFF0 is "Low" and output stage of DIFF1 level is "High" caused by offset voltage of Differential Amplifier. Then MP6 and MN6 transistor turn on, it makes short circuit current. So, to prevent turn on two transistors (MP6, MN6) at once, we add short circuit current protection circuit. Though N0 is "Low" and N1 is "High", short circuit current protection circuit makes N2 and N3 is "High" and "Low". So when VHDD stay between two levels, both MP6 and MN6 always turn off without regard for offset voltage.

When both two pull-up / pull-down transistors turn off, voltage divider (MP7, MP8) make VHDD as VDD/2 and prevent VHDD to floating state. PMOS diode or NMOS diode, or resistor be used in Voltage divider. It should be designed having high impedance to reduce stand-by current.

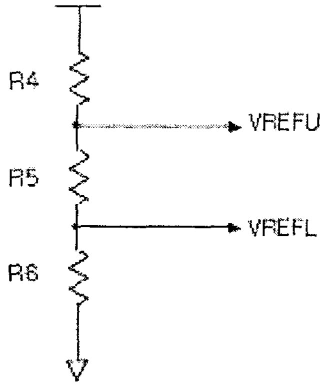

Fig.4. Reference voltage generator using voltage divider.

Reference voltage generator can be used Bandgap reference voltage generator [2]. In this paper, register divider type was used for reference voltage generator.

VREFU and VREFL is expressed as equation (1),(2)

$$VREFU = \frac{R5+R6}{R4+R5+R6} \times VDD \qquad (1)$$

$$VREFL = \frac{R6}{R4+R5+R6} \times VDD \qquad (2)$$

According to this equation, it is made VREFU as 0.775V (0.75+0.025V) and VREFL as 0.725V (0.75-0.025V) at VDD = 1.5V.

3. Simulation result

Fig.5 shows simulation result of current driving power, when VHDD swings from 0V to 1.5V at VDD=1.5V. Fig.6 shows simulation result of VHDD settling time during power-on. As you see, the driving current is increased and the power-on settling time is reduced in the new circuit.

It was tested connecting with 8 loading capacitance for 256M DRAM in 0.18□ CMOS technology. Simulation result of power-on settling time reduced from 150 to 60 .

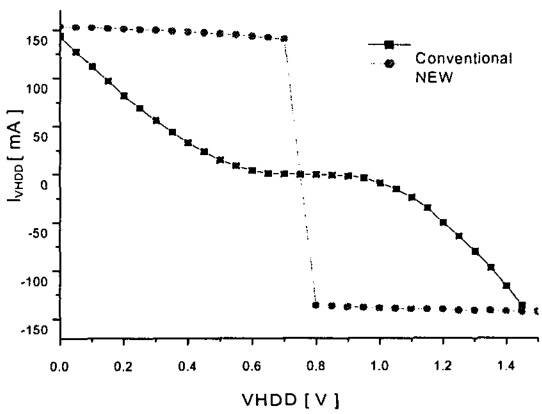

Figure 5. Simulation result of VHDD current driving power at VDD=1.5V

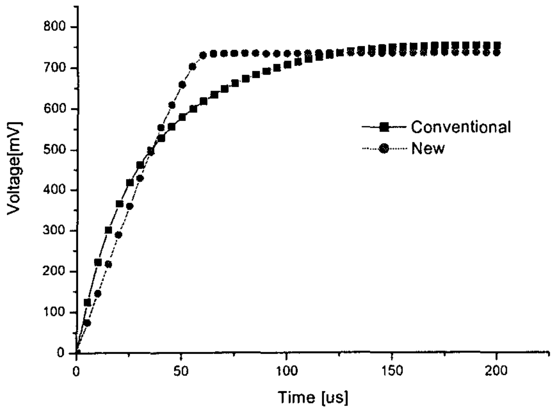

Figure 6. Simulation result of VHDD power-on settling time

4. Conclusion

This paper proposes Half-VDD voltage generator with high driving current using PMOS pull-up transistor and NMOS pull-down transistor, and voltage target is 0.75V at VDD=1.5V. This new circuit worked successfully, and power-on settling time reduced from 150□to 60□in 0.18□ CMOS technology.

References

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