A Voltage-Down Converter for Low-Voltage SoC

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Abstract:

This work is the study of Voltage-Down Converter used as internal supply voltage having large current driving and stable voltage level at any variation of process, voltage, and temperature(P.V.T). It converts VDD(external supply voltage) into V_{INT}(internal supply voltage). From the simulation results, a new Voltage-Down Converter has large current driving and a little stand-by current under lower supply voltage than conventional circuit. And bad characteristic of VINT, peaking, was eliminated. Start-up circuit for BGR is also added to one circuit, which consumes less current dissipation than convention circuit

I. Introduction

Nowadays, memories and system IC products have been produced by 0.13~0.35□ design rule and it is being developing by under 0.1□, which it is called nano technology. As the design rule is downsized and VDD is also being tended downward 1.5V, low voltage operation is essential to maintain the reliability of the small devices. But users try to preserve the same VDD. On-chip Voltage-Down Converter solves the complicated matter between maker and user. In other words, it provides makers chance to use lower VDD and provide users stable V_{INT}. On the chip, VDD is decreased so as to reduce the active power consumption. Current driving is also decreased as VDD is reduced. That causes output voltage of Voltage-Down Converter to have narrow active margin. Regardless of supply voltage, the settled voltage, V_{INT} having large current driving is needed when chip becomes active mode.

In this work, a new voltage down converter is proposed to solve the above problem using newly proposed start-up and V_{INT} circuits.

II. Circuit Description

A conventional Voltage-Down converter consists of BGR with two start-up circuits, voltage-up converter, and V_{INT} driver as shown in the block diagram of Fig. 1. [2]

The core of designing Voltage-Down Converter is to design the insensitive BGR circuit to P.V.T. the variation of **Vref** on VDD, temperature and process.

The others are reducing the stand-by current and supplying the V_{INT} voltage having stable and exact level as load current changes fast.

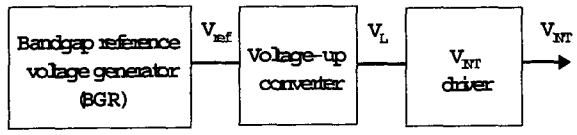

Fig.1. Conventional Voltage-down Converter Block diagram for Low-voltage SoC

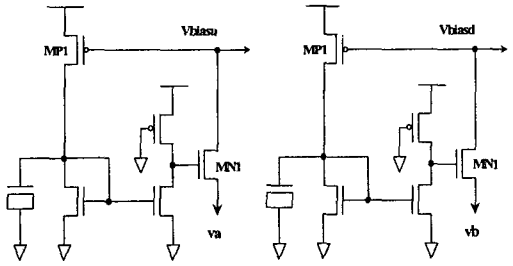

Fig.2. Conventional start-up circuit.

Fig.2 is a start-up circuit used for BGR.[1] During the power-up, if node vbiasu and vbiasd follow VDD, the bias current will reach to zero, so BGR does not operate properly. Start-up pulls out the charge of node vbiasu and vbiasd till stable voltage level. The BGR needs one start-up circuit for each node, vbiasu and vbiasd, which brings current increase.

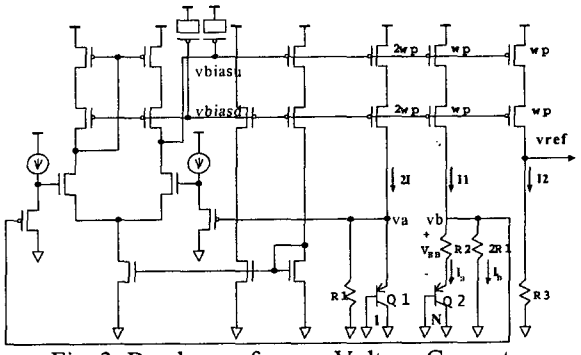

Fig. 3. Bandage reference Voltage Generator

(Vref) circuit with differential op amp and cascode current mirror. BGR shown in Fig.3 makes an invariable voltage irrespective of VDD, temperature and process. It makes stable voltage within 1.3V~1.4V VDD.[1]

Principal of BGR is to always generate steady current by appropriately summing negative V_{EB} and positive V_T on temperature. **Vref** is simply handled by multiplying current and resistor. Ratio of bipolar transistor is used 1:10. Target voltage of Vref is 0.75V. And **Vref** is express as (1) [1]

$$Vref = R3 \cdot I2 = R3 \cdot (\frac{V_{EB}}{R2} + \frac{V_T \cdot \ln N}{R1}) \quad (1)$$

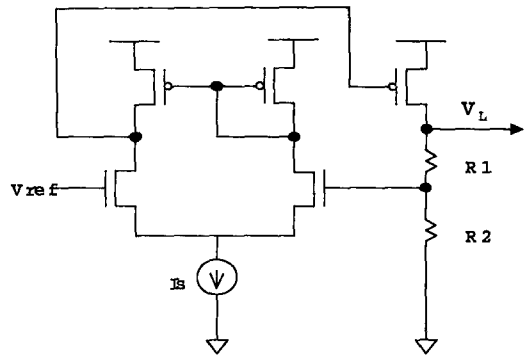

Fig. 4. Voltage-up converter circuit using resistors

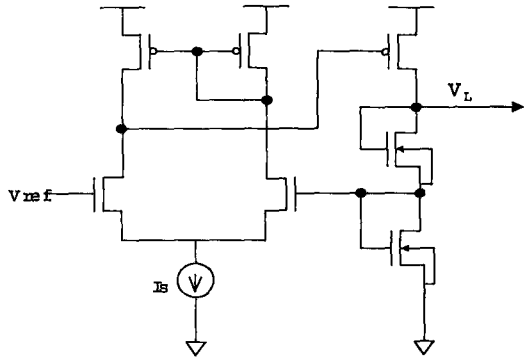

Fig. 5. Voltage-up Converter circuit using NMOS transistors.

Voltage-up converter is used to converter vref into internal supply voltage level. Fig.4 shows that it generates V_L shown as (2).

$$V_L = Vref \cdot (1 + \frac{R1}{R2}) \quad (2)$$

Due to possibility of process variation, Vref can be changed and that makes V_L out of target level. So Fuse-trimming method can solve this problem by controlling ratio of R1 to R2. [2],[4] Fig. 5 is another voltage-up converter using MOS figured diode instead of resistor. V_L is **2·Vref** when using same size NMOS transistors.

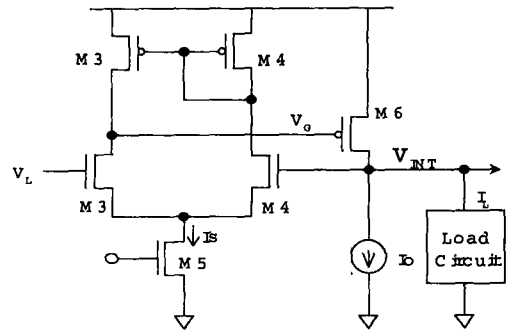

Fig. 6. Conventional V_{INT} Driver circuit

Conventional V_{INT} driver consists of differential amplifier transistors (**M1-M5**) having current-mirror active load and common source driver, PMOS transistor (**M6**).[3] The PMOS transistor length must be wide enough to supply load current. Moreover output voltage V_{INT} decreases by ΔV_{INT} when the output load current changes fast. In order to minimize the variation of V_{INT} level, V_G, gate voltage of **M6** transistor, must make response fast when V_{INT} fall down. This is possible by increasing the I_S. Bias current, **Io** plays a role in clamping V_{INT}. A conventional Voltage-Down Converter has bad current driving on low supply voltage. In this case, Maximum voltage V_G of common source driver, PMOS transistor, has **VDD-(V_L-V_T)**. And differential pair NMOS transistors (M3 and M4) of the differential amplifier go into linear region and do not function as an amplifier when VDD nearly becomes V_{INT} level. Hence it brings peaking of V_{INT}, which gives a bad electrical characteristic to IC product.

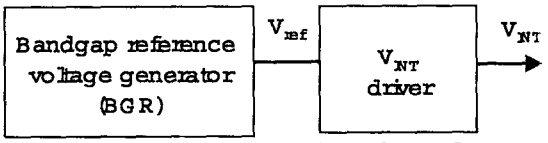

Fig. 7. A newly proposed Voltage-Down Converter block diagram for low-voltage SoC.

Fig. 7. is a newly proposed Voltage-Down Converter, which consists of BGR and V_{INT} driver. The voltage-up converter was eliminated in total circuit. Therefore current dissipation lessened.

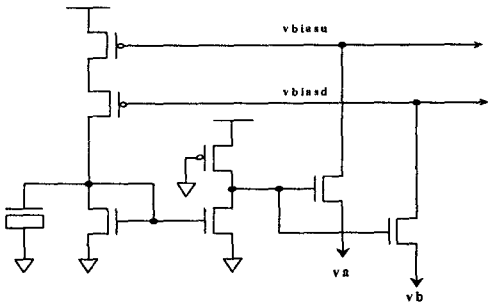

Fig. 8. Newly proposed start-up circuit for BGR

The cascode typed start-up in Fig. 8 is newly designed to decrease current dissipation by putting together node vbiasu and vbiasd in one circuit. It reaches the steady state faster than conventional type as separated each other.

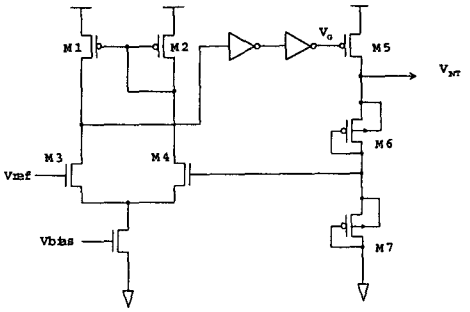

Fig. 9. Newly proposed V_{INT} driver circuit.

Fig.9 is a newly proposed V_{INT} driver. Not only it has voltage-up converter function but also larger current

driving capability. The V_{INT} driver generates V_{INT} 1.5V, 2·**Vref**, through input of Vref. By using two inverters, final output voltage, V_G of the differential amplifier is changed into CMOS level. Compared with conventional type, V_G becomes to have range 0 to VDD. This causes PMOS transistor (M5) to supply more current driving capability than conventional type.

III. Simulation Results

To verify the operation of the newly proposed Voltage-Down Converter, Fig.10 and Fig.11 are the curves showing node vbiasu and vbiasd states during power-up.

Peaking of V_{INT}, when VDD is near to V_{INT} as shown in Fig. 13, is eliminated and the reliability of V_{INT} is improved. Fig. 14 shows that a newly proposed one has much more current driving than conventional type around V_{INT}, 1.5V. The tested chip is being fabricated.

IV. Conclusion

Voltage-Down Converter's use having low power and low voltage is indispensable as nano technology below 0.1□ becomes widespread.

This thesis proposes a new Voltage-Down Converter. Two start-up circuits became one circuit. The start-up is more steady and faster than before as shown in Fig.10 and Fig.11. As putting together function of voltage-up and V_{INT} driver in a circuit, chip size become smaller and current dissipation was lessened. V_{INT} current driving ability is superior to conventional type around VDD, 1.5V. The BGR circuit also works well under VDD, 1.5V on temperature. The target voltage of **Vref** is 0.75V and V_{INT} is 1.5V. Current is limited under 15□ in BGR circuit with a start-up.

On the basis of 0.18□ CMOS process , all the above were verified through simulations and the test chip is being fabricated using 0.18□ CMOS process. The BGR circuit using the newly proposed start-up circuit and the newly proposed Voltage-Down Converter are being applied for a patent with simulation results. From the simulation results, it is expected to be suitable for source for Low-Voltage SoC.

After fab-out, measurement will be performed and verified.

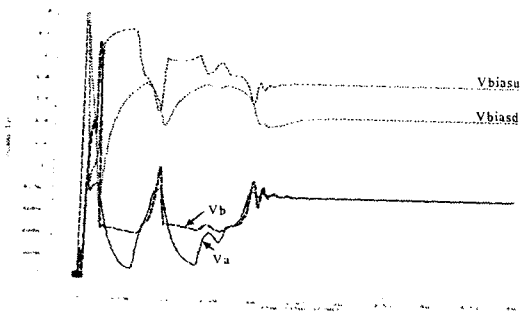

Fig. 10. Conventional Start-Up Simulation result of vbiasu and vbiasd.

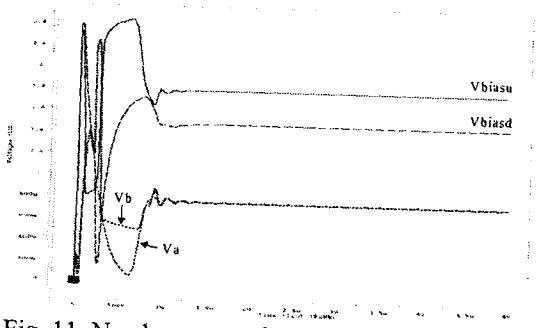

Fig. 11. Newly proposed start-up simulation result of vbiasu and vbiasd.

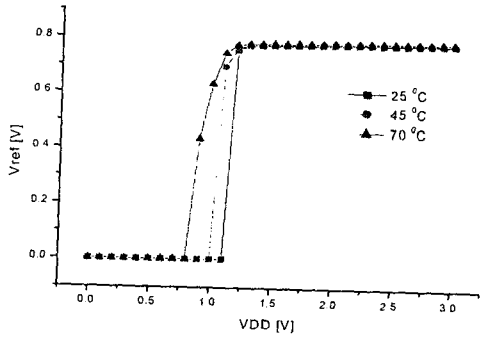

Fig. 12. Simulation results of Vref for the BGR with temperature variations.

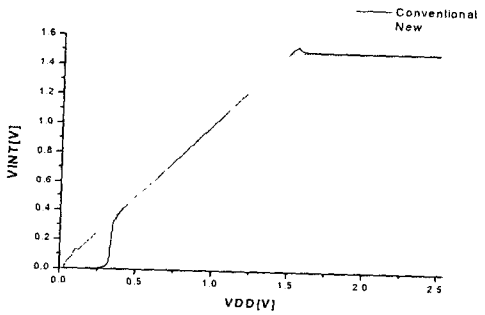

Fig. 13. V_{INT} level of Voltage-Down Converter as VDD goes up.

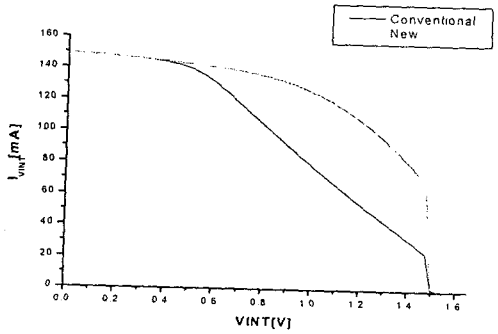

Fig. 14. Current driving capability as V_{INT} changes at VDD=1.5V.

Acknowledgement

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V. References

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[3] M. Horiguchi et al., Dual-Regulator Dual-Decoding-Trimmer DRAM Voltage Limiter for Burn-in Test, IEEE J. Solid-State Circuits, vol. 26, pp. 1554-1549, Nov. 1991

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