A Study on Single-bit Feedback Multi-bit Sigma Delta A/D converter for improving nonlinearity

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Abstract

This paper presents multibit Sigma-Delta ADC using Leslie-Singh Structure to Improve nonlinearity of feedback loop. 4-bit flash ADC for multibit quantization in Sigma Delta modulator offers the following advantages such as lower quantization noise, more accurate white-noise level and more stability over single quantization. For the feedback paths consisting of DAC, the DAC element should have a high matching requirement in order to maintain the linearity performance which can be obtained by the modulator with a multibit quantizer. Thus a Sigma-Delta ADC usually adds the dynamic element matching digital circuit within feedback loop. It occurs complexity of Sigma-Delta Circuit and increase of power dissipation. In this paper using the Leslie-Singh Structure for improving nonliearity of ADC. This structure operate at low oversampling ratio but is difficult to achieve high resolution. So in this paper propose improving loop filter for single-bit feedback multi-bit quantization Sigma-Delta ADC. It obtained 94.3dB signal to noise ratio over 615kHz bandwidth, and 62mW power dissipation at a sampling frequency of 19.6MHz. This Sigma Delta ADC is fabricated in 0.25um CMOS technology with 2.5V supply voltage

Key Words : Sigma Delta modulation, ADC, Single-bit Feedback, Stability

1. INTRODUCTION

The emergence of powerful digital signal processors implemented in CMOS technology creates the need for high-resolution Analog-to-Digital Converters(ADC) that cad be integrated in fabrication technologies optimized for digital circuits and systems.

A sigma-delta ADC, that perform over-sampling and Noise Shaping technique, is the most suitable at low speed A/D conversion and high resolution for voice and audio signal processing. The resolution of sigma delta ADC is related to Signal to Noise Ratio(SNR) characteristic. There are three ways to increase the resolution of sigma-delta ADC. One can increase the sampling frequency relative to the bandwidth of interest, the order of the noise transfer function, or the resolution of the quantizer. All three of these approaches come with an attendant cost in power dissipation and circuit area. A study on improvement signal-to-noise ratio of sigma delta ADC is running with the method of increasing quantization bit number to improve resolution.[1]. In this case, it is difficult effective resolution of DAC within feedback loop, because of element mismatch problem.[2] There are added Dynamic Element Matching(DEM) circuit which is Digital correction technique for DAC to improve resolution and linearity. But DEM technique raises delay, complexity and more power dissipation.

In this paper proposed local feedback loop filter to improve stability within simgle-bit feedback multi-bit quantization single loop sigma delta ADC. The circuit is fabricated using 0.25um CMOS process. We did SNR and output spectrum measurement.

2. Design of Sigma Delta ADC

2.1. Structure of Sigma Delta ADC

There are three ways to increase the resolution of sigma-delta ADC. One can increase the sampling frequency relative to the bandwidth of interest, the order of the noise transfer function, or the resolution of the quantizer.

Increasing the sampling frequency can yield substantial increases in the resolution of the ADC depending on the order of the modulator. The obvious drawback is that doing this costs more power in the quantizer and feedback DAC as well as in the noise-shaping filter if it is a discrete time or switched-capacitor implementation.

Increasing the order of the modulator is a technique that achieve nearly 20 bits of resolution over audio bandwidths are available publicly. In this case of a high-order modulator has several other drawbacks. It will require a higher order digital filter downstream from the modulator. Moreover for a fixed sampling frequency, a small increase in the signal bandwidth results in substantial loss in SNR.

Increasing the quantization bits has the important benefit that each additional bit of resolution in the quantizer yields an additional one bit or 6 dB of SNR across the entire Nyquist bandwidth of the ADC.[2]

A less obvious drawback has to do with the implications for the feedback DAC. In a multibit sigma-delta modulator, the multibit quantizer accompany a multibit feedback DAC. The overall resolution of the modulator is limited to the effective resolution of the feedback DAC. In today's advanced CMOS processes, it is difficult to build a DAC with better than 10 bits of effective resolution because of the effects of random device mismatch.[3] Thus those who have attempted multibit sigma-delta ADC designs have relied upon calibration or some sort of Dynamic Element Matching(DEM) technique to increase the effective resolution of the feedback DAC. This way requires more digital circuitry and power consumption. So, our purpose of multibit sigma delta ADC design avoid these problems.

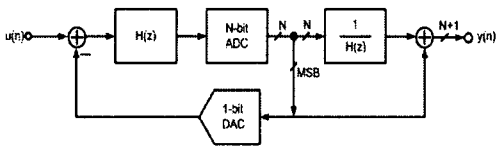

Figure 1 General Leslie-Singh Structure

Figure 1 shows general Leslie-Singh structure. This modulator uses only most significant bit(MSB) feedback at modulator input stage. It achieves noise due to multibit DAC element mismatch to be eliminated. The Leslie-Singh structure has advantage available operation at lower Over-Sampling Ratio(OSR). Because of MSB feedback, a multibit sigma delta ADC goes through reducing effective bit more than using multibit feedback DAC. [4]

In this paper proposed the loop filter for improving resolution. Because a single bit feedback reduces resolution of multibit sigma delta ADC. The three order loop filter is added local feedback. We achieved stability by eliminating lack of stability due to open path loop filter. Accordingly, we can improve resolution of conventional single bit feedback multi bit quantization ADC structure.

2.2. LOOP FILTER

Figure 2 shows block diagram of loop filter with local feedback. The loop filter perfomed Noise Transfer Function such as equation (1) to

be obtain desirable SNR and resolution.

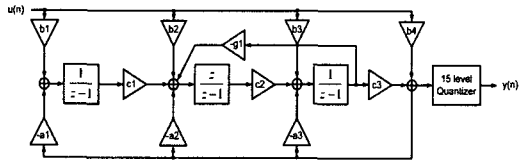

Figure 2 Block Diagram of Single-bit feedback Multi-bit ADC with local feedback

$$H(z)=\frac{(z-1)(z^2-1.977z+1)}{(z-0.185)(z^2-0.08252z+0.08614)} \quad (1)$$

We assumed that Signal Transfer Function is unity gain and decided circuit parameter of proposed loop filter block diagram.

Table 1 Circuit parameter of Loop Filter

parameter	value
a1	0.8587
a2	1.7753
a3	0.9841
b1	0.8587
b2	1.7753
b3	0.984
b4	1
g1	0.0231

To be obtain parameter of circuit and desirable characteristic of sigma delta ADC is achieved modeling by using MATLAT[5]

2.3 REALIZATION AND OPERATION

In this section describes the realization of proposed loop filter. Figure 3 shows stability improvement for higher resolution sigma delta ADC. We drew a positive part of loop filter for simplicity because of Overall sigma delta ADC fully differential mode operating. The analog summer and subtractor is consisted of switched capacitor that is made switch and capacitor. It requires high gain opamp for improving performance of loop filter. The opamp achieves high gain 54dB in loop filter. A sampling capacitor size must be larger than thermal noise in input signal. The capacitor size is calculated 0.5pF equal to thermal noise. For thermal noise to be eliminated, we use 3.5pF seven times larger than 0.5pF.

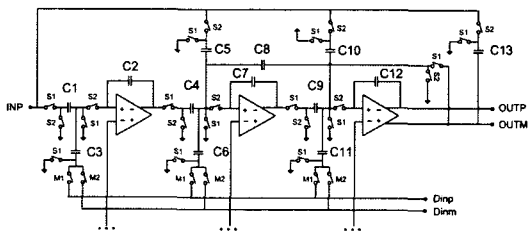

그림 3 Third Order Loop Filter(positive part) for realization

The first integrator yields output to be first order filtered. That is transfer from first integrator output to sampling switched capacitor C4. The sampling signal of first integrator output is roll of the second integrator input in order to sum. Similarly, the third integrator has same operation.

The conventional loop filter is performed open loop operation it cause lack of stability. For this reason, the local feedback has been added to proposed loop filter. It is improved stability of loop filter.

The proposed sigma delta ADC achieves SNR to be improved and noise drop within in-band by improving stability.

4. Result

Figure 4 and 5 show characteristic of the proposed sigma delta ADC that is SNR and output spectrum, respectively. SNR is improved 96.9dB more than conventional case 74.5dB. Consequently, resolution of proposed sigma delta ADC is 15.8bit that is rising value better than 12.1bit. Figure 6 shows noise shaping performance noise is reduced within in-band and increased out-of-band

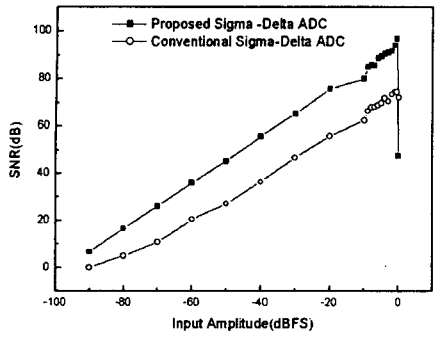

그림 4 Signal to Noise Ratio

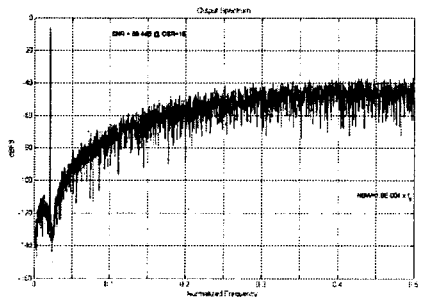

그림 6 Output spectrum for sigma delta ADC with proposed loop filter

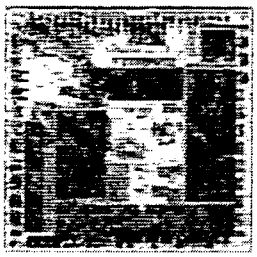

그림 7 Die micrograph

표 2 Performance of Sigma-Delta ADC

Parameter	Value
Signal Bandwidth	615㎑
Sampling Frequency	19.6㎒
Over-sampling Ratio	16
Peak SNR	96.9dB
Effective Resolution	15.8bit
Power consumption	35mW

The proposed sigma delta ADC is fabricated 0.25um CMOS process. Threshold voltage of NMOS and PMOS is 0.5V and -0.55V, respectively. That performance is summarized in table 2.

4. CONCLUSION

In this paper is described design of using single bit feedback for sigma delta ADC to improve linearity within feedback loop. Furthermore add to local feedback in loop filter in order to solve the problem of lower resolution. As a result of SNR achieves 96.9dB at low OSR(16). The designed ADC performed noise shaping, reducing noise floor within in-band.

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