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$Pt/Bi_{3.25}La_{0.75}Ti_3O_{12}/CeO_2/Si$ 구조를 이용한 MFISFET의 구조 및 전기적 특성

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Structural and electrical properties of MFISFET using a $Pt/Bi_{3.25}La_{0.75}Ti_3O_{12}/CeO_2/Si$ structure

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Abstract - The metal-ferroelectric-insulator-semiconductor (MFIS) capacitors were fabricated using a metalorganic decomposition (MOD)method. The CeO_2 thin films were deposited as a buffer layer on Si substrate and $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT)thin films were used as a ferroelectric layer. The electrical and structural properties of the MFIS structure were investigated by varying the CeO_2 layer thickness. The width of the memory window in thecapacitance-voltage (C-V)curves for the MFIS structure decreased with increasing thickness of the CeO2 layer. Auger electron spectroscopy (AES) and transmission electron microscopy (TEM) show no interdiffusion by using the CeO_2 film as buffer layer between the BLT film and Si substrate. The experimental results show that the BLT-based MFIS structure is suitable for non-volatile memory field-effect-transistors (FETs) with large memory window.

1. 서 론

Memory device using ferroelectric may be categorized into ferroelectric random access memory (FRAM), dynamic random access memory (DRAM), metal-ferroelectric-semiconductorfield-effect-transistors (MFS-FETs), where a ferroelectric film is used as a gate insulator [1]. Ferroelectric thin films such as Bi-based layered perovskite ($SrBi_2Ta_2O_9$ (SBT), $Bi_4Ti_3O_{12}$ (BTO), $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT), etc.) and $Pb(Zr,Ti)O_3$ (PZT) thin films have been extensively investigated for non-volatile FRAM devices. The PZT films have some serious problem such as the imprint, retention and fatigue which ferroelectric properties are degraded by repetitive polarization switching. The SBT films have fatigue-free characteristic. However it has a high processing temperature of above 800 C and a low remanent polarization [2, 3]. Among them, BLT thin films have advantages such as highly fatigue resistant characteristic, low processing temperature, and large remanent polarization.In this respect, BLT films are considered for the MFS-FETs. Because non-volatile memories using MFS-FETs make non-destructive operation possible, rewriting for destroyed information is not needed [4, 8]. However, the MFS-FETs that ferroelectric film deposited directly on Si substrate without inserting an electrode have been some problems such as the formation of an amorphous SiO2 layer with a low dielectric constant at the ferroelectric film/Si interface and interdiffusion between the ferroelectric film and Si substrate [5, 9]. To suppress them, a metal-ferroelectric - insulator - semiconductor (MFIS) structure has been demonstrated. The most important thing in developing a MFIS structure is to find a good insulator that acts as a buffer between the Si substrate and the ferroelectric material. The insulating buffer layer such as CeO_2, ZrO_2, and Y_2O_3 have relative high dielectric constants of 10 to 20 ranges, low leakage current, good interface characteristics, and compatibility [6, 10]. Among them, the CeO_2 is used as an insulating buffer layer because it is chemically stable at very high temperature and the lattice mismatch with Si is quite small [7].

In this paper, the CeO_2 and BLT film were fabricated using a metalorganic deposition (MOD) method, the CeO_2 was deposited as a buffer layer on Si substrate, and BLT thin films were used as a ferroelectric layer. In order toshow that the BLT-based MFIS structure is suitable for non-volatile memory FETs with large memory window, the electrical and structural properties of the MFIS structure were investigated by varying the CeO_2 layer thickness.

2. 실 험

P-Si substrates to deposit the CeO_2 film were cleaned by RCA in order to eliminate the native silicon oxide. First, CeO_2 thin films were prepared on the Si substrates using the MOD method. Precursor of cerium acetylacetonate hydrate [Ce(CH3COCHCHCH3)3x-H2O] and solvent of methanol [CH3OH] were used. BLT thin films were also prepared using the MOD method. Precursors of

bismuth acetate [Bi(CH3CO2)3], lanthanum-acetate hydrate [(CH3CO2)LaxH2O], and titanium iso-propoxide {Ti[OCH(CH3)2]4} and solvents of an acetic acid [CH3CO2H] and 2-methoxyethanol [CH3OCH2CH2OH] were used.

The CeO_2 films were deposited using spin coating o nto Si substrates at room temperature, dried at 400 o C for 10 min to remove organic material. The BLT fil ms were also deposited using spin-coated onto Si sub strates and the CeO_2/Si substrates at room temperatur e, dried at 400 oC for 10 min to remove organic mate rial, respectively. The CeO_2 films were adjusted in a r ange from 10 to 40 nm by a repetition of these proce sses. The final thickness of BLT film was 200 nm. In order to crystallize the films, the pre-baked CeO_2 and BLT were annealed at 700 C and 650C for 1 h in oxy gen ambient, respectively. Pt as the top electrode mat erial of 300 m diameter was sputtered through a shad ow mask on the BLT films.

X-ray diffraction (XRD)was used to determine the p hase of the BLT thin films and the CeO_2 layer. The morphology of the films and the interface structures o f the BLT and the CeO_2 layers were investigated by f ield emission scanning electron microscopy (FE-SEM) and transmission electron microscopy (TEM), respecti vely. The depth profile of the BLT/CeO_2/Si structure was analyzed by auger electron spectroscopy (AES). The polarization-electric field (P-E) hysteresis of the BLT film was measured using RT66A. The high freq uency C-V characteristics of the CeO_2/Si and the BL T/CeO_2/Si were measured using a HP 4192 impedance analyzer with 1 MHz and a sweep speed of 0.2 V/s.

3. 본 론

Figure 1 represents the XRD patterns of (a) CeO_2 film deposited on Si substrates, (b) BLT films deposited on CeO_2/Si and (c) BLT films deposited on Si substrates. As shown in Fig. 1(a), the CeO_2 film showed the (311) diffraction peak, which was conformed to a cubic fluoride consistent with the joint committee of powder diffraction standard (JCPDS) cards. The BLT film deposited on the Si substrates shows the typical XRD patterns of BTO layered perovskite polycrystalline structure. Secondary phases or preferred orientations were not observed and the BLT film deposited on the CeO_2/Si has the same polycrystalline phase without the change. In Fig. 1(b), the (311) peak of CeO_2 film is considered that be heaped up the (173)/(371) peak of BLT film which moved due to the generated stress for annealing.

Electrical properties of BLT/CeO_2/Si structures were characterized by the high frequency C-V measurements. Figure 3 shows C-V characteristic of a Pt/BLT/CeO_2/Si structure, measured for different thicknesses of the CeO_2 film. The insert displays the memory window of Pt/BLT/CeO_2/Si structure, measured at the corresponding thicknesses of the CeO_2 film. The thickness of CeO_2 film varies from 20 nm to 40 nm and the thickness of BLT film is fixed at 200 nm. The applied voltage was swept at the speed of 0.2 V/s from +5 V to 5 V and from 5 V to +5 V. The C-V curve shows a hysteresis loop witha counterclockwise trace due to the ferroelectric polarization reversal of the BLT film and varies from the accumulation to the inversion state. The C-V curve shows the parallel shift from an ideal state along the positive voltage-axis. The equivalent sheet surfacecharge is induced by the dipole moment of the ferroelectric. The BLT film is considered to have caused the voltage shift in those structures. The width of the memory window in the C-V curves for the MFIS structure decreaseswith increasing thickness of the CeO_2 layer see insert Fig.2. The memory window of Pt/BLT/CeO_2/Si structure has the large value for the CeO_2 film of 20 nm thickness. The memory window is related to the mobile ions, coercive field and saturation level of the polarization, and is affected by the crystal orientation, film thickness and grain size of the ferroelectric thin film.

Figure 4 shows the 1 MHz C-V characteristics of BLT/CeO_2/Si and BLT/Si structure. The thickness of CeO_2 and BLT film is 20 and 200 nm, respectively. The applied voltage was swept at the speed of 0.2 V/s from +5 V to 5 V and from 5 V to +5 V. As shown in Fig. 4, the memory window of BLT/CeO_2/Si and BLT/Si was about 2.82 V and 2.3 V, respectively. The BLT/CeO_2/Si structure using CeO_2 film as insulating buffer layer can obtain good characteristics for the memory window and capacitance than BLT/Si structure.

Figure 3 show the C-V characteristic with different voltage sweep for the each applied voltage of Pt/BLT(200 nm)/CeO_2(20 nm)/Si structure. The insert shown the memory window for the each applied voltage of Pt/BLT(200 nm)/CeO_2(20 nm)/Si structure. The 1 MHz C-V characteristic was measured corresponding to applied voltage from 3 V to 7 V. The memory window increases with the applied voltage under the same thickness of the CeO_2 film, see insert in Fig. 5. It is considered that the polarization and the coercive voltage of ferroelectric is being increased the increasing applied voltage, and thus the memory window is also increase.

In order to verify the effect of the CeO_2 film as a buffer layer, the depth profile of BLT(200

nm)/CeO_2(40 nm)/Si structure has been measured by AES. AES operation conditions are that Ar sputtering ion, the speed of 303Å/min for SiO2, the electron accelerating voltage of 10 kV, and the base pressure of 5×10^{10} torr. Figure 4 shows the AES depth profile of BLT/CeO_2/Si structure. Generally, there are some problems such as the formation of an amorphous SiO2layer with a low dielectric constant at the ferroelectricfilm/Si interface and interdiffusion between the ferroelectric film and Si substrate. As shown in Fig. 4, the concentration of the component (Bi, La, Ti)is nearly uniform through the whole film of the BLT thin films. There is no interdiffusion between the BLT film and Si by using the CeO_2 film as buffer layer. At the interface between the CeO_2 thin film and Si substrate, the SiO2 layer of the about 10 nmis formed by the reaction of O and Si as shown in Fig. 4. It seems to form during the BLT annealing in oxygen. Also, the interface between the CeO_2 thin film and SiO2 has the cerium silicate consisting of cerium, silicon, and oxygen. Therefore, if gate bias will be applied to the MFIS structure, the gate bias should be divided into the BLT, CeO_2 cerium silicate, SiO2, and Si substrate, respectively.

Figure 5 shows a cross-sectional TEM image of the interface structure of BLT/CeO_2/Si sample. The CeO_2 film of 6 nm is uniformly deposited on Si substrate. Also, it is evidentthat interdiffusion at the ferroelectric film/Si interface does not occur and an amorphous SiO2 layer of the 5 nm and the cerium silicate of the 2 nm are present. It is considered that the CeO_2 layer prevents diffusion of Si atoms into the BLT film and charge injection and ion drift effects are negligibly small. For the formation of SiO2 layer, the source of the oxygen species should be the annealing ambient gas and CeO_2 film itself. Thus, the thickness of the SiO2 layer in the Figure 4 is more larger than the SiO2 layer in the Figure 5 because the thickness of CeO_2 film in the Figure 4 and 6 is 40 nm and 6 nm, respectively. As a result, although the SiO2 exists between the CeO_2 and the Si substrate, the CeO_2 film is suitable as an insulating buffer layer for MFIS structure.

4. 결 론

MFIS structure of Pt/BLT/CeO_2/Si using the BLT film as ferroelectric layer and the CeO_2 film as insulating buffer layer were fabricated by MOD and spin-coated method. The CeO_2 film has only the (311) diffraction peak and BLT films show the typical XRD patterns of BTO layered perovskite polycrystalline structure. The memory window of BLT/CeO_2/Si and BLT/Si was about 2.82V and 2.3 V, respectively. The memory window increases as applied voltage under the same thickness of the CeO_2 film. AES and TEM show no interdiffusion by using the CeO_2 film as buffer layer between the BLT film and Si substrate. The experimental results can be concluded that the BLT-based MFIS structure is suitable for non-volatile memory FETs with large memory window.

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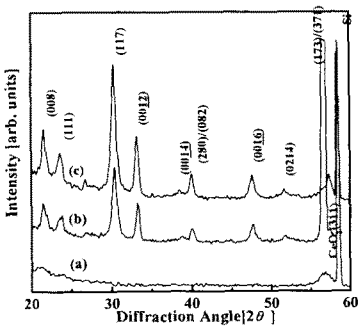

Fig.1.XRDpatternsof(a)CeO_2/Si,(b)BLT/CeO_2/Si,(c) BLT/Si.

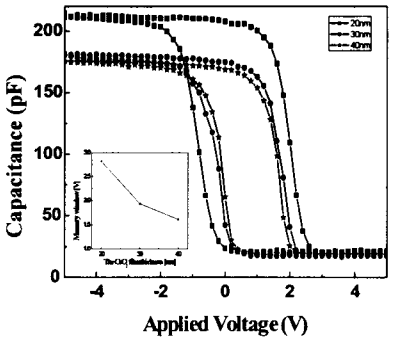

Fig. 2. Capacitance-voltage characteristic of Pt/BLT/CeO_2/Si structure measured with the different thickness of CeO_2 film (Insert for memory window of Pt/BLT/CeO_2/Si structure measured with the different thickness of CeO_2 film).

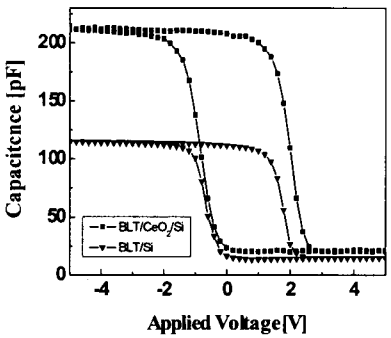

Fig.3. Capacitance-voltage characteristic of Pt/BLT (200nm)/Si and Pt/BLT/CeO_2(20nm)/Si structure.

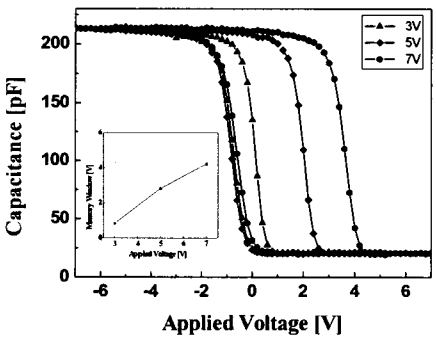

Fig.4. Capacitance-voltage characteristic of Pt/BLT/CeO_2/Si structures measured with different voltage sweeps (Insert for memory window of Pt/BLT/CeO_2/Si structures measured with different voltage sweeps).

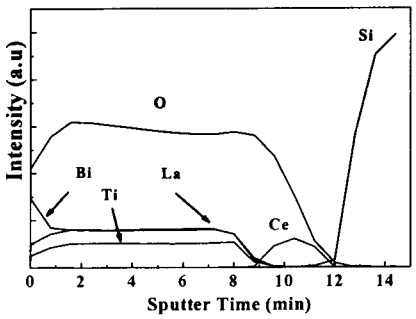

Fig.5. AES depth profile of BLT/CeO_2(40nm)/Si structure.

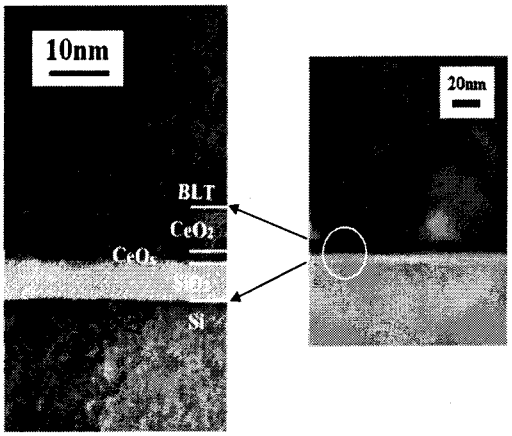

Fig.6. Cross-section TEM image of BLT/CeO_2 (20nm)/Si.