Signal Integrity Issues for Reliable Electronic System Designs

Prof. Yungseon Eo

Giga-Electronic System Laboratory
Dept. of Electrical and Computer Engineering
Hanyang University, Ansan. Korea

Pho. +82. 31. 400. 5295
Fax. +82. 31. 406. 2974
E-mail eo@giga.hanyang.ac.kr

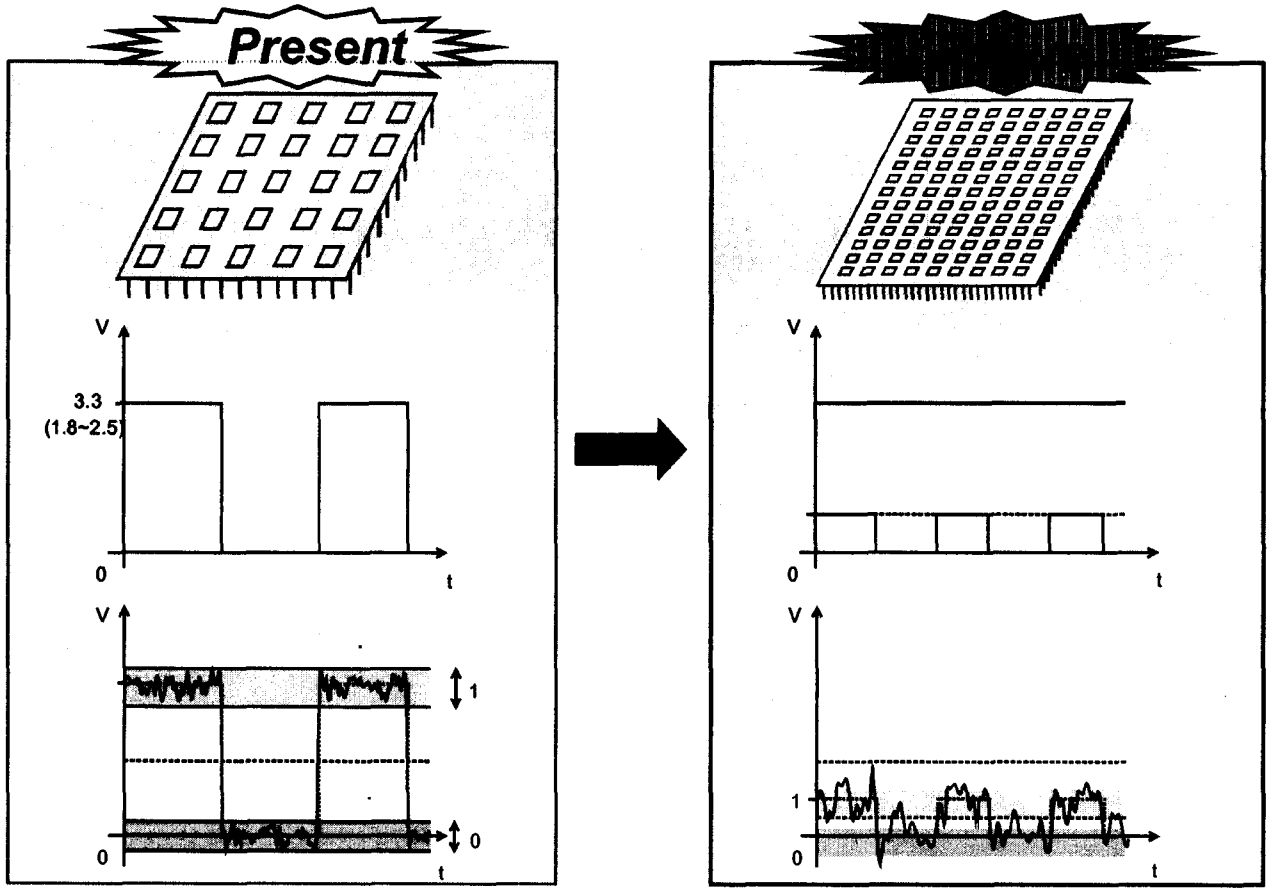
Outline

- General Introduction
- Signal Integrity Issues for Electronic System Designs
- Estimation-Based System Design
  - Related Issues
  - Summary and Conclusion

- ***It was "Reliability Analysis"***

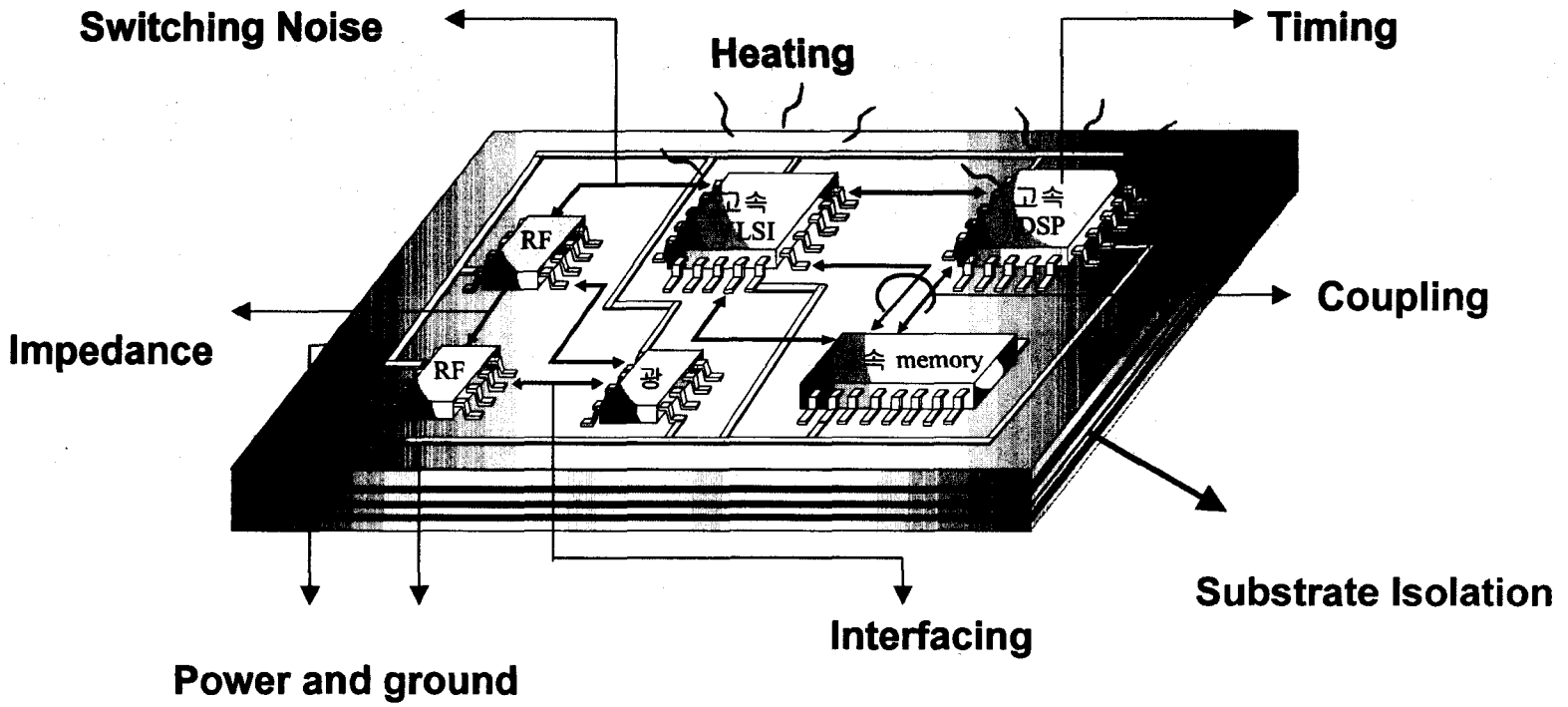
  But It is "Reliable Design" !!!

Future Disaster: Technical Challenges



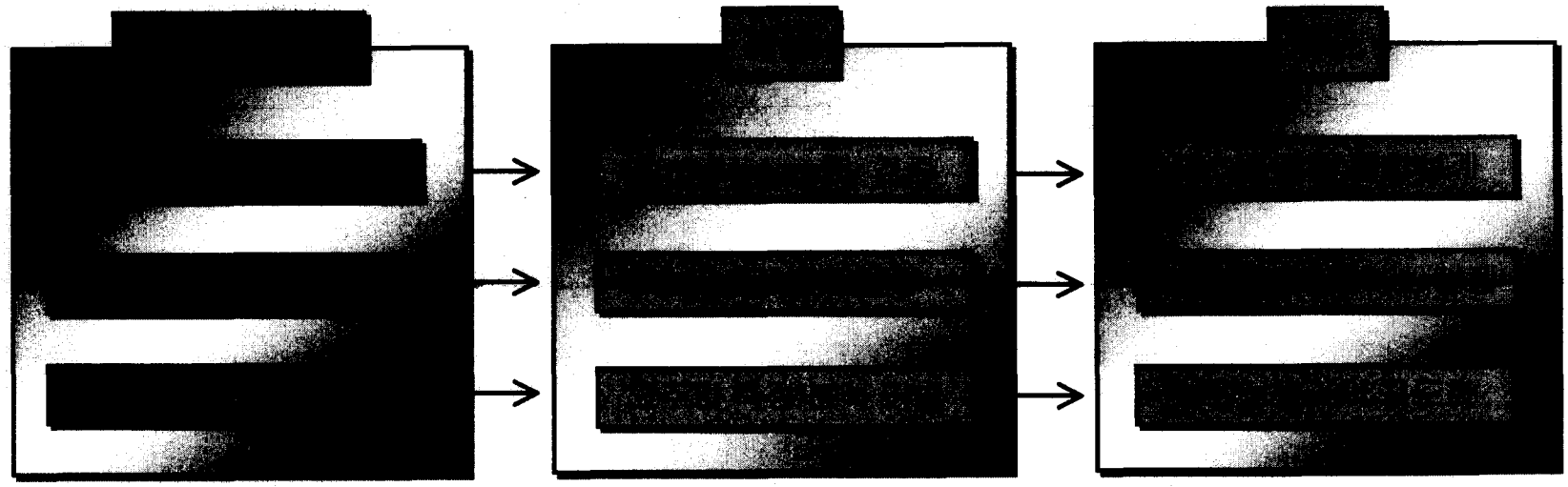
How is it going to be ?

Why ?



- ***Key Issue is the Signal Integrity Verification of the System !!***

Everybody Knows it, But ...??



Goal: System Level Integration Tech. Development !!

Where Are You ?

There is One Group of Engineers who believe

- *CAD Tools are Everything !!*
- *Theory is One Thing, Design is Another !!*

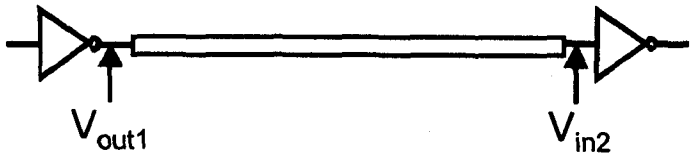
There is Another Group of Engineers who believe

- *Engineers are More Important than CAD Tools !!*
- *Design is the Simplified Version of a Theory !!*

Detailed Problems

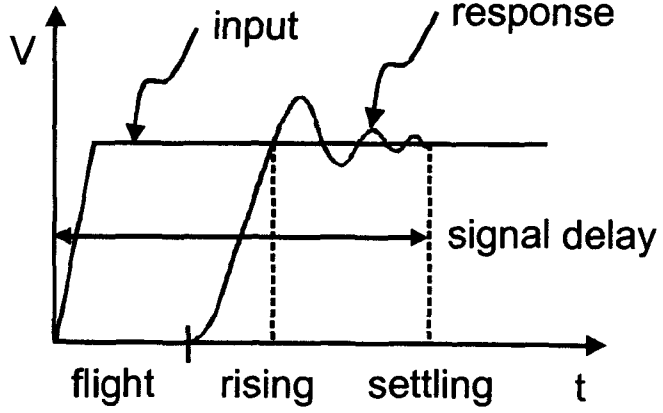
1. Timing Problem: Digital Signal Delay

- Signal Delay



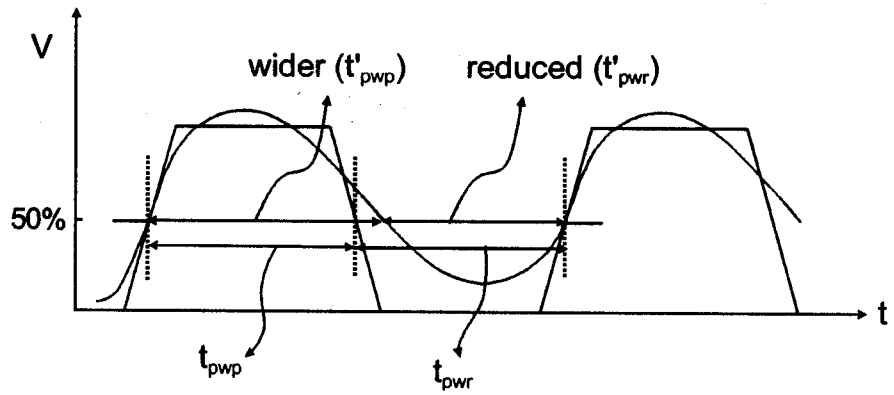
➡ for ideal system $V_{out1}=V_{in2}$

- Schematic Presentation of Delay

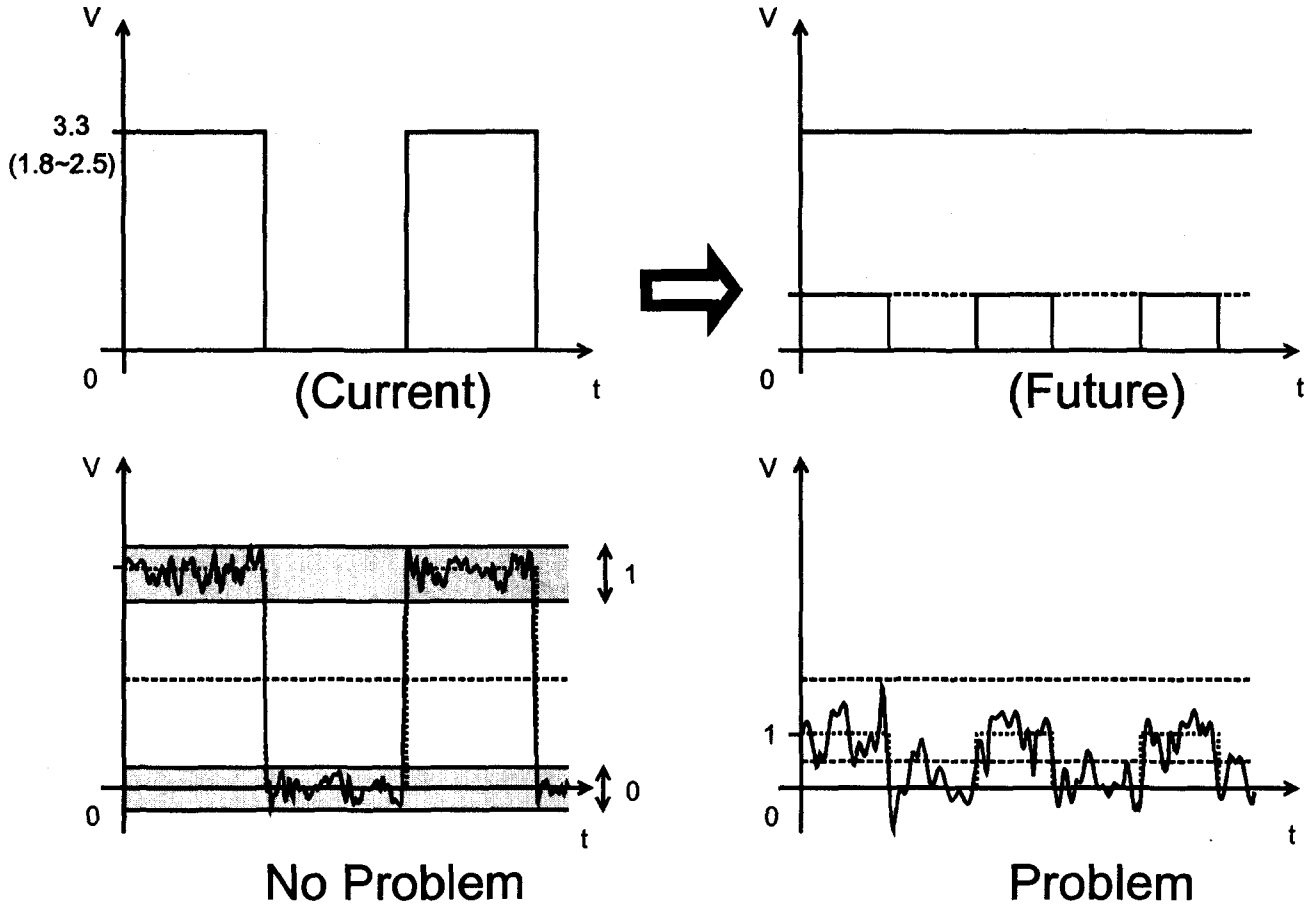


2. Dispersion

- Pulse Spreading

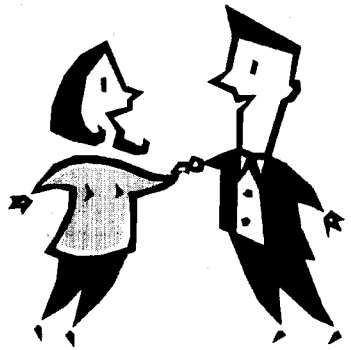


3. Little Noise Margin



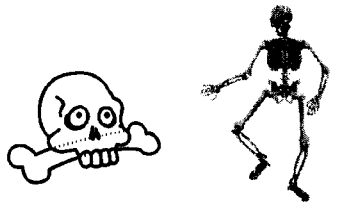
4. Electromagnetic Coupling: Crosstalk

High Potential Line (Ansan)



High Potential Line (Suwon)

(Seminar Room)



(Lobby)

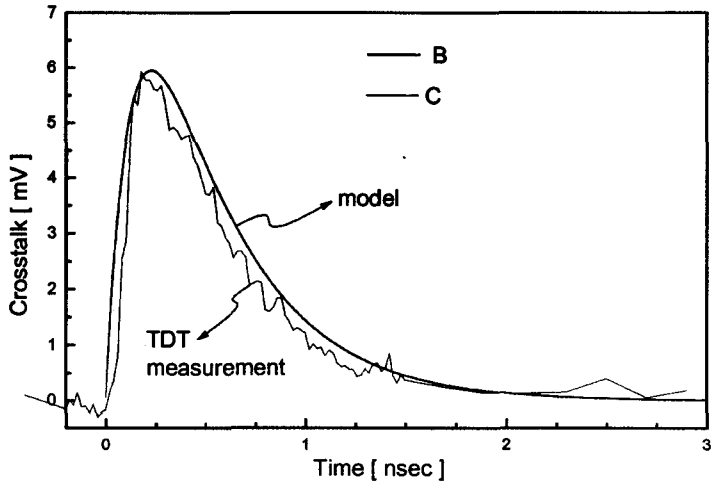
Safe **Die**

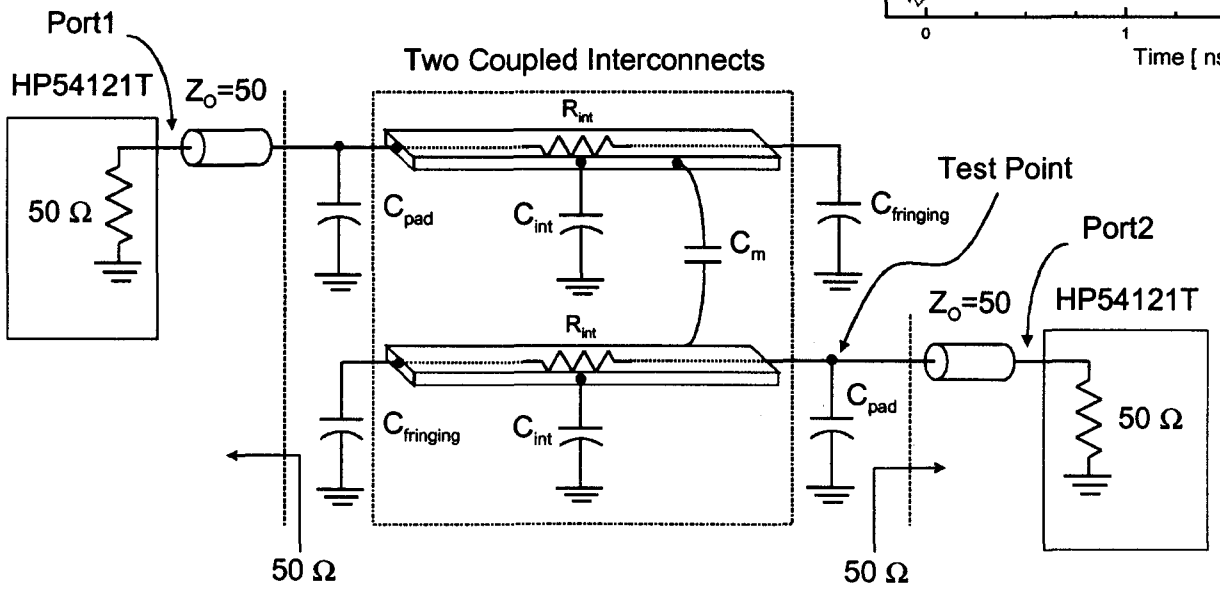
Why?

Crosstalk/Signal-Coupling

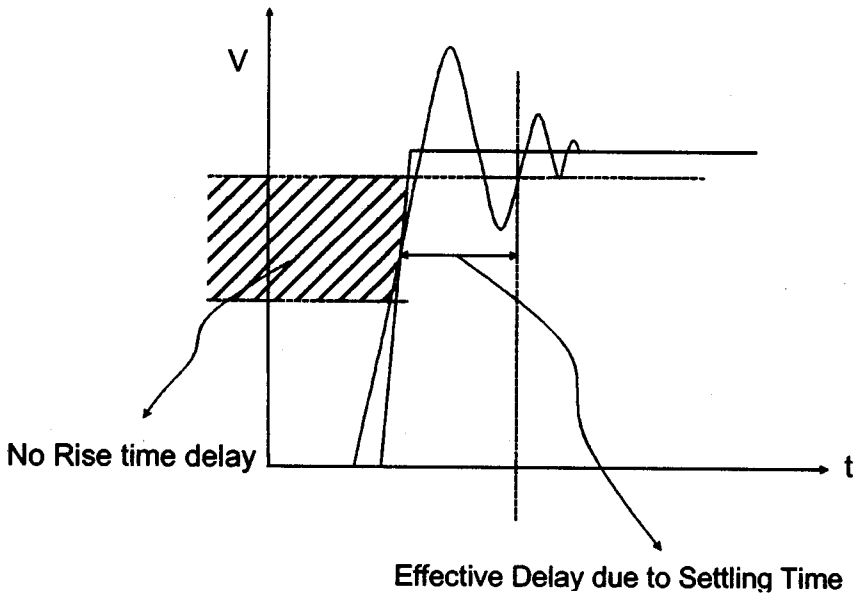
■ Why Crosstalk ?

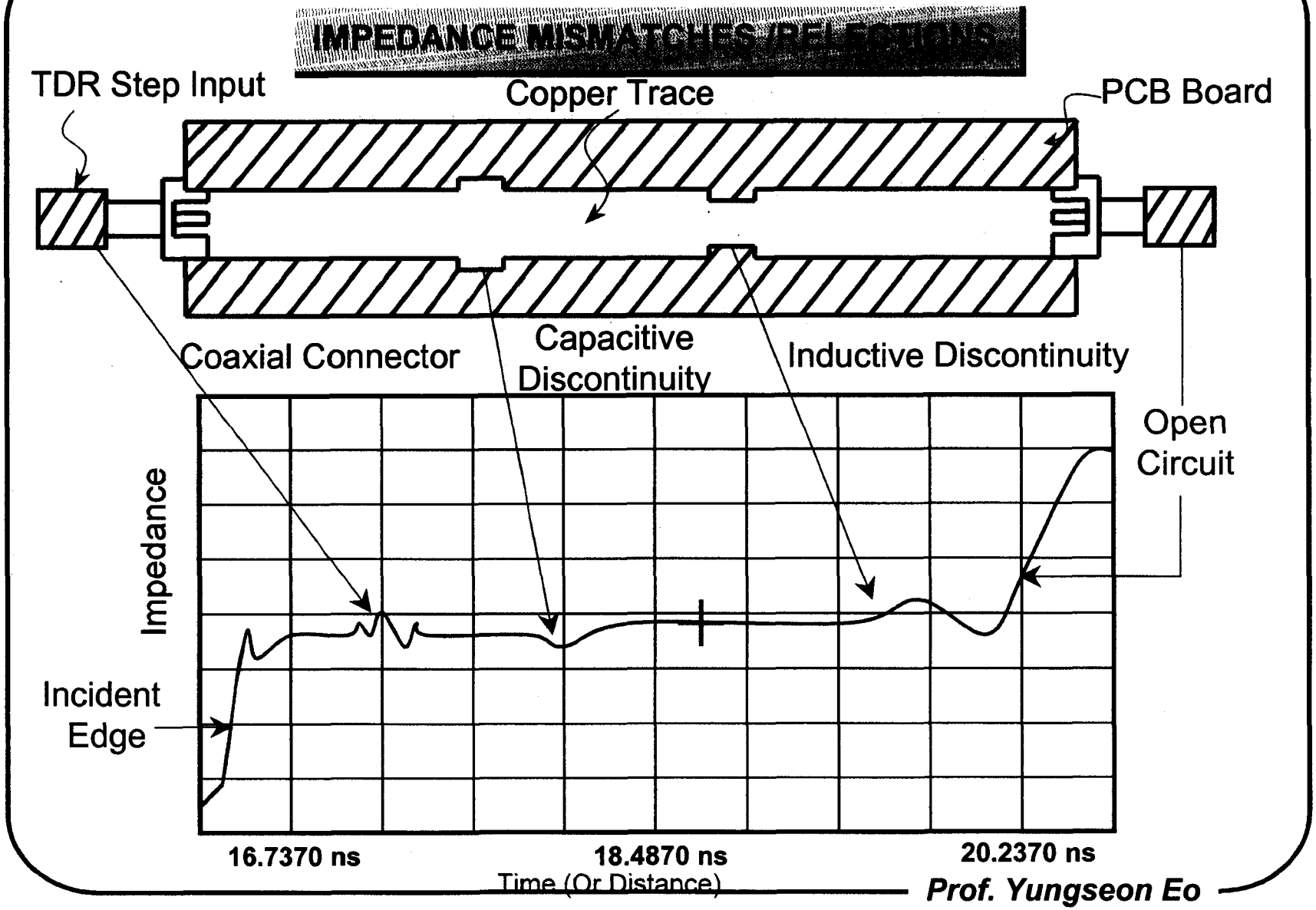
- ➢ Aspect Ratio increase
- ➢ Red. Spacing between the lines
- ➢ Inductive Coupling



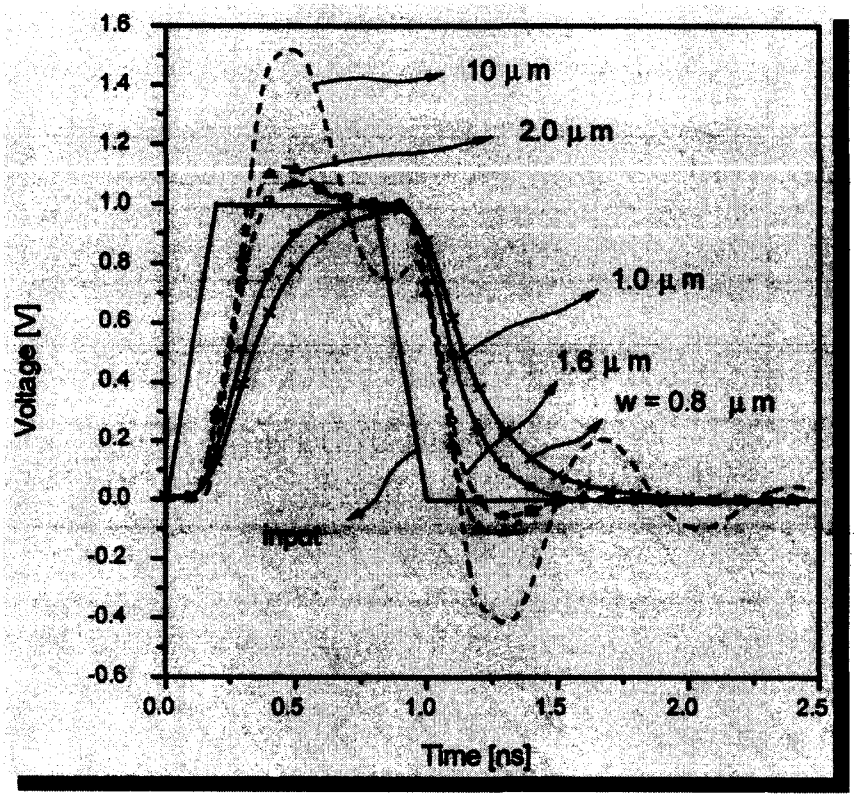


5. Reflection : Cause significant settling time



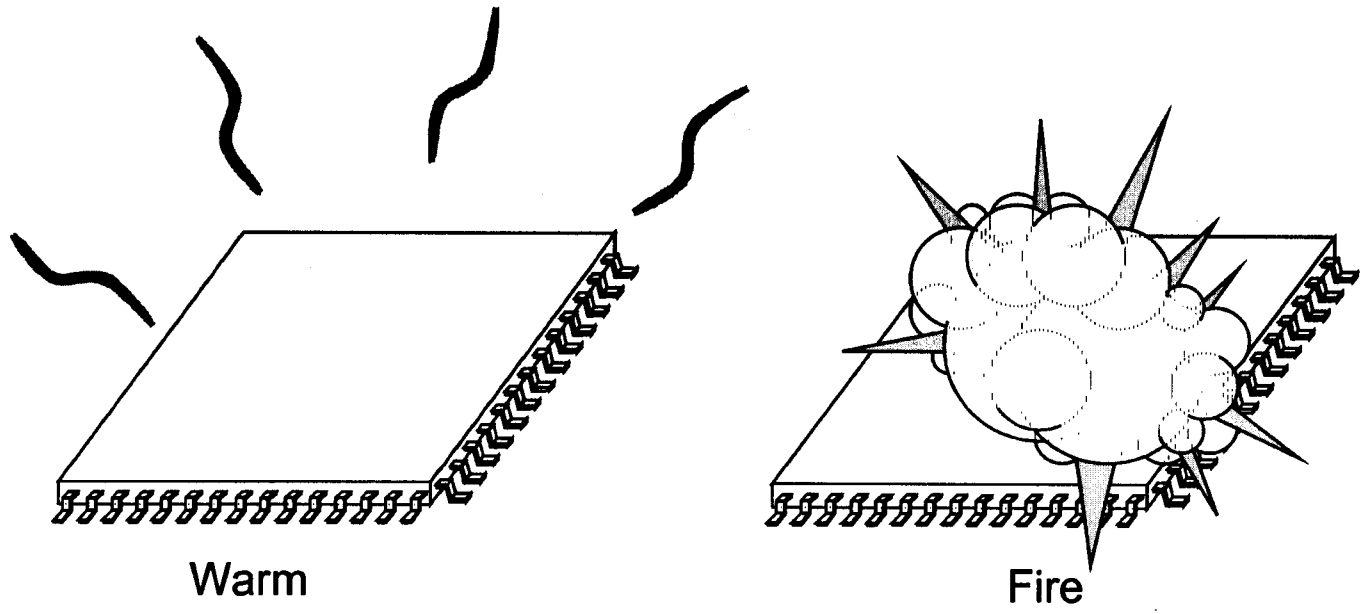

IMPEDANCE MISMATCHES/REFLECTIONS
TDR Step Input
Copper Trace
PCB Board
Coaxial Connector
Capacitive Discontinuity
Inductive Discontinuity
Open Circuit
Impedance
Incident Edge
16.7370 ns
18.4870 ns
20.2370 ns
Time (Or Distance)

- continued -



Responses for a pulse of the t_r=0.2nsec with different line widths

6. Thermal Problem due to High Power

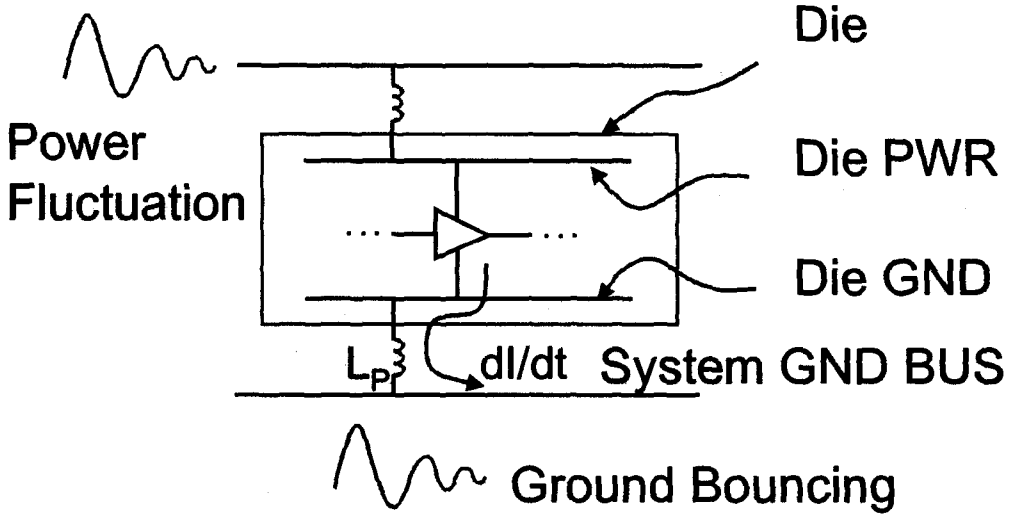


Semiconductor is a Function of Temperature.

At high temperature, semiconductor is meaningless

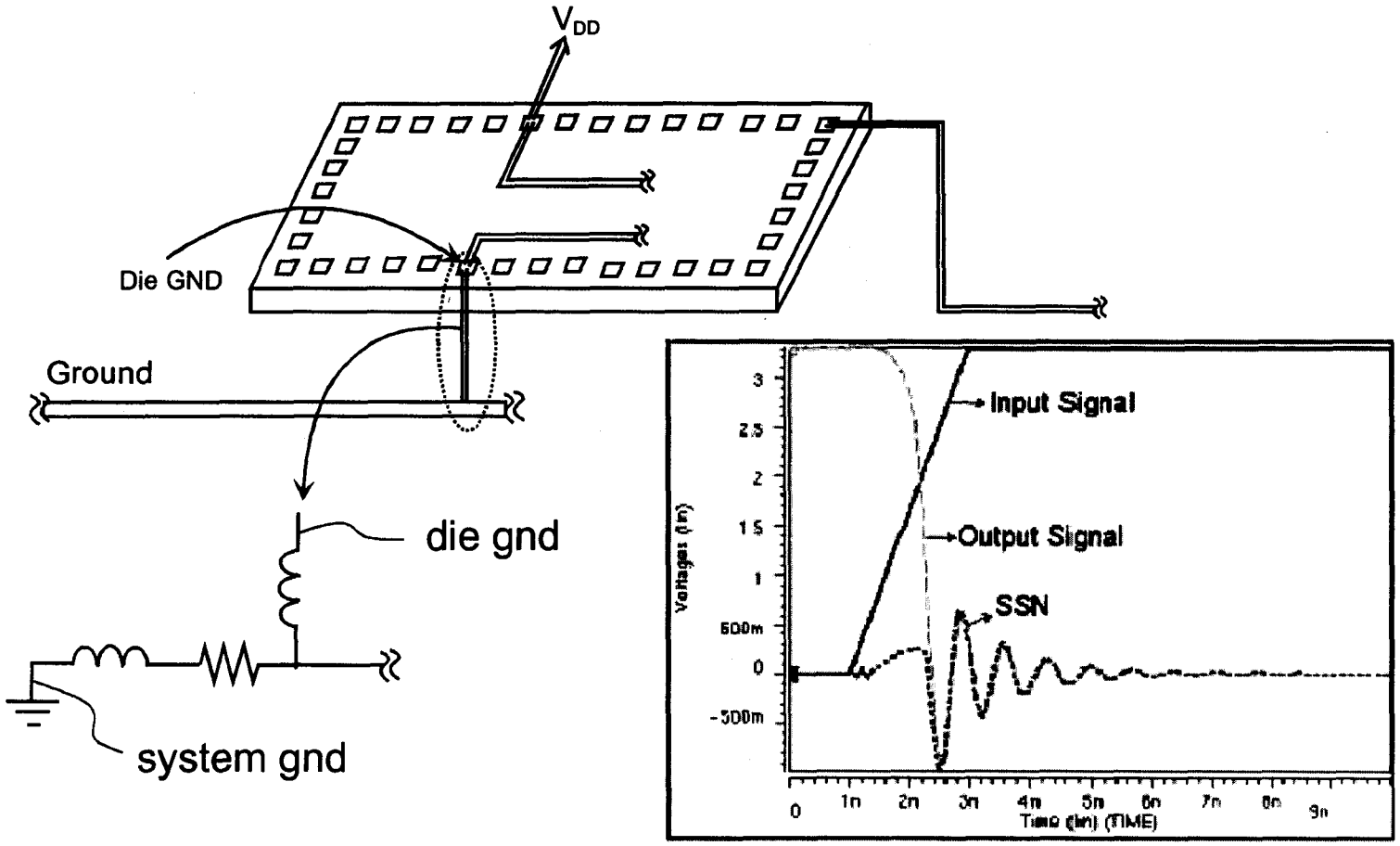
7. Simultaneous Switching Noise (Delta-I Noise)

⇒ Relative Ground and Power Definition Problem

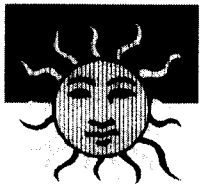


- Reference Potential Change
- Cause Glitch and Logic Failure
- Integrate Every Individual Noises

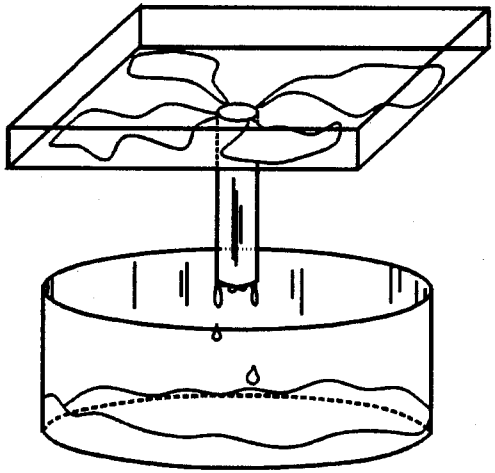
Simulation Example

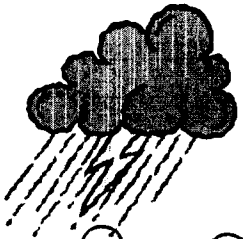


Another Point of View

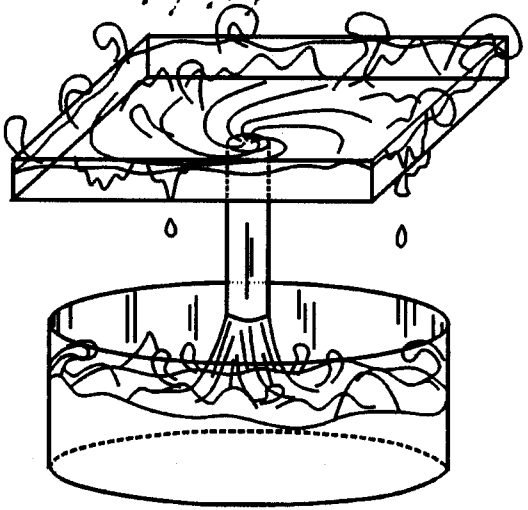


Sunny Day





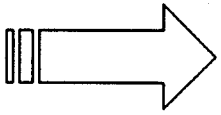
Rainy Day



Solution?

- Short
- Many Conduits

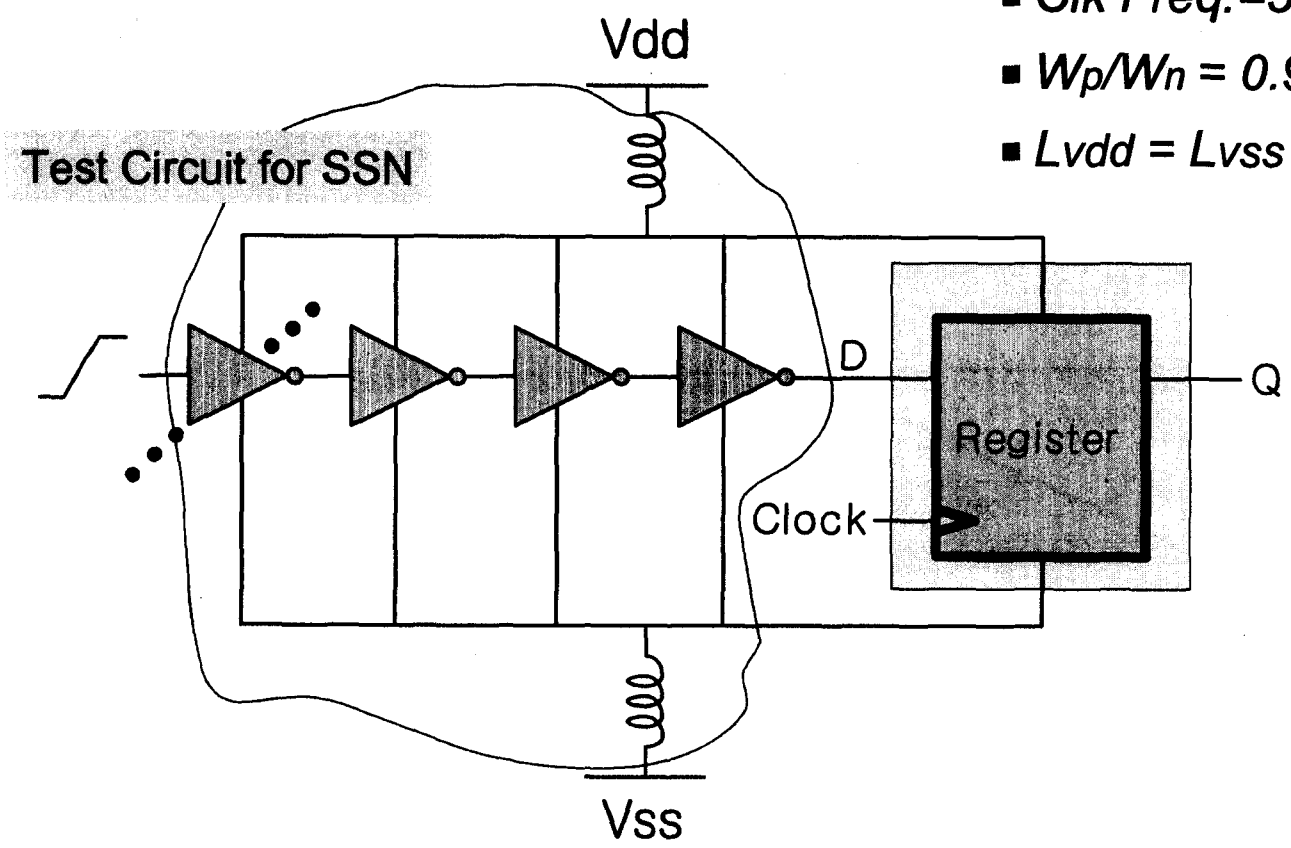
뷨 low water flowing



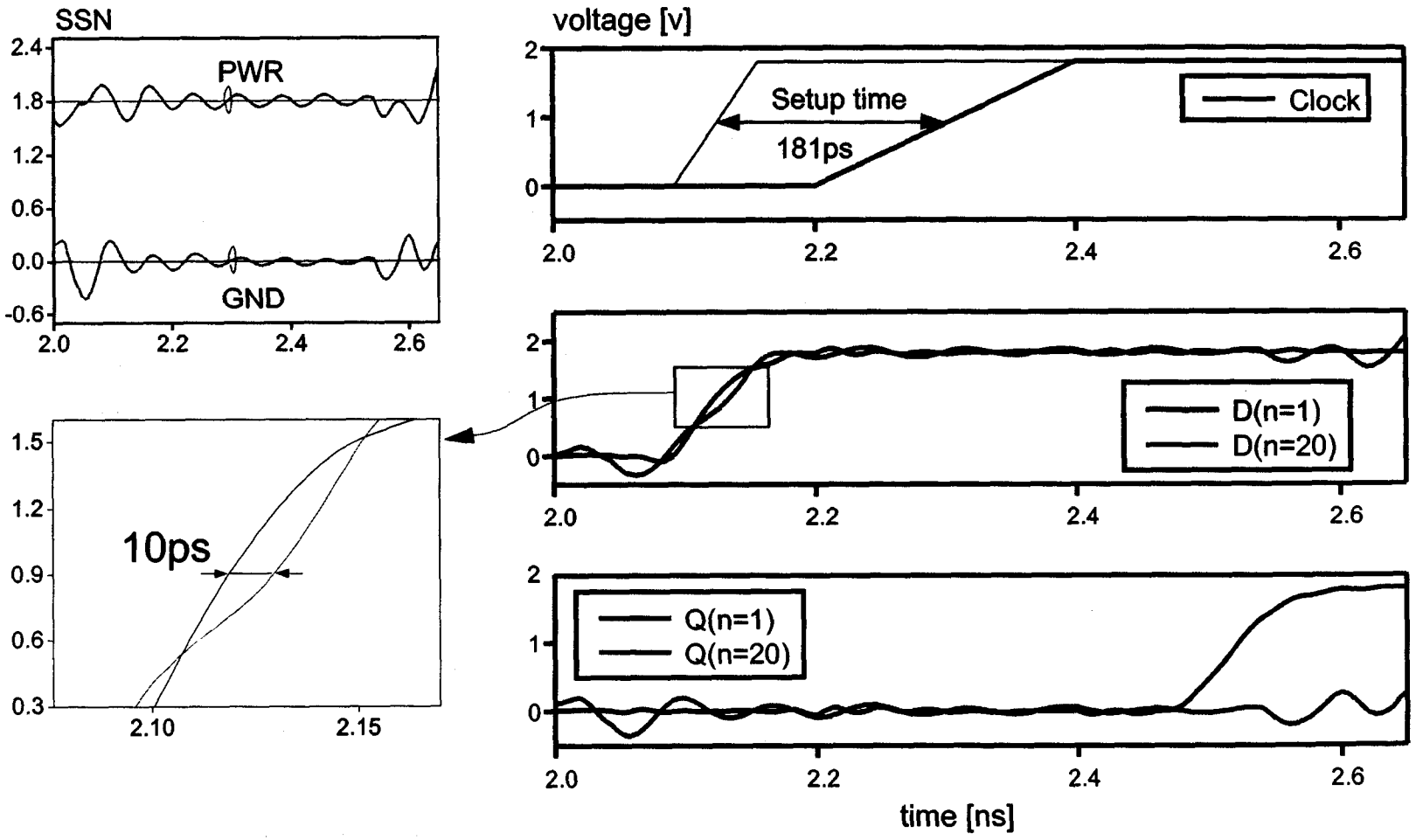
DIP --> BGA --> CSP
Many I/O
(X)

Example of a Circuit Failure due to SSN

- *TSMC 0.18μm/1.8V*
- *Clk Freq.=500MHz*
- *Wp/Wn = 0.9/0.36μm*
- *Lvdd = Lvss = 5nH*



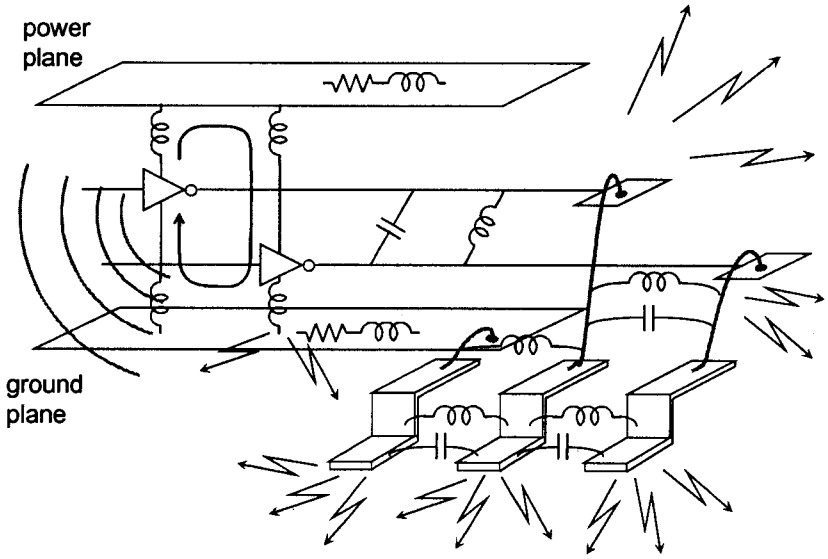
Simulation Result



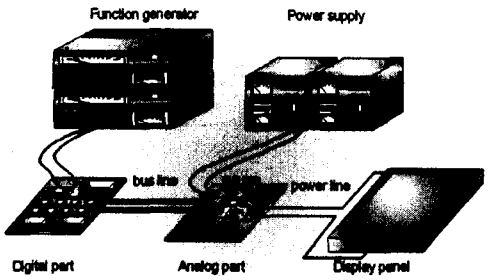
8. EMI/EMC of an Electronic System

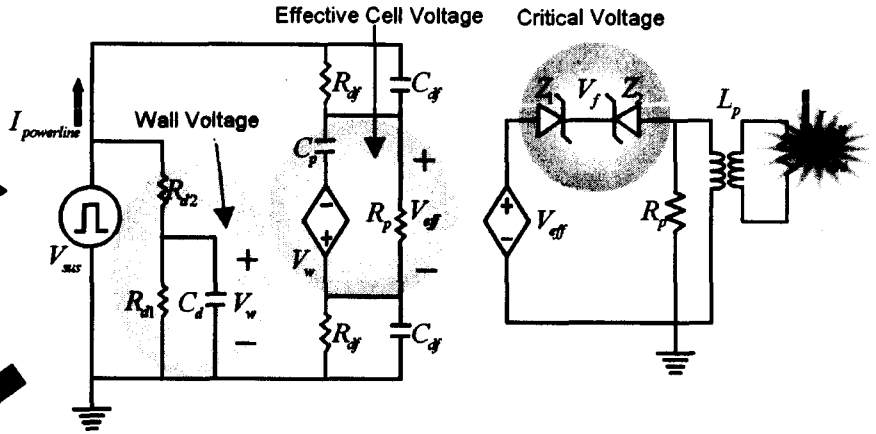
- **Why ?**
  - Complicated System-Level Charge Dynamics (*di/dt*)
  - High-Speed and High-Density Digital Circuits

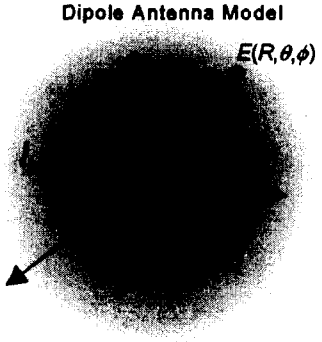
- **Where ?**
  - Clock Distribution Circuits
  - PCB Lines
  - IC Package
  - PWR&GND Distribution



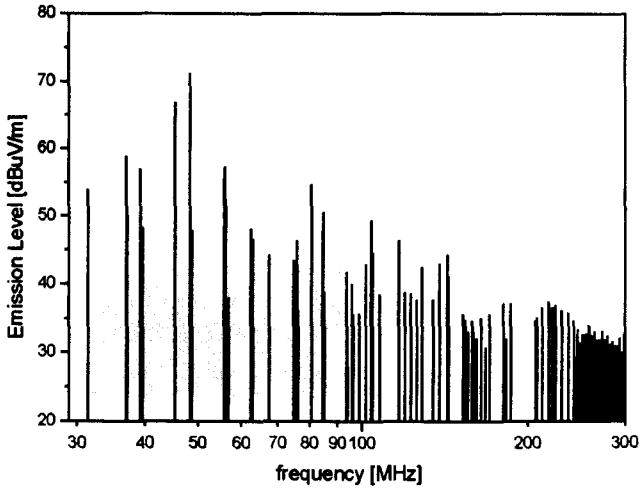
Example of an EMI-Problem



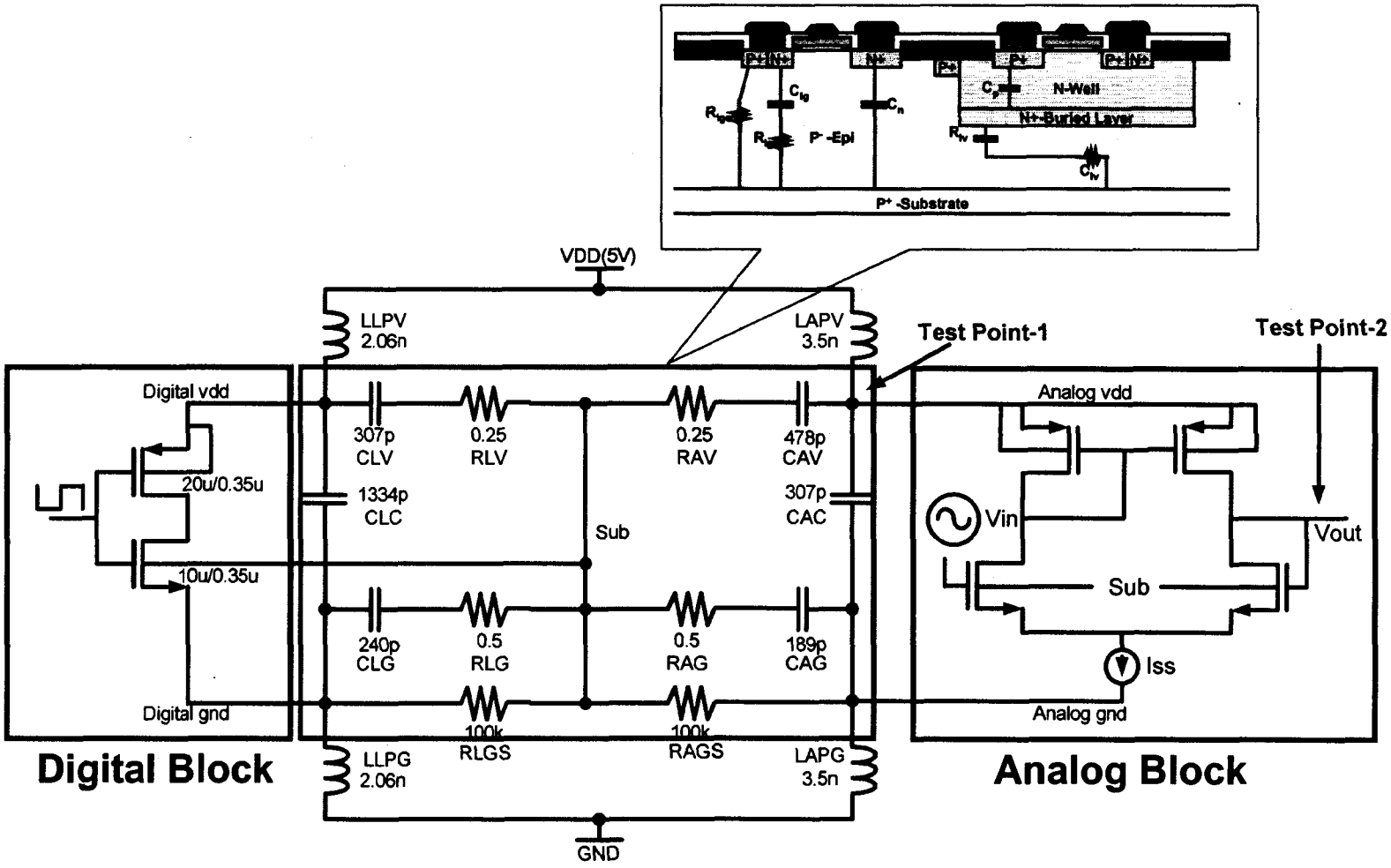




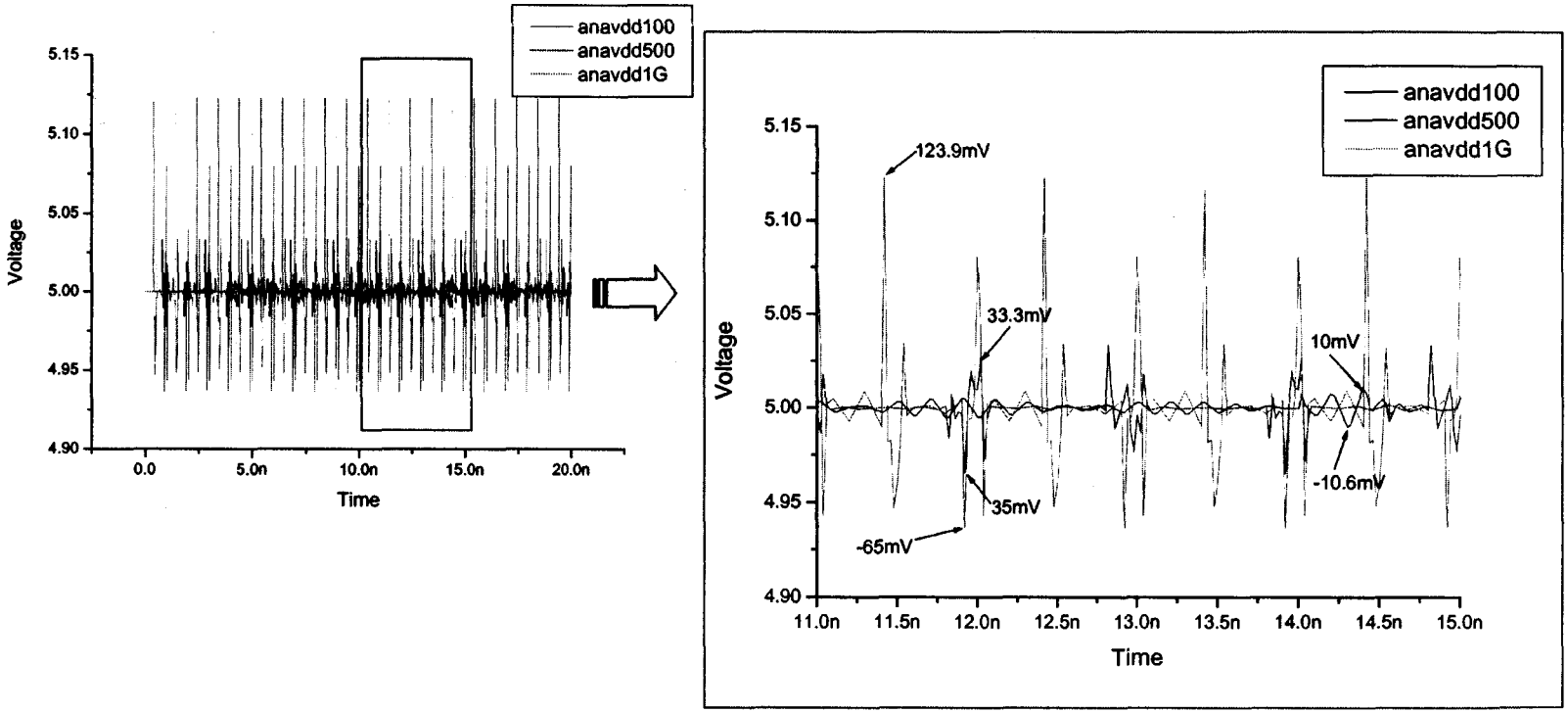
EMI Radiation



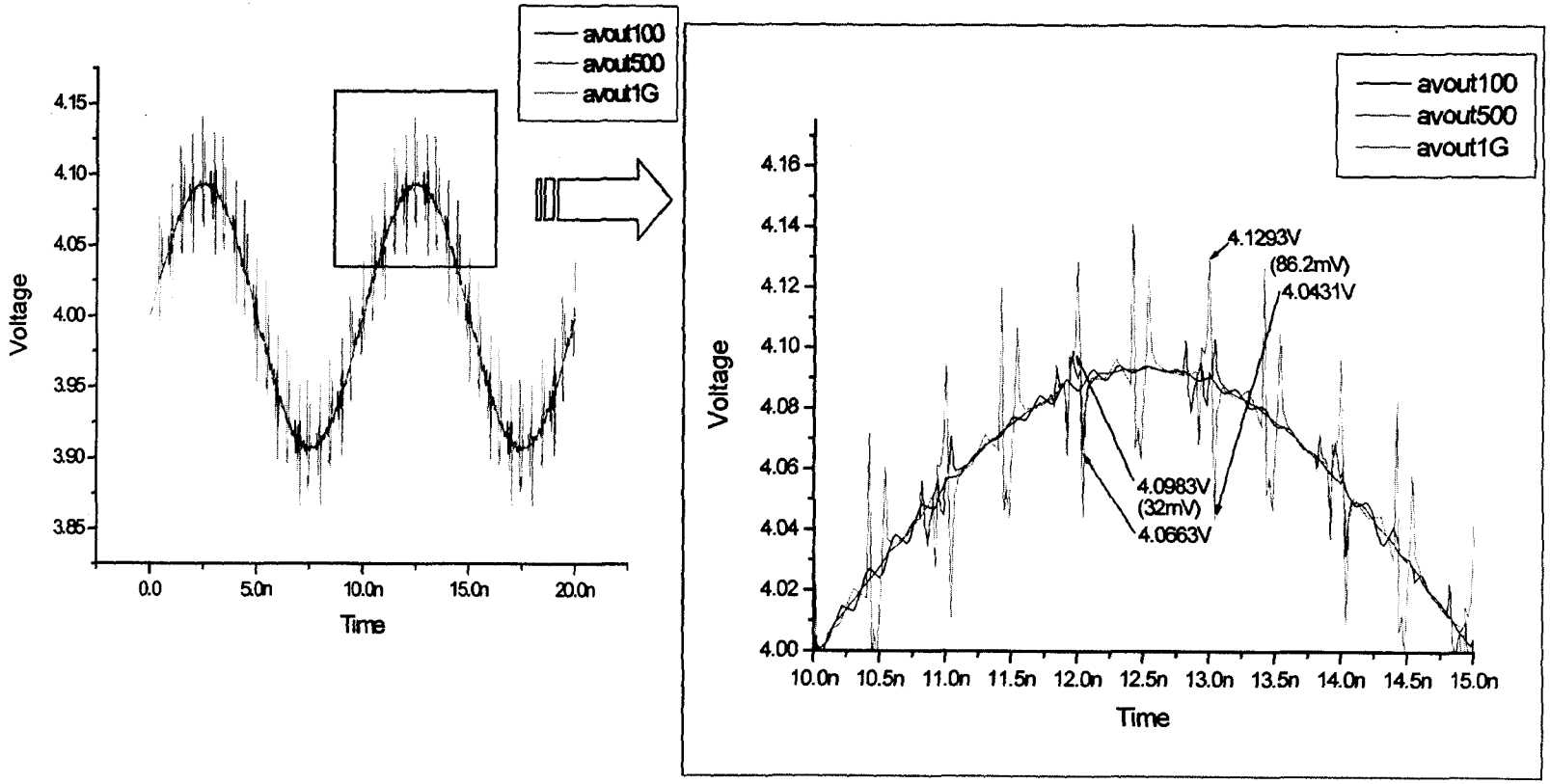
9. Silicon Substrate Problems



Analog Power Line Noise (Test Point-1)



Output Noises (Test Point-2)



Noise Budgets

➡ ***high integration / fine device / fast cycle time***

fast cycle time means high possibility of all the noise sources to be overlapped within narrow incident time window !!!

Noise Budget

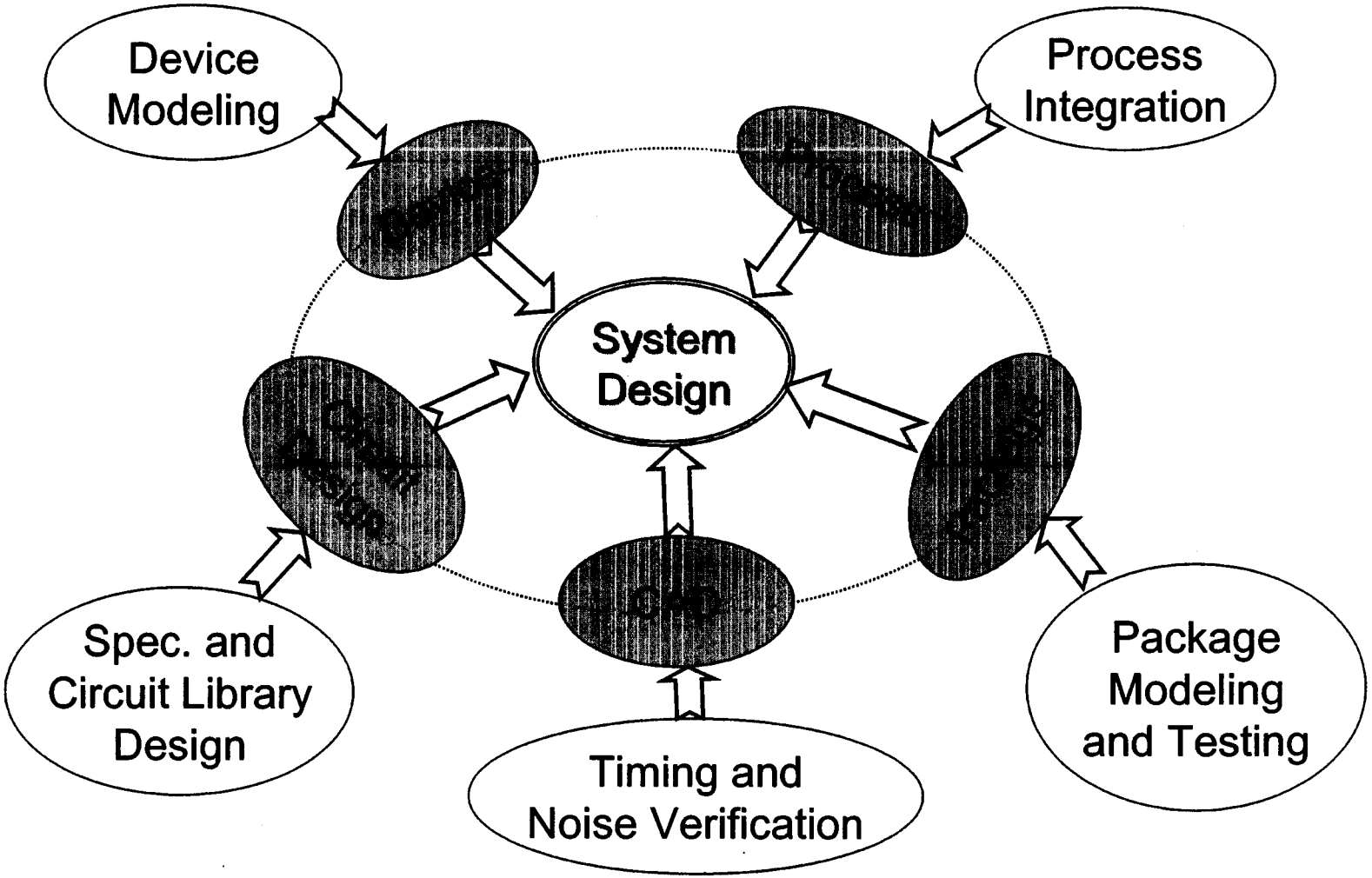
➡ *typical receiver circuit noise margin is about* ±35% ~ ±40% *of the total voltage swing.*

- X-talk uses ±20% ~ 25%
- Delta-I uses ±5%
- Switching threshold voltage variation use about ±3%
- Remaining ±7% is used for other noise sources

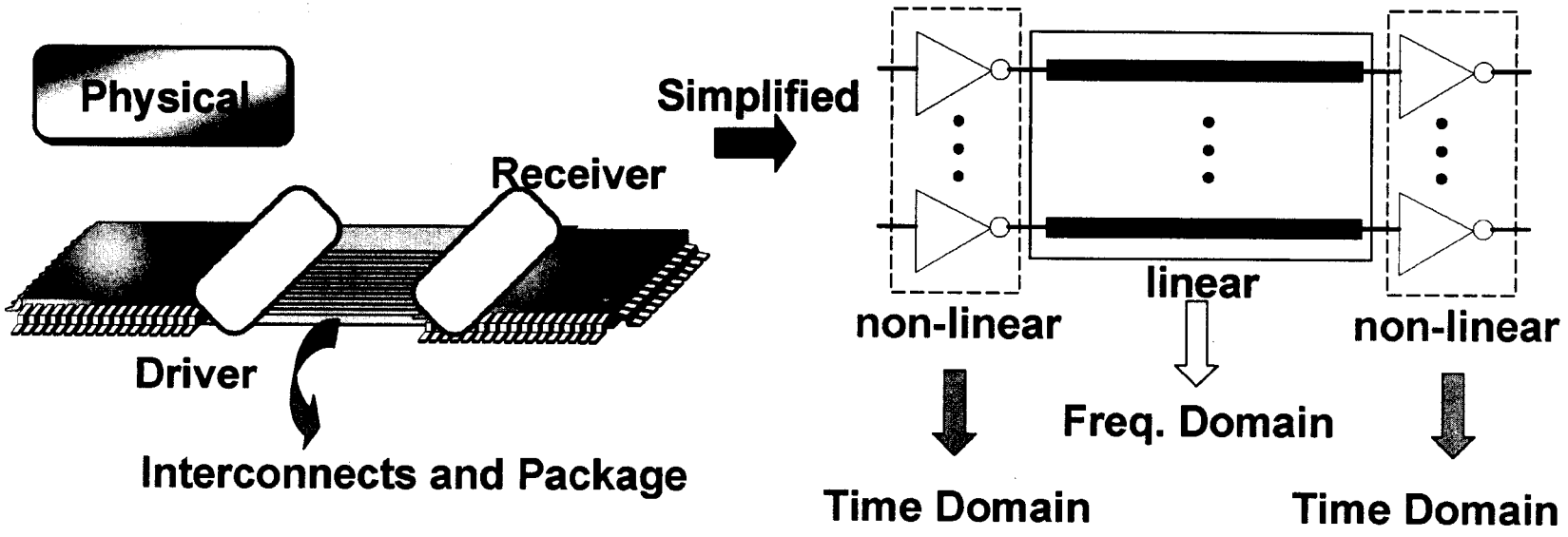
- ***Estimation-Based Design ?***

How ??

Solutions for Future Technology Development



Generic Simulation Problem for Complicated Network



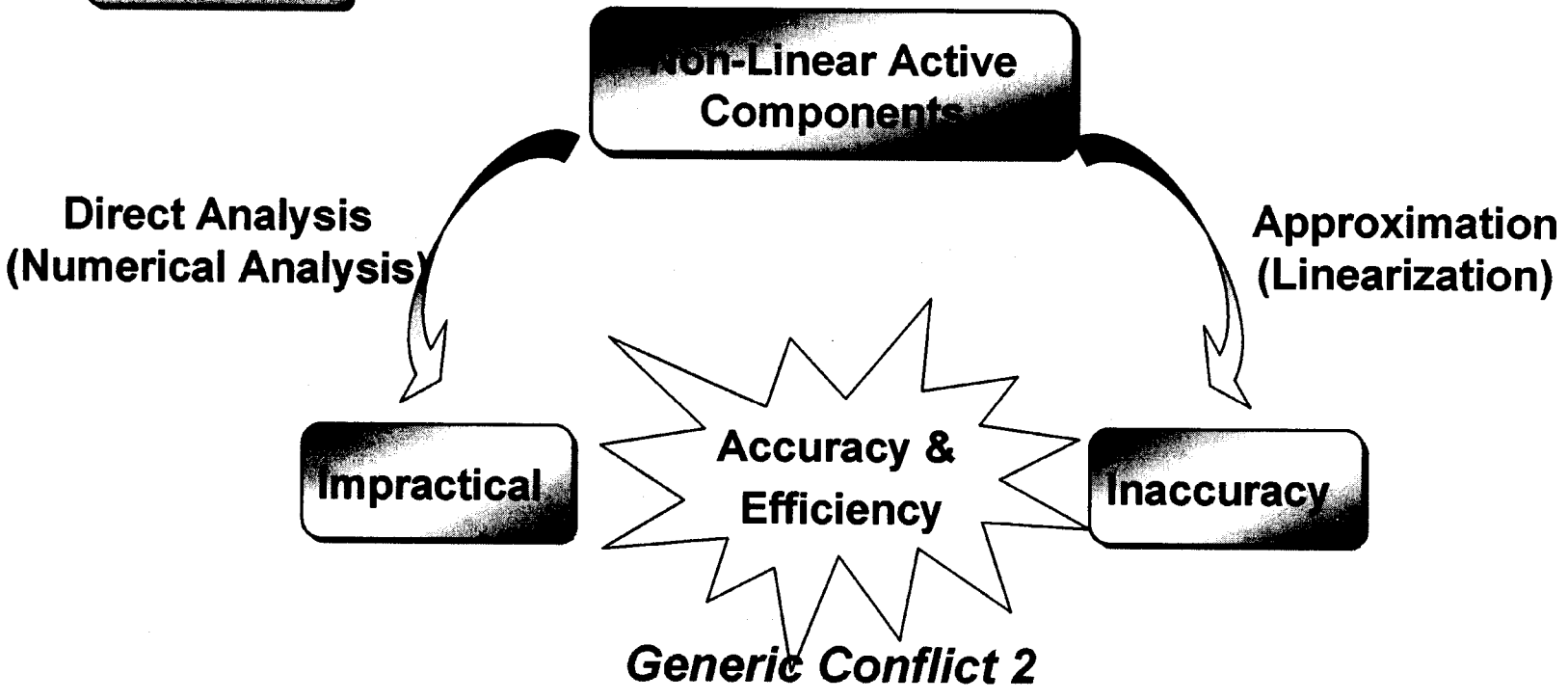
Conflict 1

Active & Components : Can be well described in Time Domain
Interconnect & Package : Can be well described in Freq. Domain

➡ *Domain – Transform ; Generic Conflict 1*

- continued -

Conflict 2



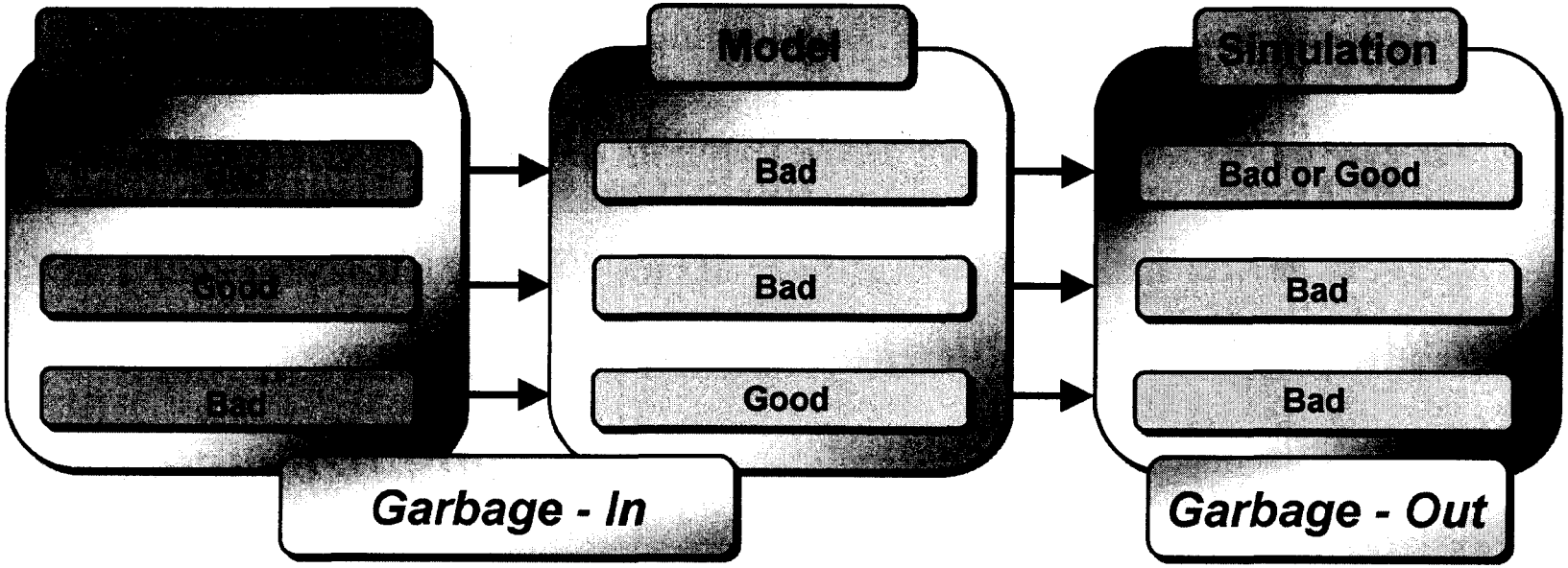
Generic Conflict 2

Thus, W/O Domain Transform and W/ Approximation(Linearization)
but What are the Tolerable Boundaries?

➡ *Compromise (Trade – Off)*

Conflict 3

Inherent Inaccuracy in Model, Parameters, & Simulation !!!



CAD Tools ?

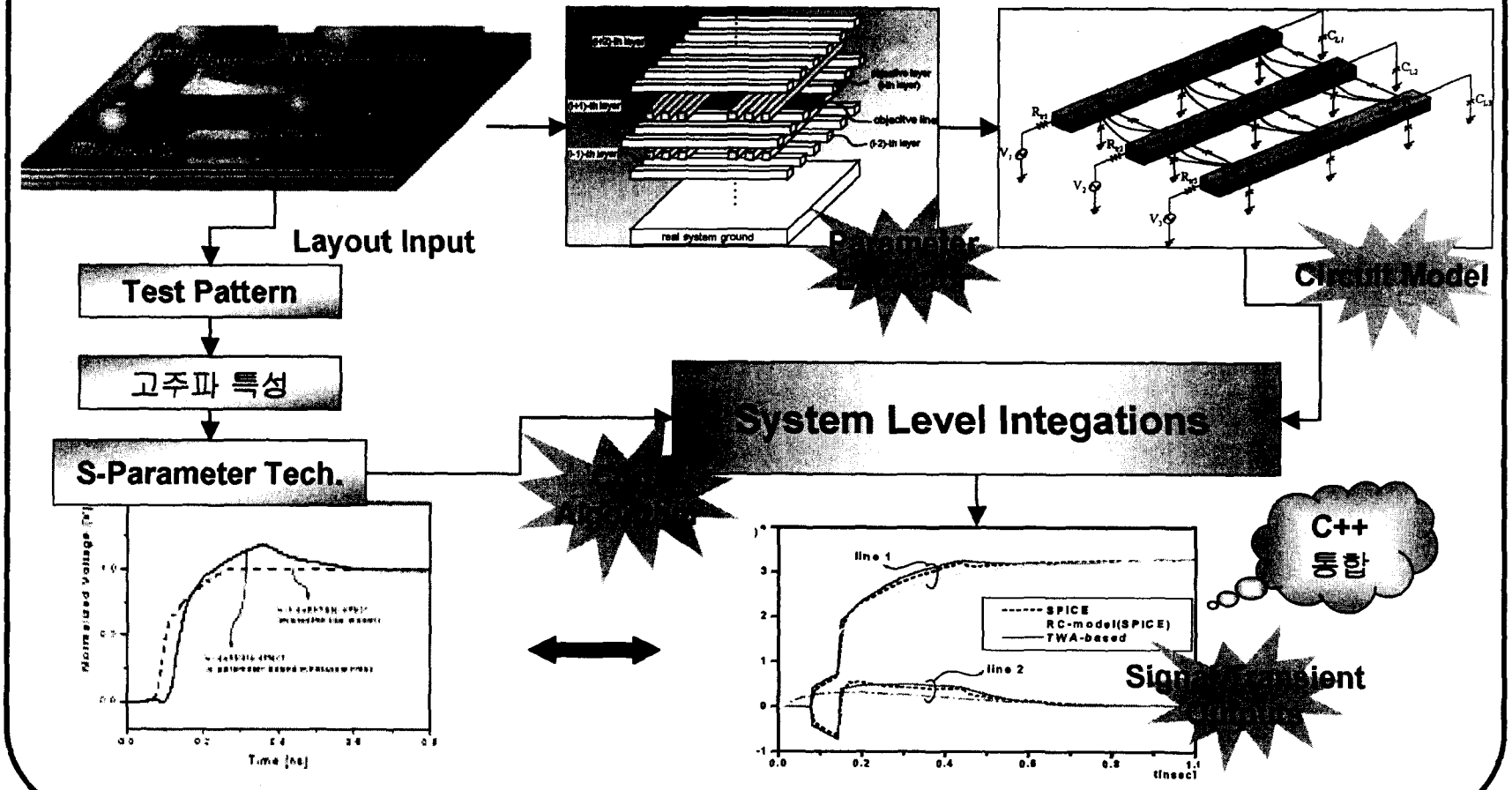
Still Do you believe the CAD Tools ?

- Masakazu Shoji -

- *"The Present Design Automation" means "Low Performance" Chip Design !!*
- *"Circuit Simulation" is essentially a "Mechanical Procedure" without Thinking !!*
- *Why "Circuit Design Failures" occur ? Answer is Simple: Because we don't understand their working "Well Enough" !!*

Estimation-Based System Design

How to Estimate Signal Transients and Noises?



Conclusion

➡ *Future Circuit Design means*
"Unimaginably Intricate Engineering Problems"

Thus,

Future Circuit Designers may be "Victims" of
"Inexorably Complicated Signal Integrity Problems"