소더 Reflow시 발생하는 잔류 휨 양상의 측정과 플립칩 전자 패키지 신뢰성에 미치는 영향

(Solder Reflow Process induced Residual Warpage Measurement and Its Influence on Reliability of Flip-Chip Electronic Packages)

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Abstract

To meet the future needs of high pin count and high performance, package size of flip-chip devices is constrained to become larger. In addition, to fulfill the environment issues, lead free solders will be replacing lead contained eutectic(Sn/37Pb) in near future. Thus, in this work, the effect of residual warpage and consequent residual stress on the reliability of large flip-chip using lead free solder is examined. Several effective experimental approaches to accurately measure residual warpage, using moire interferometry, shadow moire, and image processing schemes, are introduced. Moreover, geometric, process, and material parameters affecting the residual warpage during reflow process are discussed and some modifications are suggested. Finally, it is verified that it is crucial to accurately quantify and control the residual warpage in order to guarantee the overall reliability of flip-chip packages regardless of presence of underfill.