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# CMOS 아날로그 보청기 증폭회로의 최적 설계

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# Optimal Design for CMOS Analog Hearing Aid OP Amp Circuit

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## Abstract

Short channel IC circuits become increasingly important in modern high performance electronic systems. In this paper, parts of an analog hearing aid, an amplifier and a regulator, which are implemented with short channel CMOS devices, are designed and optimized in its performance.

## I. Introduction

The amplification part of a hearing aid consists of several channels. Every channel covers a part of frequency band and provides a variable gain to a changing signal. The gains of different channels are also different because of the individual requirement. Therefore, by adjusting the gain of these channels, we are able to compensate for the hearing impairment. The channel circuits are rather complex and there are many designs on this point. Anyway, it mostly contains regulators, amplifiers, filters, equalizers, etc.

**Regulators** : The hearing aid is powered by Zinc-air battery, which generates approximately 1.4V when it is in use. Fig 1 shows the supply voltage of the battery changing with time. In addition, that even in the flat part, the voltage supply is unsteady.

Therefore, the regulator, which changes the battery supply voltage to a constant value, is of great importance. In this paper, we use a simple linear regulator. Despite its low efficiency, the linear regulator does an excellent job.

**Amplifiers** : The operational amplifier is another important component as well as the regulators. In addition, the design of the regulators will use qualified op-amps. Therefore, low power low supply voltage op-amps are wildly used in hearing aids. In this paper, the op-amp has a high gain at all frequency (125Hz to 8kHz). In the channels, the following circuit will modify signal for hearing impairment compensation. Owing to developing of the short channel devices, a standard two-stage op-amp is good enough to be used here.

## II. Design and Optimization

The regulator and the op-amp are implemented within CMOS technology. The design and simulation are all based on the TSMC .35μ fabrication process parameters.

## II.1. Regulators

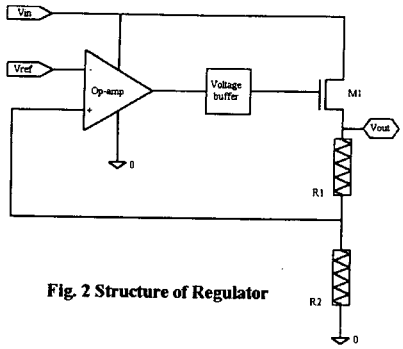


**Fig. 2 Structure of Regulator**

**Design and Circuit Description:** The regulator used in this paper is a simple linear regulator. It consists of voltage reference, error amplifier, voltage buffer and a resistance feedback network. Fig. 2 shows the structure of the regulator. A CMOS voltage reference based on weighted difference of gate-source voltages between PMOS and NMOS transistor [2], shown on Fig. 3, generates a steady reference voltage. The error amplifier with the feedback network amplifies the reference voltage to a desired value via the ratio of R1 and R2, 1.3V in this case. In addition, it adjusts the output voltage to be a constant automatically. The output load of the regulator is the following amplification parts, channels. It has big equivalent impedance.

Voltage reference is an essential building block in a linear regulator. The voltage reference used here is based on the threshold voltage difference of PMOS and NMOS transistors [2]. Three parts form it; a low-voltage bias circuit (M1-M4 and RB), a start-up circuit (Ms1-Ms3), and reference core circuit (Mp, Mn, R1 and R2).

**Optimization and Results:** Hspice provides a very powerful optimization tool for users. Here we use the curve fitting optimization tool. Set a wanted curve, then compare it with the result of simulation and get a steadiest one. The aim of optimization is to: Scale all the transistors and resistors; Get a steadiest output of the voltage reference.

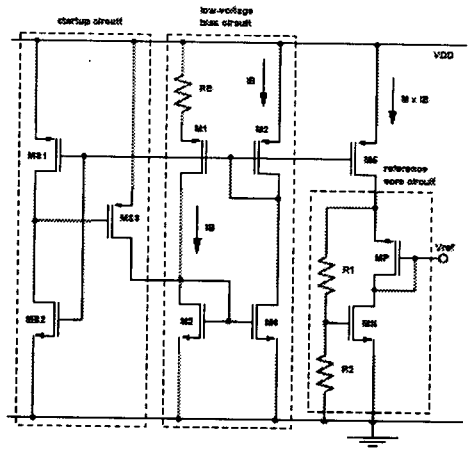


**Fig. 3 CMOS Voltage Reference**

The battery supply voltage varies between 1.35V and 1.45. In this range, the output of the regulator is almost a constant, 0.345V.

**Table 1. Optimization Results**

| Transistor | W/L (μ m/μ m) | Transistor | W/L (μ m/μ m) |
|---|---|---|---|
| MS1 | 1.70 | M3 | 8.70 |
| MS2 | 16.1 | M4 | 8.70 |
| MS3 | 11.6 | M5 | 101.95 |
| M1 | 6.30 | MP | 8.40 |
| M2 | 5.10 | MN | 16.20 |

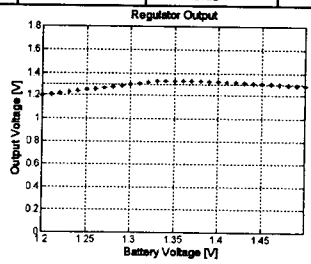


**Fig. 5 Regulator Output – Battery Voltage**

With the voltage reference, we get a linear regulator. The performance of the regulator is shown on Fig.5.

## II.2. Op-amp

**Design and Circuit Description:** The design begins with the analysis of the requirements of the hearing

aid. The input signal is from the former stage, microphone. Moreover its amplitude usually varies between - 1.0mV and + 1.0mV. The supply voltage is about 1.3V, which is stable from the regulator mentioned above, and other detail specifications are listed below.

**Table 4. The Desired Spec**

Then comes the selection of the op-amp structure. Because of the reduction of the channel length and threshold voltage, many standard circuits can be used in low supply voltage cases. Here we use standard two-stage op-amps. The low supply voltage is well enough to driver the circuit and we can use the high gain of the standard two-stage op-amps thought the efficiency is not so good. The top level schematic is shown in Fig 6.

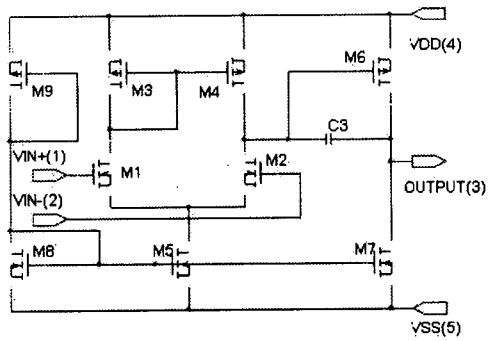


**Fig. 7 Core Circuit**

**Core circuit** Fig 7 shows the schematic of the core circuit. It consists of two parts, the differential pair and the gain stage, which is also the output stage. M1 and M2 is a differential pair with active loads, M3 and M4. The purpose of the second gain stage is to provide additional gain in the amplifier. It is consisting of transistors M6 and M7. M7 amplifies the output of M2 and the M6 serves as an active load of the M6. It is also a simple class A output stage. C3 is a compensate capacitor. The third step is to select dc currents and begin to size the transistors and design the compensation circuit. With given specifications, the main parameters of the circuit, such as W/L ratios, are available. The parameter list based on hand calculation. It is the initial guess of the optimization.

**Table 5. Hand Calculation Results**

| Transistor | W/L (μ m/μ m) | Transistor | W/L (μ m/μ m) |
|---|---|---|---|
| M1 | 3.2 | M6 | 52.7 |
| M2 | 3.2 | M7 | 31.5 |
| M3 | 1.1 | M8 | 3.8 |
| M4 | 1.1 | M9 | -- |
| M5 | 3.8 | | |

**Optimization** In this part, curve fitting and goal optimization tools will be used to get a qualified op-amp. The aims of optimization:

Scale all the transistors; use the hand calculation results as the initial guess. Get a desired AC small signal Gain at the desired frequency range, 125Hz - 8kHz.

Minimize the power dissipation and get a desired setting time.

According to the aims of the optimization, we divide the optimization into 2 steps.

First, scale the transistors, and get a satisfied gain and frequency bandwidth. We use the curve fitting to satisfy these two requirements. Table 6 shows the comparisons of the hand calculation and Optimization results of the W/L ratio of all the transistors. Then we may adjust some of these parameters to get other required specifications.

Secondly, minimize the power dissipation and get a desired setting time. The goal optimization was used in this step. The power dissipation should be as smaller as possible. The goal is to reduce it to the 100uWatt or less. In addition, the sitting time, should less than 500us.

## III. Simulation and Results

Open-loop transfer characteristic.

In open-loop characteristic simulation, we got the output swing of the circuit, -1V to 1V. Because the offset voltage is about -0.003V, set it to zero. The Fig. 8 shows the curve.

Open-loop transfer function response.

Open-loop transfer function response is shown in Fig. 10 and Fig. 11. The small-signal gain is about 38.8dB. That is, the output signal is about -.85V to .85V. It is quite enough for the input of the receiver.

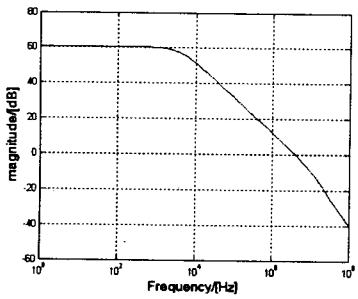


**Fig. 10 Open loop Transfer Function Magnitude Response**

The ICMR, CMRR and Setting time

The CMMR we get like this, to measure differential voltage gain in dB and then common-mode voltage gain in dB by applying a common-mode signal to the input. The CMMR in db could b found by subtracting the common-mode voltage gain in dB from the differential-mode voltage gain in dB.

There, the CMMR = 60.47-(-7.82) = 68.89dB.

**Fig. 12 PSRR+ Magnitude Response**

**Fig. 13 PSRR+ Phase Response**

So the PSSR+ = 89dB, PSRR - = 80dB

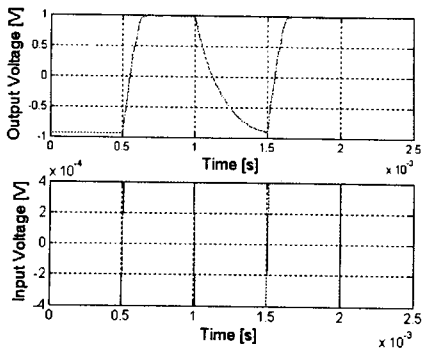


**Fig. 16 Swing time**

The Swing time + = 300μ s, Swing time - = 500μ s.

## III. Conclusion

A regulator and an op-amp used in a hearing aid have been designed and optimized. By using small channel devices, the supply voltage of the circuit can be greatly reduced. The optimization based on the hand calculation helped to scale and optimal the circuit more efficiently. Simulations show the performance of the two parts of the hearing aid.

**Acknowledgment**

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[3] Hspice User' s Guide , 2002.