A Low Power Multi-Function Digital Audio SoC

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ABSTRACT

This paper presents a system-on-chip prototype implementing a full integration for a portable digital audio system. The chip is composed of a audio processor block to implements audio decoding and voice compression or decompression software, a system control block including 8-bit MCU core and Memory Management Unit (MMU) a low power 16-bit ΣΔ CODEC, two DC-to-DC converter, and a flash memory controller. In order to support other audio algorithms except Mask ROM type's fixed codes, a novel 16-bit fixed-point DSP core with the program-download architecture is proposed. Further, an efficient power management technique such as task-based clock management is implemented to reduce power consumption for portable application. The proposed chip has been fabricated with a 4 metal 0.25um CMOS technology and the chip area is about 7.1mm x 7.1mm with 100mW power dissipation at 2.5V power supply.

I. INTRODUCTION

The demands for high-quality digital audio systems are now being increased. In company with the development of digital video and image processing, digital audio technique is also being improved. Specially, MPEG Audio based on ISO/IEC [1] is the most well known technique. As more consumer products become portable, the implementation of digital audio algorithm need low power architecture. Moreover, as even portable communication devices such as cellular phone and PDA and DMB, tend to support the digital audio algorithm for audio-on-demand services, low power consumption and cost effectiveness become more important.

Through a hardwire implementation of audio algorithms, or a porting audio algorithm with MCU/DSP Core, many kinds of digital audio chips have been developed. A hardwired chip could not implement flexibility of algorithm and full function of digital audio system [2]. Chips porting audio algorithm with DSP/MCU Core consume large power because of high-width data-path and more cost to develop system because of high cost DSP/MCU core with high performance [3] [4]. In this paper, a low power flexible digital audio SoC with cost effectiveness based on 16-bit fixed-point DSP core and 8-bit 8051 MCU core are proposed. In order to improve the performance of 8-bit 8051 MCU, MMU with Direct Memory Access (DMA) and FIFO is included. To download newer algorithm in DSP core, the program-download architecture is proposed. And in order to save cost of digital audio system, a low power 16-bit ΣΔ CODEC, two DC-to-DC converters, a memory controller to support flash memory are included. The remaining part of this paper consists of four sections. In Section II, the basic configuration of digital audio SoC is described. Chip design technique, configuration of sub-block, chip layout, experimental results discussed in Section III. We will conclude in Section IV.

II. SYSTEM ARCHITECTURE

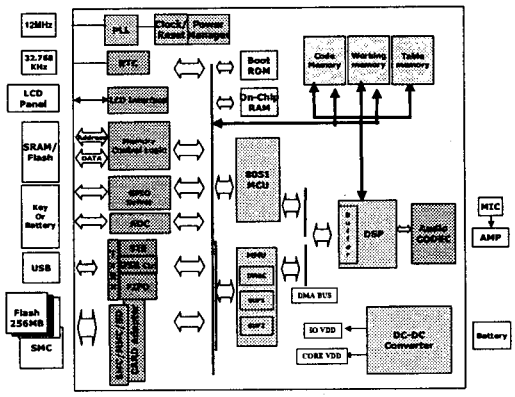

Figure 1. Block Diagram of the digital audio SoC

A block diagram of the digital audio SoC is shown in Figure 1. The SoC consists of Audio processor with DSP core, MCU, Memory Management Unit (MMU), Universal Serial Bus (USB), Phase-Loop-Locked (PLL) and analog blocks. The digital audio SoC receives audio bit stream from flash memory through MCU and memory controller. It decodes the bit stream and generates decoded output. After the decoded output is converted into analog audio sound at DAC block of CODEC, an audio amplifier drives a headphone. Further, the analog data MIC can be converted into digital data through an amplifier and the ADC block of CODEC. MCU controls all of the

system operations such as checking of status changes of Keypad, sending commands of data to IO interface, managing data storage, and communicating with audio processor. General Propose IO (GPIO) and SAR-ADC are used for user interface. Flash memory is used for storage and Flash memory interface is supported. USB interface is used to download or upload audio file or voice data between the digital audio system and a host. More USB interface is used to download flexible audio algorithm. PLL generate the system clock for digital blocks and the audio clock for the audio CODEC. The Audio CODEC is a low voltage 16-bit A/D & D/A converter for portable digital audio applications including speech encoding and audio decoding. DC-DC Converter is a high-efficiency, low –voltage, synchronous-rectified, step-up DC-DC Converter intended for use in devices powered by 1-cell alkaline, NiMH, or NiCd batteries or lithium battery.

III. CHIP IMPLEMENTATON

A. Micro-Control System

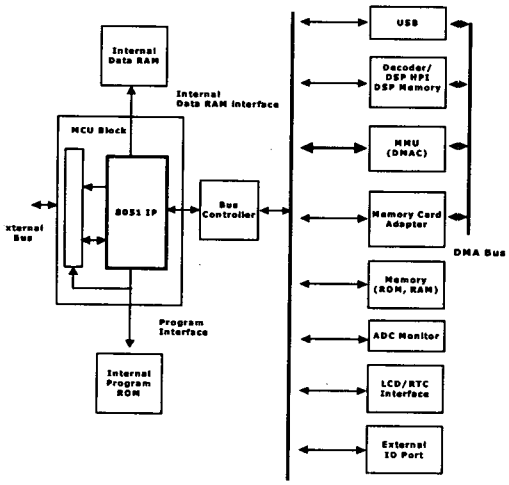

Figure 2. Block Diagram of the Micro-Control System

The block diagram of the micro-control system is shown in Figure 2. The 8-bit 8051 MCU implements the user interface by directly driving an alphanumeric display and managing a set of keypad through interrupt signals. Startup code, download code and other low-level firmware are stored in the internal program ROM to be available at the system power-up and downloading flexible algorithm code. The internal data RAM is partitioned in two different banks. One bank is used for Register Memory and Data Memory, the others is used for Data Memory only. The second bank is further split into 8 selectively accessed RAM modules to reduce total power consumption by use of clock gating. The MMU is used to extend performance of the 8051 MCU and has 1Kbytes FIFO memory for template storage to transfer data, an 8-bit DMA. DMA supports four different operations to access system bus by configuring software-accessible registers and four channels for source and destination. The channels are USB, Host Processor Interface (HPI) port of audio processor, Smart-Media-Card (SMC) [5], multi-Media-Card (MMC), [6] Secure Digital (SD) [7]. DMA performance can extend the performance of the 8051 MCU by 4 times. Other peripherals of the 8051 MCU are Real Time Clock (RTC), Timer, UART, LCD interface and SAR-ADC.

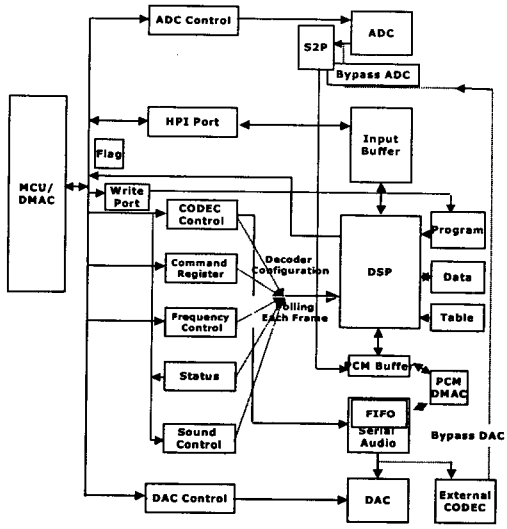

Figure 3. Block Diagram of the Audio Processor

B. Audio Processor

The block diagram of the audio processor part is shown in Figure 3. The audio processor has been designed on the basis of the 16-bit fixed-point DSP core.

The HPI port receives or transmits bit stream. In case audio decoding, the received bit stream is transferred to Input Buffer through DMA controller. DSP accesses Input Buffer to get the bit stream and decode it. When decoding process is done, the result is loaded into PCM Buffer. By using DMA operation, the data stored in PCM Buffer are transmitted to DAC of CODEC through Serial Audio Buffer. In case of voice recording, the voice data generated by ADC of CODEC is loaded into PCM Buffer by use of DMA operation through Serial Audio Buffer. Then, the voice data is compressed by DSP and loaded into Input Buffer. The data of Input Buffer are transmitted to MCU through DMA operation to be stored in the flash memory. In case of voice compression and decompression operation, lots of memory resources are needed. The Write Port is used to download or upload program and

table through DMA operation. Executable modules up to 15Kbytes are downloaded to program RAM from dedicated sectors of the flash memory through an 8-bit Direct Memory Access (DMA) and the Write Port. Further the audio processor supports the digital volume control, bass/treble control, and 10-band equalizer function. These features are helpful in implementing various sound effects and controlled by MCU.

Audio/ Voice	Program KW	Data KW	Table KW	MIPS
MP3	6.5	11.0	7	25
MTRSC	8.7	8.5	4.5	10/28
G.726	3	2.7	3	7
G.729A	8.7	3.5	8	10
MTSM	1	2	0.25	12
VOR	0.15	0.21	X	0.15
WMA	8KW	10KW	15KW	40

Table 1. Memory Size and Performance

The DSP core is based on an advanced Harvard architecture that has one program memory bus and three data memory buses. This DSP core provides an Arithmetic Logic Unit (ALU) that has a high degree of parallelism, application-specific hardware logic, a highly specialized instruction set, which is the basis of the operational flexibility and speed of DSP. The DSP core has also 6 pipeline stage: Pre-fetch, Fetch, Decoder, Access, Read, Execute and 17x17 Parallel Multiplier Coupled to a 40 –bit dedicated adder.

The total memory size of audio processor and the performance of algorithm are shown in Table.1.

D. Power Management Scheme

The power management feature of the digital audio SOC can make the SoC get into very low-power dormant state through hardware or software control. There are 4 power management states in the proposed SoC: RUN, LOAD, Wait, SLEEP, and POWERDOWN. In Run State, the SoC is fully working to decode bit stream or compress and decompress voice data except USB interface. In LOAD State, the USB interface is working and the clock of the audio processor is down. In WAIT state, the SoC is waiting user interactions or data. In this state, only some peripheral blocks are active. In SLEEP state, only PLL is active, and all other blocks of SoC are inactivated. In POWERDOWN state, all the blocks of SoC are power-downed.

The digital audio SoC has three strategies for clock gating to power management. First, because audio processing is independent of USB download or upload, the clock for USB interface can be disabled in audio processing mode and vice versa. Second, when the MCU makes WAIT or SLEEP for power down or audio playing paused, all of the clocks in SOC are disabled. Finally, based on analysis of audio decoding algorithm and voice compression or decompression algorithm, we decouple the module of audio processes and apply independently the clock management to each decoupled modules. And also decouple the memory of audio processor and apply independently the clock management to each decoupled memory modules. For example, the clock generation block monitors the states of the DSP block and PCM Buffer controller, Input Buffer controller. When they wait for the next audio data in idle state, the clocks for them are masked and disabled.

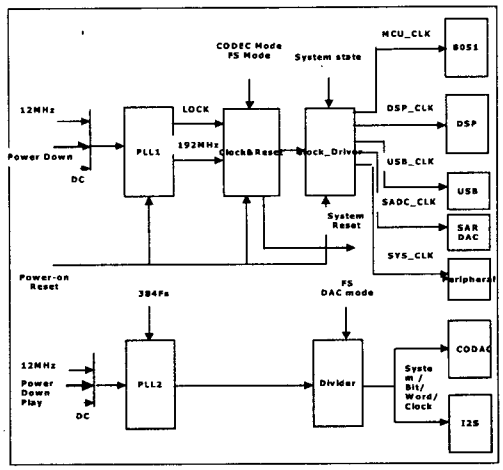

Figure 4. PLL and Clock Management

PLL1 generates the master clock for SoC and clock divider generates the clock of sub-block. PLL2 generates the audio master clock for the audio CODEC. Clock divider generates Word clock and bit clock. Figure 4 shows the overall clock management for each block including PLL.

E. Audio CODEC Configuration

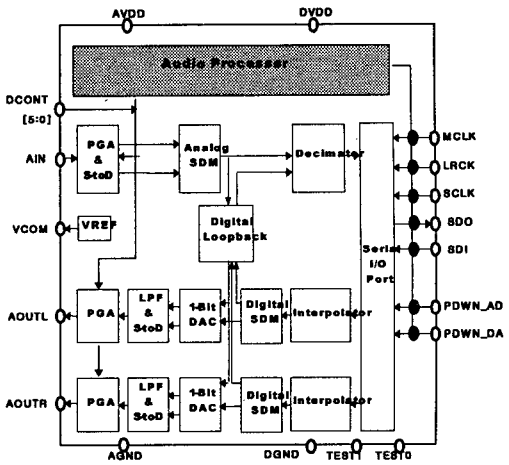

Figure 5. Audio CODEC Configuration

The Audio CODEC is a low voltage 16-bit A/D & D/A converter for portable digital audio applications including speech encoding and audio decoding. It features a 16-bit A/D conversion channel for speech and two 16-bit D/A conversion channels for digital audio. Also It is suitable for a variety of

applications in the speech, telephony and audio area including low bit rate, high quality compression. speech enhancement, recognition and synthesis, etc. Also the analog input and outputs are single-ended to allow low power consumption and smaller package.

The master of audio CODEC can be 256fs. The hardware has been designed to support all sampling rate specified in MPEG standards, 48, 44.1, 32, 24, 22.05, 16, 8KHz. The relationship between the external clocks applied to the master input and the desired sample rate is defined in generally. The word clock input must be synchronized with master, however the phase is not critical. Figure 5 shows the audio CODEC configuration.

F. Chip Implementation

Figure 6 shows the chip layout of the digital audio SoC. It is composed digital logics including DSP core and MCU core, USB interface, working memory, program memory, audio CODEC, SAR-ADC, and PLL for clock generator. All the digital blocks of SoC are implemented top-down approach, on the basis of HDL. Further, we have carried out a HDL synthesis with low power 0.25um CMOS ASIC library. In order to satisfy the specified timing constraints, the result of floor planning is fed back into synthesis stage. In case of analog block such as CODEC, SAR-ADC, DC-DC and PLL, we have designed them with a full custom method.

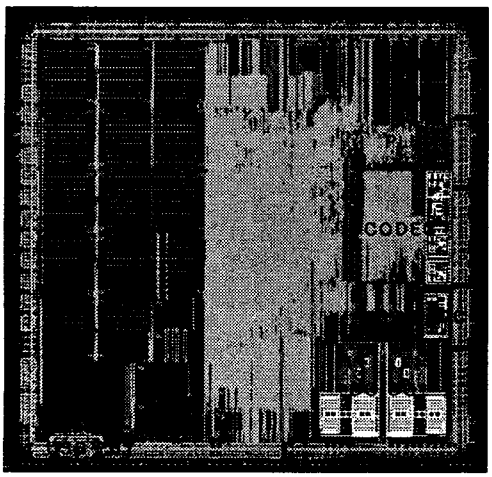

Figure 6. Chip layout

The characteristics of the digital audio SoC were described in Table 2.

Power Supply	3.3V IO, 2.5V CORE
Process	0.25um 4-metal CMOS
Package	128 pin QFP
No. of Transistors	3,200,000
Chip Area	7.1 mm x 7.1 mm
Power Consumption	138 mW
USB	4M bps
DC-DC	85%
CODEC	82 S/N ADC, 85 S/N DAC

Table 2. Summary of the Proposed Digital Audio SOC

IV. CONCLUSION

A system-on-chip prototype implementing a full integration of a portable digital audio system was proposed in this paper. The main focus of SoC was:

- Higher integration decreases system cost by reducing the parts count and power consumption.
- To reduce power consumption, power optimization strategies are proposed: task-based clock management and task-based memory access.
- In order to satisfy flexibility of algorithm, the program-write-architecture is proposed

The digital audio SoC has been fabricated a 4 metal 0.25um CMOS process and chip area was about 7.1mm x 7.1mm with 100mW power dissipation at 2.5V power supply. The digital audio SoC will be a great role to implement the digital audio system.

References

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