Nanotopography Impact and Planarization Efficiency of Ceria Slurry for STI-CMP

Ceria 슬러리를 이용한 STI CMP의 나노토포그래피의 영향과 평탄화 효과

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Nanotopography is defined as the height variations (normally, smaller than 100 nm) on bare wafer surfaces within a spatial wavelength range of 0.2 to 20 mm. Nanotopography has emerged as a concerning issue in STI process since it impacts on the post-CMP thickness deviation of dielectric films. Ceria slurry with ionic surfactant is widely used in STI-CMP process since it can reduce nitride erosion and widen the processing margin with offering high oxide-to-nitride selectivity in the polishing removal rate.

In this study, we independently controlled the grain size and particle size of the polycrystalline abrasives in a ceria slurry with an ionic surfactant by changing the calcination temperature and the mechanical milling time, respectively, during abrasive synthesis. CMP experiments using slurries with various process combinations showed that the oxide removal rate increased with both the grain size and the abrasive particle size, while the nitride removal rate was independent of both. On the other hand, examination of the nanotopography impact showed that the planarization efficiency increased as the particle size decreased but was independent of the grain size. We also investigated the nanotopography impact on post-CMP oxide thickness deviation and the non-Prestonian behavior of ceria slurry with a surfactant. We found that not only the surfactant but also the slurry abrasive size influence both the non-Prestonian behavior and the nanotopography impact. We made a one-dimensional numerical simulation of the nanotopography impact, based on a wear-contact model. The simulated results achieved good agreement with the experimental results. This work was supported by the Korea Ministry of Science and Technology through the National Research Laboratory (NRL) program. We thank Hynix Semiconductor Inc. and Sumitomo Mitsubishi Silicon Corp. for helping us with our experiments.