특 별 강 연

(전자패키징 기술 현황 및 향후 발전 방향)

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용접학회 Seminar

패키징 기술 개요 및 발전 동향

2004. 11. 11.

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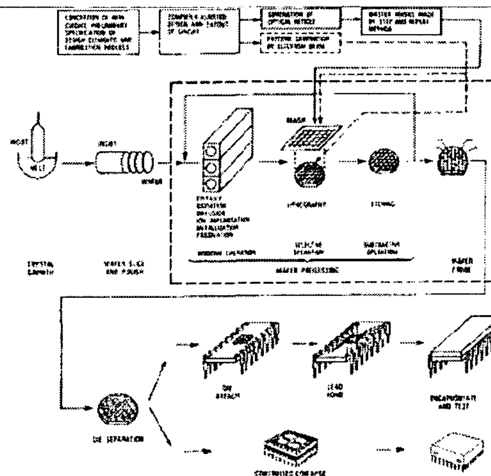
- Introduction
- Trend
- Advanced Packages
- Importance of Joining Technology
- Pb-free solders
- Summary

An Outline of the Manufacture of an IC



Source: JOM

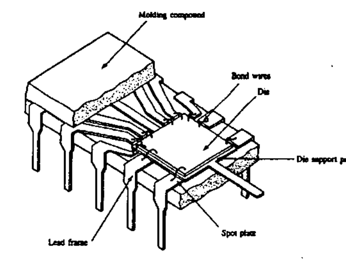
Definition of Packaging and Packaging Structure

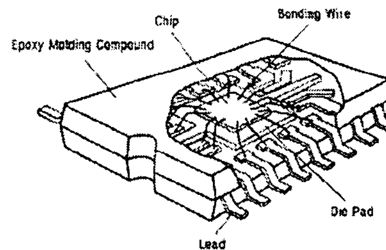
- **Definition**

  "Packaging begins where the chip ends."

  by A.J. Blodgett, Jr

- **Structure**





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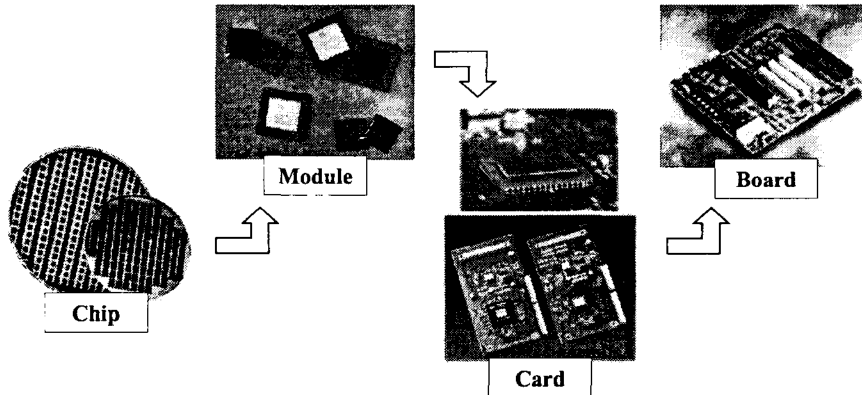
Electronic Package Hierarchy

- 0th Level Package
- 1st Level Package
- 2nd Level Package
- 3rd Level Package



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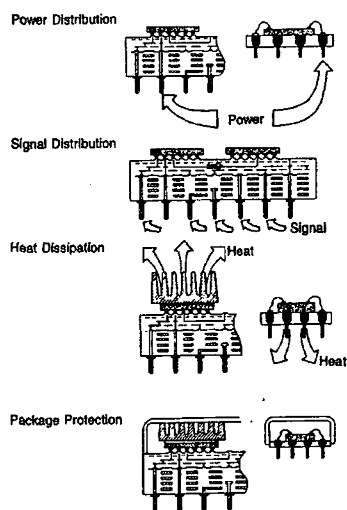
Four Major Functions of the Package



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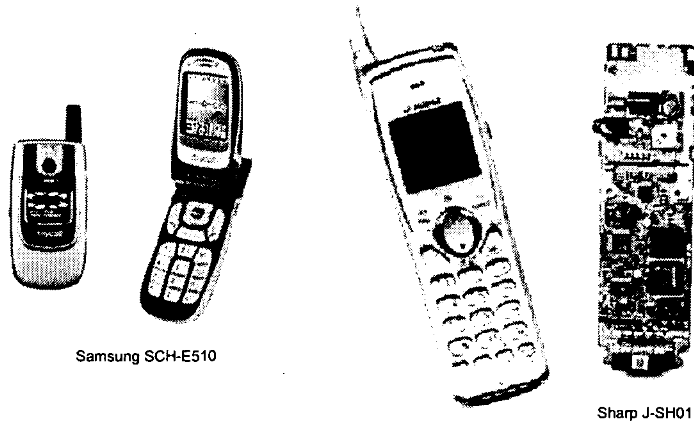
Importance of Electronic Packaging



Samsung SCH-E510

Sharp J-SH01

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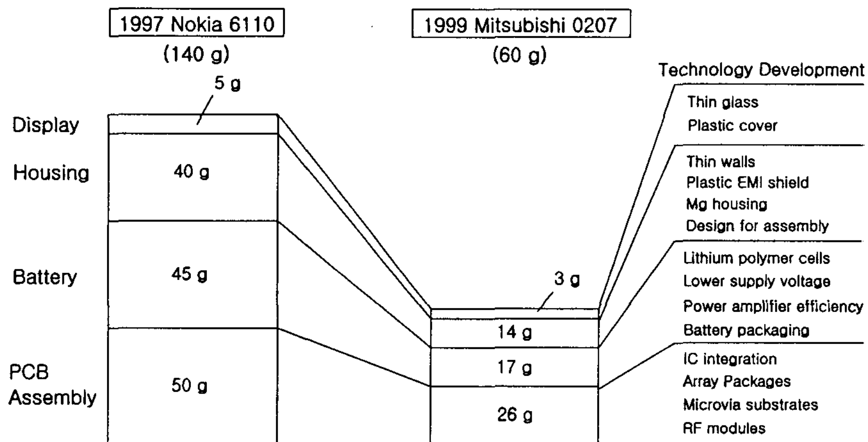
The Shrinking of Mobile Phone



(Source : Prismark)

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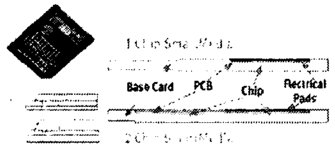
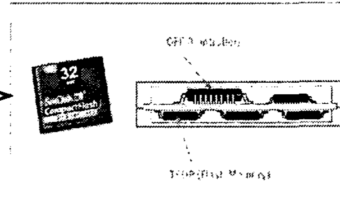
Memory Card Packages

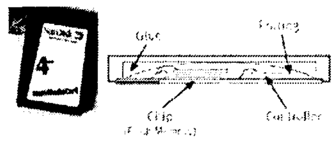
Smart Media Card



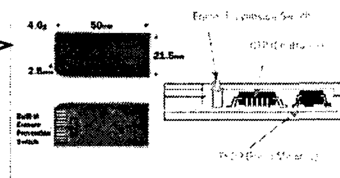
Compact Flash Card



Multi-Media card

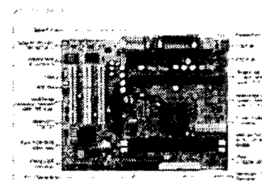


Memory Stick



Cost Evaluation of Personal Computer ($ 1000)

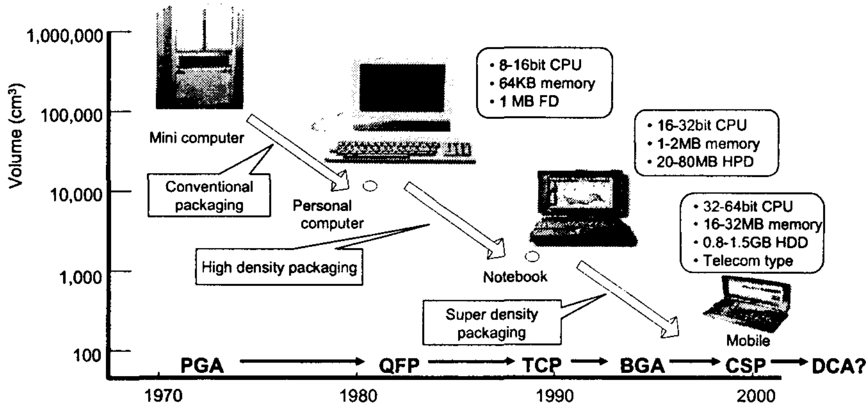
Components	ICs	27 %	
	Discretes	4 %	
	Substrates	4 %	
	Connectors	3 %	38 %
Assembly & Test			14 %
Housing & I/O			16 %
SGA & Profit			16 %
Distribution			14 %
R & D			2 %
Total			100 %



Manufacturing cost

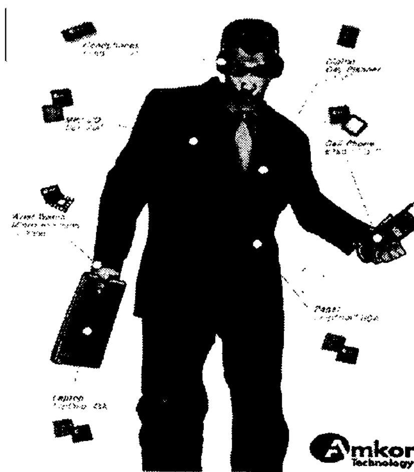
= 68 %

Miniaturization / Volumetric Density Trends



Source: Hitachi Cable

IC packages for portable and wireless applications



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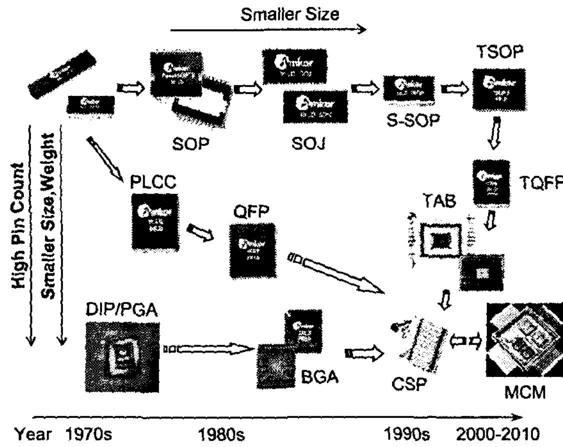
IC Package Trend

- smaller, lighter, thinner shorter, faster
- more friendly functional powerful reliable
- less expensive



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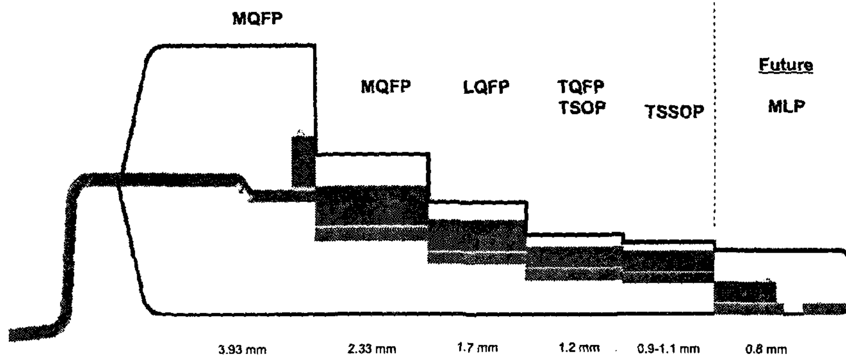
Leadframe Package Total Height Reduction



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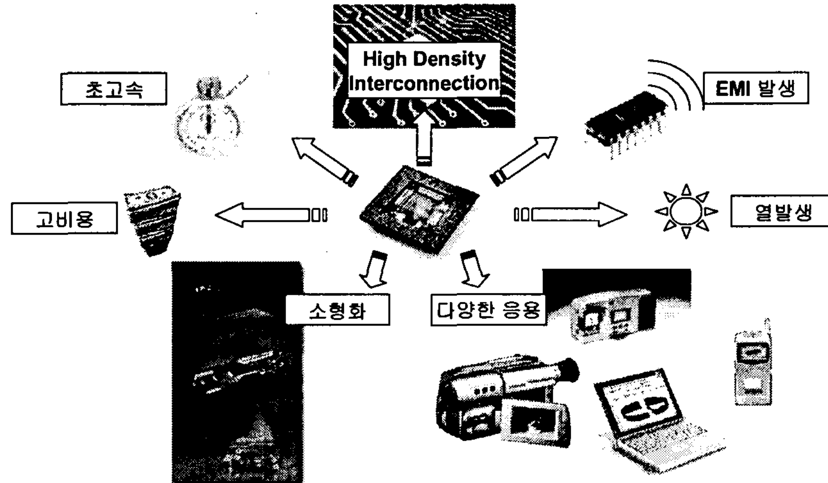
차세대 전자 패키지의 요구조건 및 문제점



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Chip Size Package (CSP)

- **Chip Size Package or Chip Scale Package**
- **Definition by IPC**

  Package area ≤ 1.2 × (chip area)
- **특 징**
  - **Smaller, Thinner, and Lighter**
  - **Better Electrical Performance**
  - **Higher Interconnection Density**
  - **Alternatives for Known Good Die**

    test before assembly

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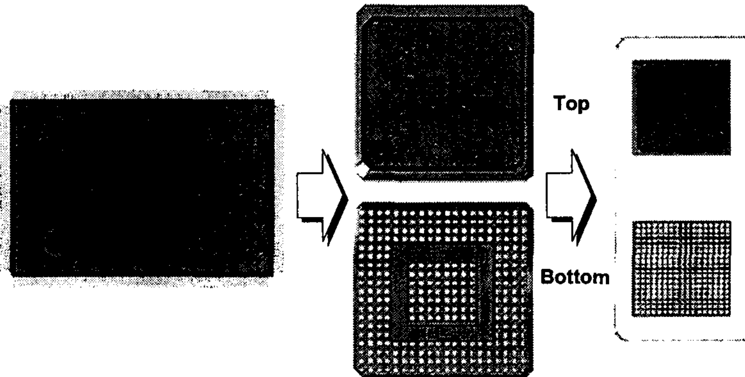
패키지 형태에 따른 크기 비교

QFP	BGA	CSP
QFP253-P-2840	BGA256-P-2323	FLGA320-C-1515



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CSP Classification

Category	Type	Example	Companies
Flex Circuit Interposer	TAB/flip chip		GE, Sony, Mitsubishi, NEC, Tessera and licensees
	Wire Bonding		Fujitsu, Mitsubishi, Sharp, TI Japan, Toshiba
Rigid Substrate	Flip Chip		Citizen Watch, Kyocera, Matsushita, Motorola, Nikko, Oki Electric, Toshiba, Sony
	Wire Bonding		Amkor, Fujitsu, National, NEC, Sony, Toshiba, Oki, Hitachi, Motorola
Custom Lead Frame	TAB/flip chip		Rohm
	Wire Bonding		Amkor, Fujitsu, Hitachi Cable, LG Semicon
Wafer-Level Assembly	Redistribution		ChipScale, EPIC, IME (Sing.), NEC, Sandia National Labs, Motorola
	Substrate		ChipScale and Licensees, ShellCase, Tessera, 3-D Plus, Motorola

Source: TechSearch International, Inc.

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Wafer Level CSP

- **Wafer Level CSP란?**
  - wafer 상에서 직접 패키징 한 후 개개의 칩으로 분리하는 chip size package

  cf) **Die Level Package (DLP)**
  wafer를 die로 분리한 후 개개의 die를 패키징 하는 package

- Features
  - Lower cost due to wafer-level batch process
  - Miniaturization : True chip size (소형화, 경량화)
  - Matured process technologies
  - Performance : short length and controlled dimensions
  - More suitable for memory devices (≤ 150 pins)

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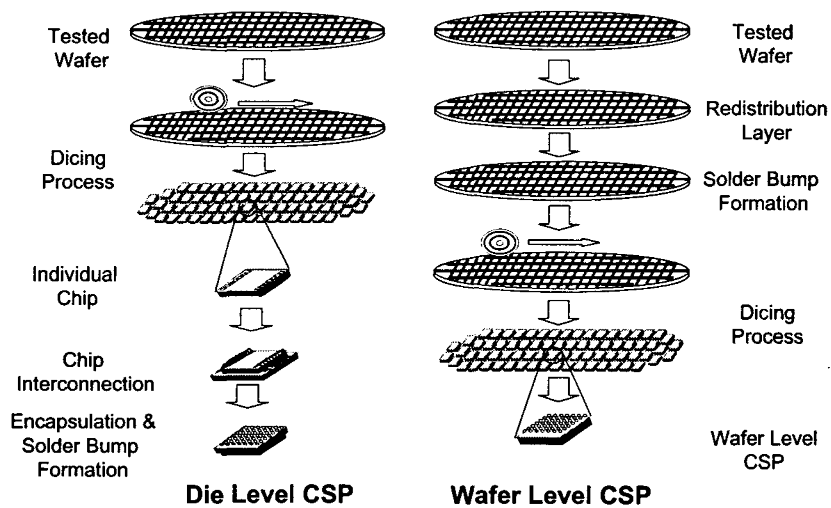
Die Level Package와 Wafer Level Package의 비교



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Multichip Module

- Two or More Dies on the module
- Decreasing the average spacing between ICs in an electrical system
- 특 징
  - 소형 경량화
  - 우수한 전기적 특성
  - lower power consumption
  - Chip density 증가
- 분 류
  - MCM-L (Organic Laminates)
  - MCM-C (Cofired Ceramics)
  - MCM-D (Deposited Dielectric) - Thin Film Module

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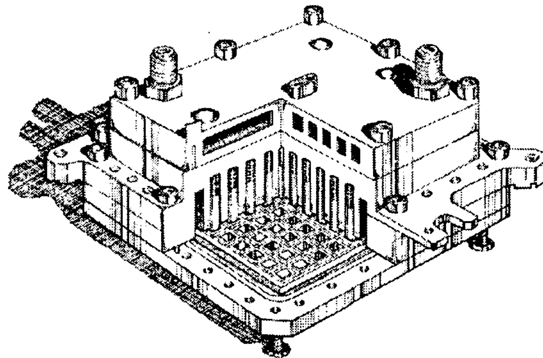
Thermal Conduction Module (IBM)



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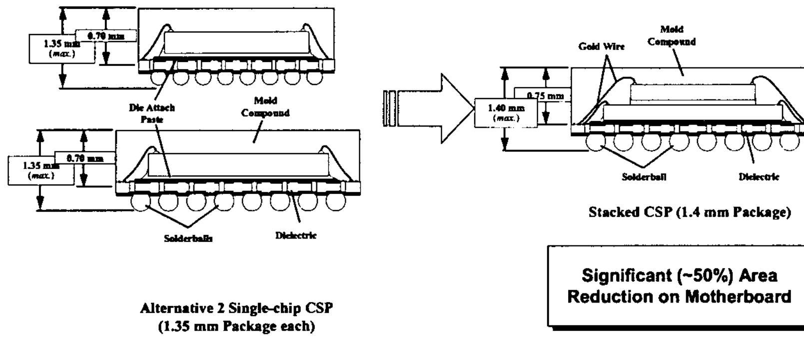
Stacked CSP

Single Package vs. Two Package Solution



Stacked CSP (1.4 mm Package)

Alternative 2 Single-chip CSP
(1.35 mm Package each)

Significant (~50%) Area Reduction on Motherboard

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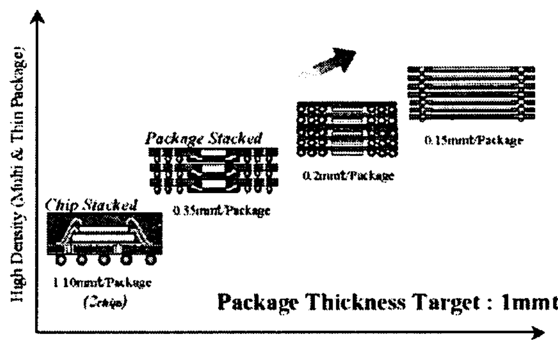
Package Stacked MCP Roadmap



(Source : NEC 2003)

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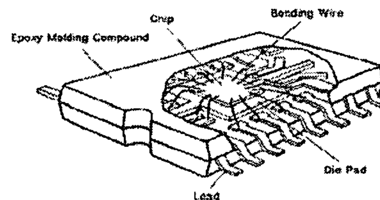
Chip Interconnection 방법

1. **Wire Bonding**
2. **Tape Automated Bonding (TAB)**
3. **Flip Chip Bonding**

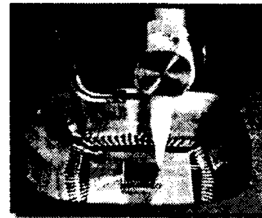


Wire Bonding

● **the most common chip interconnection technique**

(특징)

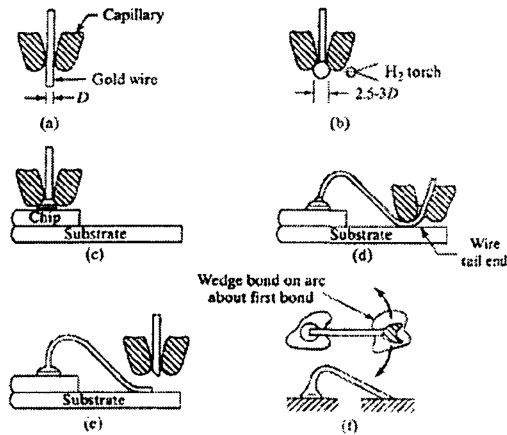
- **경제적, 생산성 우수 (automation)**
- **good flexibility and reliability**
- **I/O density의 제한 (< 300)**
- **inductance 발생 (wire의 길이를 줄여야)**



(공정 방법)

- **Thermocompression method**
- **Ultrasonic method**
- **Thermosonic method**

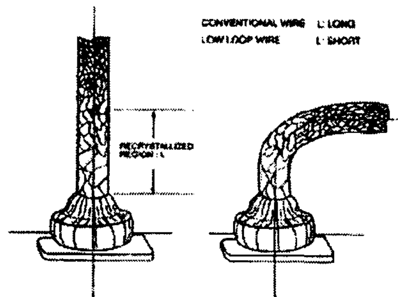
Thermocompression Bonding



Semiconductor International (May 1982)

Heat-Affected Zone

- **Au Bonding Wire**



Microelectronics Packaging Handbook III p.206, (1997)

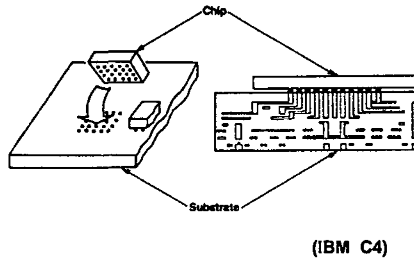
The recrystallization temperature of the wire is controlled by the type of dopants added, which determines the length of this "zone".

Flip Chip Technology

- **Definition**

  the direct electrical interconnection of electronic components onto substrates by means of bumps

- **Characteristics**
  - **Smallest Size**
  - **Greatest I/O Flexibility**
  - **Highest Performance**
  - **Reliable**

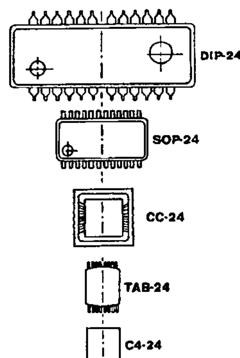


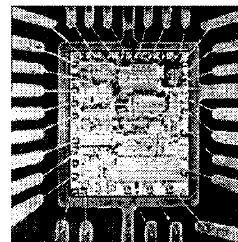
(IBM C4)

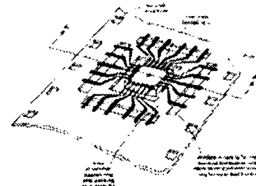
- **Application**

  Flip chip components
  - **Semiconductor device**
  - **Passive component**
  - **Detector arrays**
  - **MEMs device**

Space Efficiency by IC Package Type







Package Space (16K CMOS SRAM)

	DIP-24	SOP-24	CC-24	TAB-24	C4-24
mm X mm	31.0 × 15.24	15.4 × 10.24	11.18 × 11.18	5.65 × 8.87	5.65 × 6.57
mm^2	472.44	157.70	124.99	50.12	37.12
Ratio	12.73	4.25	3.37	1.35	1

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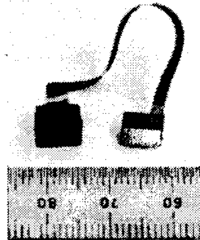
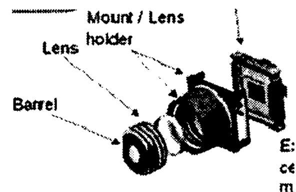
Image Sensor Module

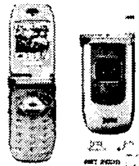
CCM VGA 외관

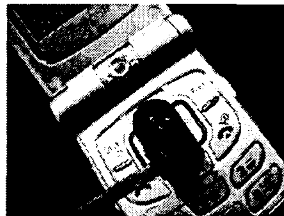




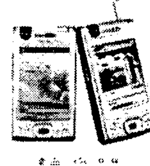
Application

Mobile Phone





PDA



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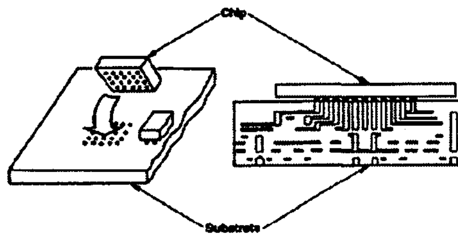
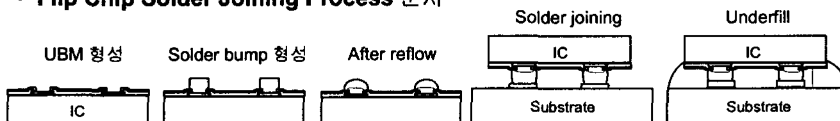
Flip Chip Solder Joining 공정

- IBM C4 (Controlled Collapse Chip Connection) Technology



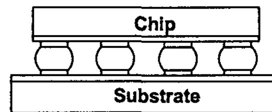
- Flip Chip Solder Joining Process 순서

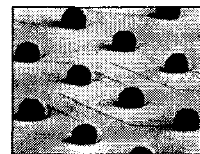


Solder Bump

- 기능
  - Chip과 Substrate 사이의 Electrical and Mechanical Connection
  - Chip으로부터의 Heat Dissipation Path
  - Chip과 기판사이에 공간을 만들어 전기적 접촉을 막음

- 재료
  - Eutectic Pb-Sn, Pb-Sn-Ag
  - High Pb-5～10 %Sn
  - Pb-In(50/50)
  - In
  - Pb-Free solders (Sn-Ag-Cu, Sn-Cu 등)





Pb-free Solders

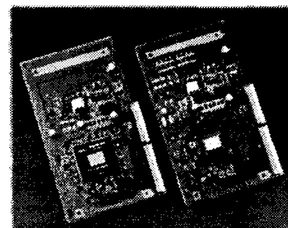
- **Commercial solder alloys for electronic applications**
  Sn-37Pb-(Ag)
  Pb-(5~10)Sn 등

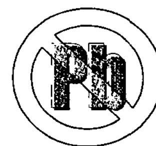
- **Pb free solder의 필요성**

  1. 법의 규제를 피하기 위해

  2. 환경보호

  3. 소비자의 요구에 의해





각국의 무연 솔더에 대한 활동

- **EC**

  WEEE (Waste from Electronic and Electrical Equipment) directive:
  recycling, recovery, reuse by product producers

  ROHS (Restriction of Hazardous substrates) directive:
  Ban on 4 heavy elements (Pb, Cd, Hg, hex Cr), PBB, and PBDE
  from Jul. 1, **2006** (a few exemption by **2010**)

- **Japan**

  상무성: Recycling law for electrical appliance 입안 **(2001)**

  JEIDA (Japan Electronic Industry Development Association) &
  JIEP (Japan Institute of Electronic Packaging): Pb-free roadmap 작성 (1998)

- **US**

  NEMI (National Electronics Manufacturing Initiative):
  Pb-free task force 결성 **(1999)**
  Goal : total Pb elimination by **2004**

Japanese Companies' Activities

- **Fujitsu: total abolition of leaded solder by 12/2002**
- **Matsushita Electric: total abolition of leaded solder by 03/2001**
  Green product 홍보
- **Seiko-Epson: total abolition of leaded solder including internally manufactured products by 03/2002**
- **Hitachi: total abolition of leaded solder by 03/2002**
- **NEC: 50% abolition of leaded solder by 03/2001**
- **Sony: application of unleaded solder to all products by 12/2001**

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US Patents on Pb-Free Solder (I)

	US Pat #	Assignees Sn	Sn (wt%)	Bi (wt%)	Ag	In	Sb	Cu	Zn	Others	Major Composit'n
7/88	4758407	Harris	87–93		0.1–0.5		4–6	3–5		Ni(1)	Sn Sb Cu
	4778733	Engelhard	92–99		0.05–3			0.7–6			Sn Cu Ag
	4806309	Willard	90–95	1–4	0.1–0.5		3–5				Sn Sb Bi
	5229070	Motorola	90	5		5					Sn Bi In
	5328660	IBM	78	10	2	10					Sn Bi In Ag
	5344607	IBM	90	2		8					Sn In Bi
	5393489	IBM	93	2	3		1	1			Sn Ag Bi Sb
	5411703	IBM	94	2			3	1			Sn Sb Bi Cu
	5368814	IBM	42	56		2					Bi Sn In
5/95	5414303	IBM	70–90	2–10		8–20					Sn In Bi
	5455004	Indium Co.	82–90	1–5		3–6			4–6		Sn In Ag Bi
	5580520	Indium Co.	71–92		2–4	4–26					Sn In Ag
	5410184	Motorola	92–97					3–8			Sn Cu
	5538686	Lucent	86			5			9		Sn Zn Ag
	5569433	Lucent	40–60	40–60	0.2–0.5						Sn Bi Ag
	5698160	Lucent	59–82		2–11				16–30		Sn Zn Ag
	5520572	US Army	86–97	0–5	0.3–4.5	0–9.3		0–5		Interm	SnAg BiInCu
	5527628	Iowa St. U	89		3.5–7.7			1–4			Sn Ag Cu
6/96	5658528	Mitsui	90	0.5–1.5	1–4	3–4					Sn In Ag Bi
	5718868	Mitsui	90	2–3				0.5	7–9		Sn In Ag Bi
	5733501	Toyota	65–95	0.1–9.5	0.8–5	0.1–9.5	0.1–10				SnSbBiInAg
	5730932	IBM	80	12	3	5					Sn BiIn Ag

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US Patents on Pb-Free Solder (II)

	US Pat #	Assignees Sn	Sn (wt%)	Bi (wt%)	Ag	In	Sb	Cu	Zn	Others	Major Composit'n
	5762866	Lucent	76–98	0.2–6	1–6	0.2–6			0.2–6		Sn Ag, BiInZn
10/98	5755896	Ford	37–57 48–58	37–57 40–50		6–10 2–5					Bi Sn In Sn Bi In
	5833921	Ford	43–58	38–52	1–2	2	5–15	1–4			SnBiSbCuIn
	5843371	Samsung	77–89	6–14	3–4	2–5					Sn Bi In Zn
2/99	5863493	Ford	91–97		2–5			0–3		Ni(0–3)	Sn AgCuNi
	5874043	IBM	70–74		6.5–7.5	12–24					Sn In Ag
	5938862	Delco	84–90		2.5–3.5	7–11		0.5–1.5			Sn In Ag Cu
	5993736	Mitsui	91–95	2–3	2–4				0.5–2		SnAgBiZn
12/00	5942185	Hitachi	72–87	10–23					3–5		SnBi Zn
	6077477	Matsushita	81–91	5–10	3–6	0.1–1.0		0.1–2			Sn Bi Ag Cu
91/01	6139979	Murtata	92–96				3–5	0.7–2		Ni(0.5)	Sn Sb Cu Ni
	6176947	H–Tech	bal	(0.5–5)	2.5–4.5	6–12	(0.5–2)	0.5–2.5			SnIn Ag Cu
	6179935	Fuji Elec	bal		0–4.0		(0–3.5)	0–2.0		Ni, Ge	Sn Ag Cu Ni
	6187114	Matsushita	bal					(0.1–5)	(Ni)	Pd(3.0)	SnPdCuNi
	6228322	Sony	bal	0.5–8.0	1.5–6.0			0.15–5	SmGd	La,Ce	Sn Bi Ag Cu
	6231691	Iowa St.U	bal		3.0–7.7			0.5–4	Fe(0.5)	Co(0.5)	SnAgCuFeCo
2/01	6253988	Antaya Tec	30	(0.25)	4.5	65	(0.75)	0.5			InSnAgCu
	6267823	Matsushita	bal	5–18	2–3.5	(0.1–1.5)		(<0.7)	(<10)		Sn Bi Zn Ag
	6296722	Nihon Supr	bal					0.1–2	(Ga<1)	Ni(<1)	SnCuNi(Ge)
	6319461	Nppon Gls	bal	(<10)	0.1–6		(<10)	0.1–6	0.1–3	AlTi	SnAgCuZnAl
	6325279	Matsushita	bal	5–10	3.0–6.0	0.1–1.0		0.1–2, 0			SnBiAgCuIn

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Pb-free solder candidates

- **Sn-Ag-Cu**

  Sn-(3.0-4.7 wt%)Ag-(0.5-1.7 wt%)Cu

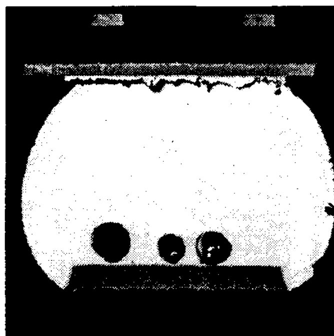
Sn-3.9Ag-0.6Cu: NEMI consortium (reflow soldering)
Sn-3.8Ag-0.7Cu: US commercial alloy/Europe IDEALS consortium
Sn-3.0Ag-0.5Cu: Japanese Comm / Consortia

- **Sn-Cu or Sn-Ag**

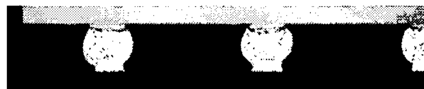
Sn-0.7Cu: NEMI Consortium (wave soldering)
Sn-3.5Ag

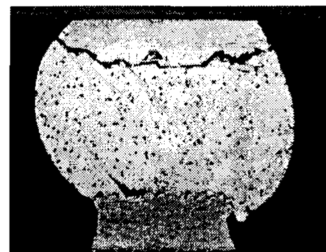
Thermomechanical Fatigue Behavior

Sn-Ag-Cu solder Joints



W. J. Lee (2003)





D. Frear (2002)