Pre-applied Underfill Technology

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Stencil Printed Wafer-Level Pre-applied Underfill Application

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Presentation Outline

- Wafer applied underfill process
- Coating underfill on bumped wafer
  1) material selection
  2) process optimization
  3) uniformity and consistency
- Voids entrapment and bump contamination by printing
- Assembly results and summary

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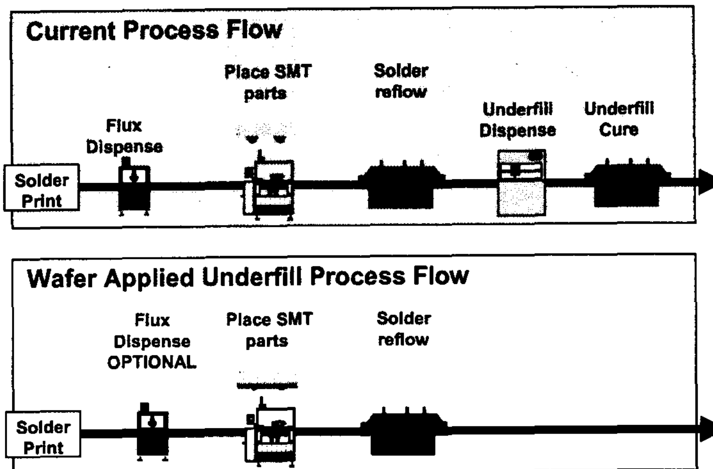
Underfill Processing for Flip Chips



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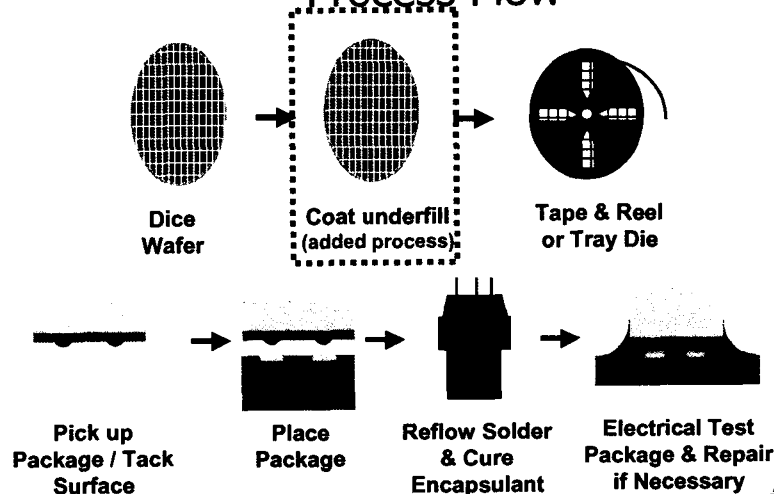
Wafer Applied Underfill Assembly Process Flow



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Coating Underfill on Bumped Wafer

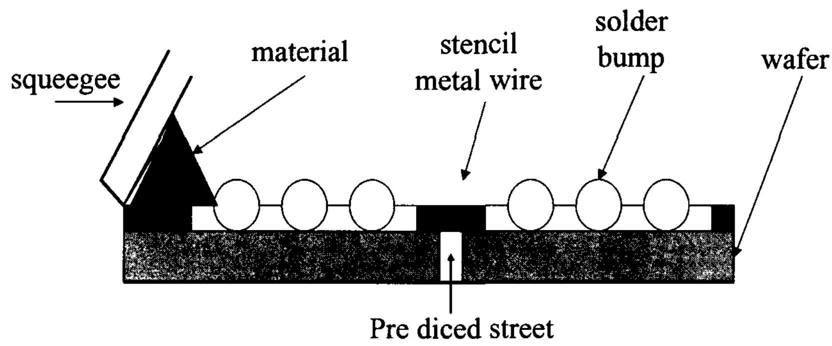
Underfill coating:
Several options have been explored.

Stencil printing selected:
Availability and familiarity in SMT industry.

Stencil Printing Setup

Screen Printer:
MPM/SPM semiautomatic screen printer
Wafer:
Five (5) inch FA10 full area array bumped wafer
Stencil:
Array of openings each for each individual die
Squeegee:
Polyurethane trailing edge with various hardness

Stencil Printing Process



An illustration of stencil printing process

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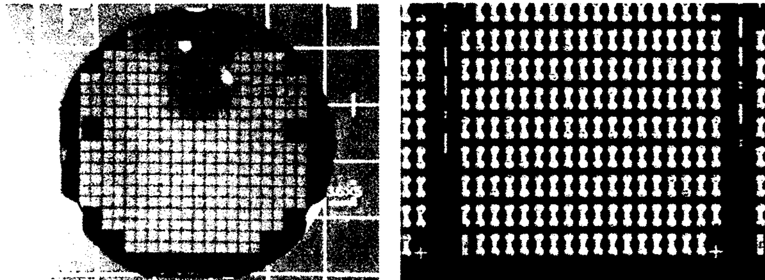
Diced FA10 Wafer, without coating



Whole wafer

Single chip

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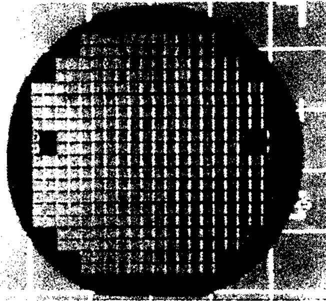
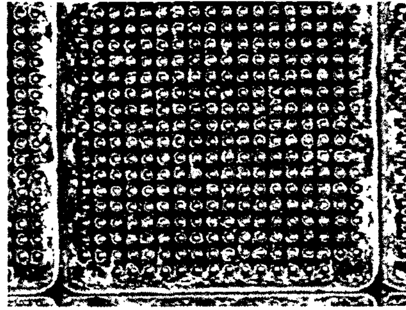
Diced FA10 Wafer, with coating



Whole wafer



Single chip

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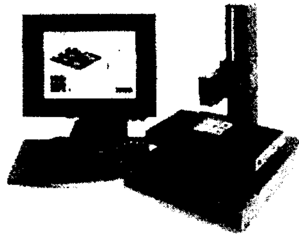
Coating Thickness Measurement



Solarius Viking non-contact laser profilometer

- X/Y 200 mm moving platform
- Camera for viewing the surface
- 600 um measuring range
- 0.1 um vertical resolution
- 2 um laser spot size

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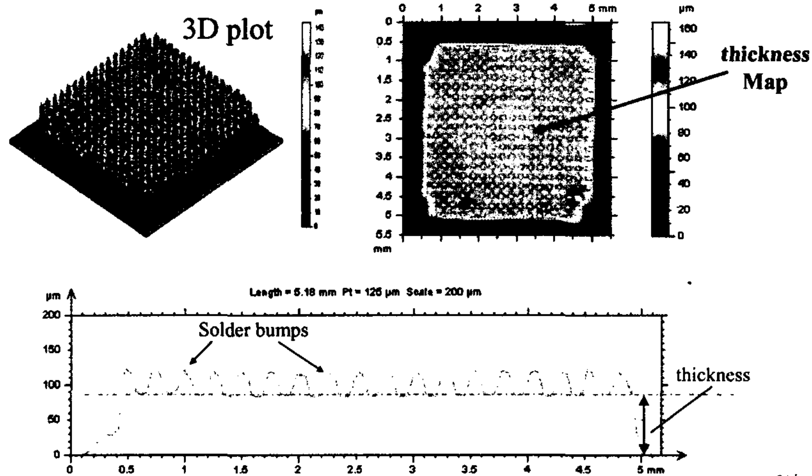
A scan example



Material development

All materials:

- Before B-stage:
  mixed with solvent for stencil printing
  viscosity varied by solvent content
  no-Newtonian shear thinning behavior
- After 110 C 2 hours B-stage
  solvent removed, tacky free
  60 wt% of silica fillers

Material	A	B	C	D	E
Viscosity (cps)	2000	5000	20000	50000	200000

Material Selection

- Five materials were printed under same process parameters.
- The coating was B-staged at 110 C for 2 hours before the thickness of each die was measured individually,

Material	Average coating thickness	Street cleanliness	Uniformity (Max. minus Min.)
A	78.5 um	worst	11.5 um
B	82.4 um	bad	12.4 um
C	87.6 um	good	14.8 um
D	101.3 um	good	20.5 um
E	132.8 um	bad	35.6 um

- Based on street cleanliness and uniformity, C was selected for the process development.

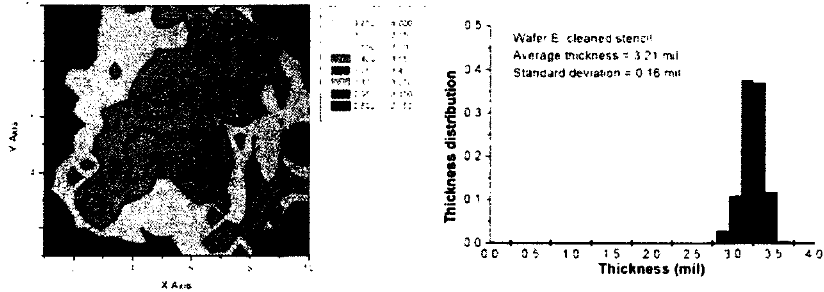
Squeegee selection

- Polyurethane squeegee selected to protect solder bump
- Squeegee hardness tested under same process parameters

Squeegee hardness	Average thickness (um)	Uniformity (um) Max minus min.
50	108.7	23.4
70	94.5	17.4
90	87.6	14.8
110	91.9	16.5
metal	102.5	11.4

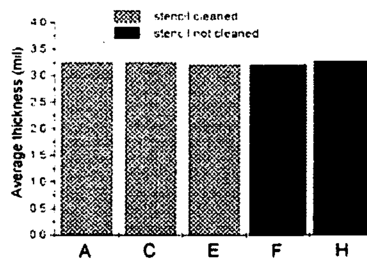
- By uniformity produced, hardness of shore A 90 was selected for wafer coating experiment.

Coating uniformity on a single wafer



- Coating on center tends to be thicker than around edges
- Variation of the coating thickness is about 0.6 mil (15 um)
- Standard deviation is within 5% of the average thickness

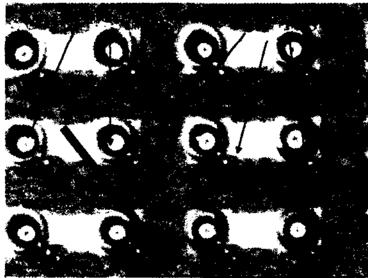
Coating consistency from wafer to wafer

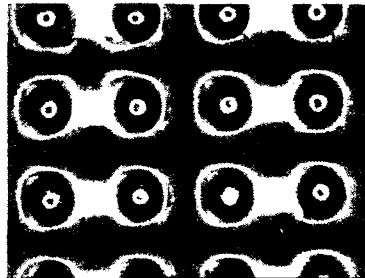


Wafer	Average Thickness (mil)	Standard Deviation (mil)
A	3.21	0.15
C	3.24	0.15
E	3.21	0.16
F	3.24	0.15
H	3.27	0.16

- Eight wafers were coated for the study. Among them, five were measured thickness distribution.
- A, B, C, D and E were coated with stencil cleaning.
- F, G and H were coated without stencil cleaning.

Printing voids


Before B-stage


After B-stage

- Voids are trapped behind solder bumps during stencil printing.
- Printed film is B-staged at 110 C for 2 hours
- Voids driven out from the coating during the B-stage.

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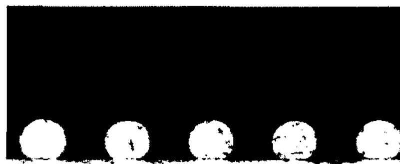
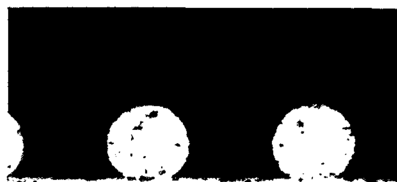
Solder bumps after coating B-staged





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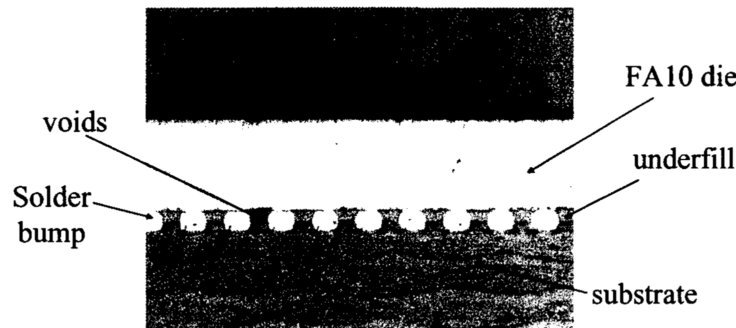
Assembly result

Flux directly applied on solder bumps

- Good solder wetting, Consistent 100% electrical yield
- Solder bumps are clean enough for good wetting !!

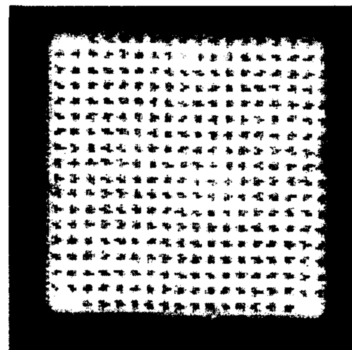


Assembly result

Flux directly applied on solder bumps

- Voids observed in assemblies

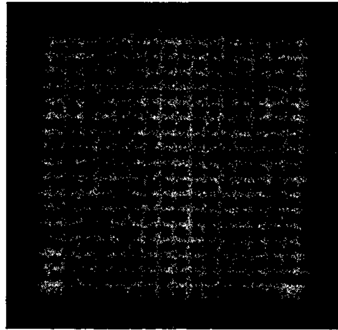
  flat coating causing placement voids



Assembly result

Flux dispensed on board

- 100% electrical yield
- no voids



Assembly result

Flux dispensed on board