

**Recent Progress in Pb-free Solders
and Soldering Technology:
Fundamentals, Reliability Issues
and Applications**

Sung Kwon Kang
(IBM/USA)

(ISMP 2004, Sept 2-3, Seoul, Korea)

Progress in Pb-Free Solders and Soldering Technology: Fundamentals, Reliability and Applications

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Recent Development

European Union passed two directives on 10/11/2002;

- **WEEE (Waste Electrical & Electronic Equip) for recycling, recovery, reuse by product producers**
- **RoHS (Restriction of Hazardous Substances), ban on 4 heavy elements (Pb, Cd, Hg, hex Cr) and brominated flame retardants (PBB and PBDE) from July 1st, 2006.
(a few exemptions by 2010)**
- **The WEEE and RoHS Directives became European law on 2/13/03, and member states now have to implement them by 8/13/2004.**

(9/04, SKK)

Intel to reduce lead-content in chips by 95%

NY Times, April 07, 2004

TOKYO - Intel Corp. said Wednesday (April 7) it would begin **reducing the lead content of its processors and chip sets by 95 percent later this year.**

Intel executives also indicated the company intends to label the reduced-lead microprocessors as "lead-free" **beginning with some microprocessors and chip sets in the third quarter.**

Intel is using new packages that use **lead-free solder balls.** The company said it is trying to find a reliable solution for the **tiny amount of lead still needed inside the processor packaging to connect the actual silicon "core" to the package.**

Intel shipped **millions of lead-free flash memory components in 2003.** Today's announcement is the next major step on the road to a lead-free product line for Intel's high volume CPU and chipset product line.

Selected Topics on Pb-Free Solders

Fundamentals

- Microstructure of Sn-Ag-Cu (tin dendrites, eutectic)
- Control of Ag₃Sn Plates
- Alloy Modification of SAC
- Properties of IMCs (nanoindentation)

Reliability Issues

- Thermal Fatigue Behaviors
- Impact Reliability
- IMC Growth, Spalling, Void Formation

Applications

- CBGA (ceramic ball grid array)
- CuCGA (copper column grid array)
- Wafer Bumping by IMS
- Pb-free Flip Chips

(9/04, SKK)

Fundamentals

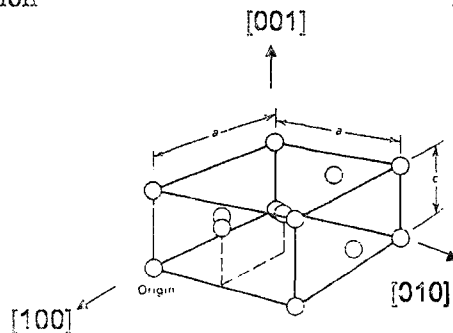
- **Microstructure of Sn-Ag-Cu**
- **Tin dendrite structure (CPL, EBSD)**
- **Control of Ag₃Sn Plate Formation**
- **Alloy Modifications (Ag, Cu, Zn, Ni, Fe, Co)**
- **Nano-indentation of IMC's**

(9/04, SKK)

β -Sn Dendrite Orientation Determination

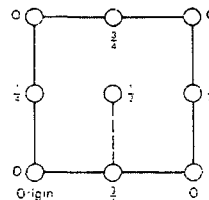
Electron Backscatter Diffraction (EBSD)

Direct Measurement of Crystallographic Orientation



Polarized Light Microscopy (PLM)

Qualitative Orientation Imaging Based on the Strongly Anisotropic Optical Properties of β -Sn



(D. Swenson, TMS 2004)

MichiganTech

Controlling Ag₃Sn Plate Formation in Near-Ternary Eutectic Sn-Ag-Cu Solders by Minor Zn Addition

**S. K. Kang, D. Y. Shih, D. Leonard, D. Henderson*,
T. Gosselin*, S.I. Cho+, J. Yu+, W.K. Choi++**

**IBM T.J. Watson Research Center, Yorktown Hts, NY,
* IBM Microelectronics, Endicott, NY 13760**

+ KAIST, Dept of Mat's Sci. & Eng, Daejon, Korea,

++Samsung Adv. Inst. of Tech, Suwon, Korea

Objectives

- **Three methods to control Ag₃Sn plate formation;**
 - 1) Providing high cooling rate (>2 C/s)**
 - 2) Modifying alloy composition (reduce Ag & Cu)**
 - 3) Reducing undercooling by minor alloying elements (Zn, Al, Sb, etc)**

(7/03, SKK)

Undercooling of SAC + Zn Alloys

- Heating at a rate of 1°C/min
- Cooling at a rate of 6°C/min after holding at 250°C for 10 min.

| Solder Composition (wt %) | Melting Temp. during Heating (T_1) | Peak Temp during Cooling (T_2) | $\Delta T(T_1 - T_2)$ |
|---------------------------|--|------------------------------------|-----------------------|
| Sn-3.8Ag-0.7Cu (SAC) | 217.0 | 187.2 | 29.8 |
| SAC + 0.1Zn | 217.7 | 213.3 | 4.4 |
| SAC + 0.7Zn | 217.2 | 213.6 | 3.6 |
| Sn-8Zn-3Bi | 193.7 | 191.8 | 1.9 |

Segregation and Coarsening Effects on Mechanical Properties in Aged Sn-Ag-Cu Solder Joints

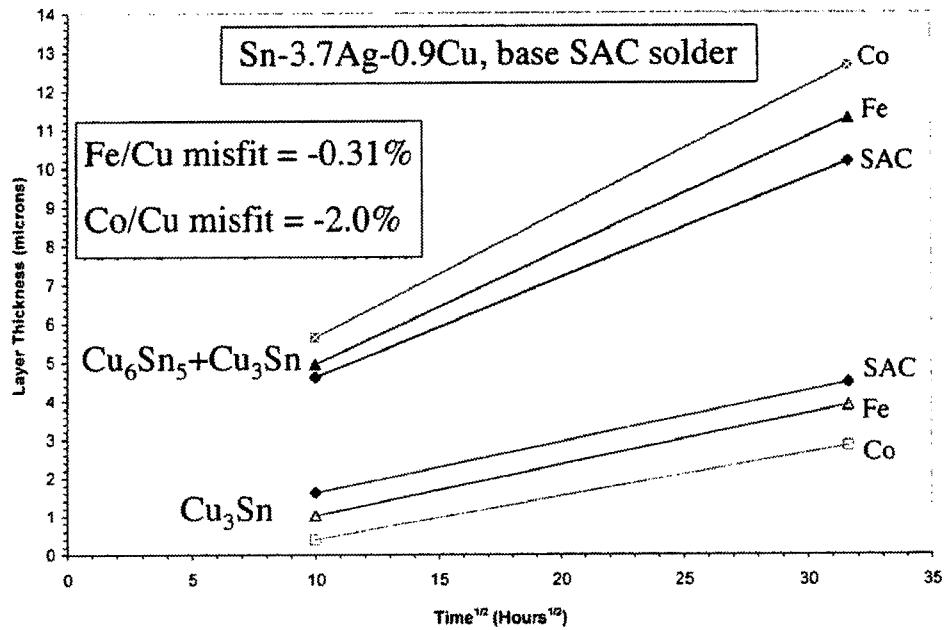


Iver E. Anderson, Joel L. Haringa, and Bruce A. Cook
Materials and Engineering Physics Program, Ames Laboratory (USDOE)
Iowa State University, Ames, Iowa 50011

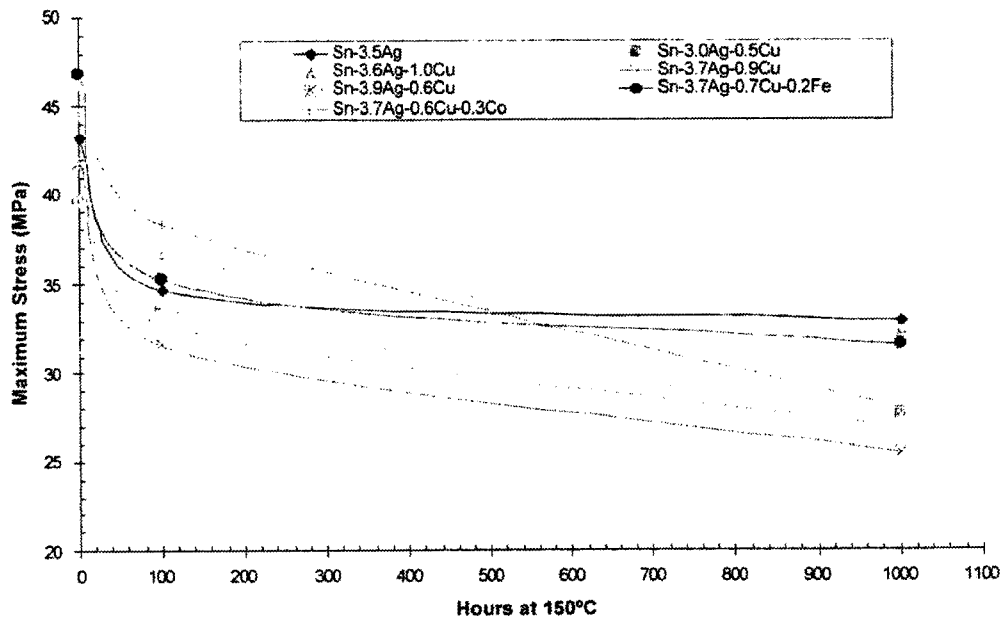
Invited talk at: Pb-Free Solders and Processing Issues Relevant to Microelectronic Packaging:
Mechanical Properties and Fatigue Behavior
Sponsored by TMS Electronic Packaging and Interconnection Materials
Committee of EMPMD
2004 TMS Annual Meeting
Charlotte, North Carolina
March 16, 2004

Supported by: Iowa State University Research Foundation and USDOE-BES (Materials Sciences) through contract no. W-7405-Eng-82.

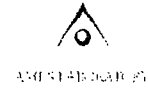
Substitutional Alloying Effect on Diffusion, Limited Growth of Intermetallic Layers



Maximum Shear Strength (at RT) from Asymmetric Four-Point Bend (AFPB) Test



Overall Conclusions



- ☞ All as-soldered and 100 h aged solder joints experienced ductile shear failure, either uniform (highest strength) or localized (typical, near Cu_6Sn_5 layer) shear in solder matrix.
- ☞ The main drop in shear strength (about 20%) occurs within the first 100 h of aging at 150°C , with an additional loss (about 16%) after 1,000 h of aging.
- ☞ After 1,000 h of aging, partial debonding of the $\text{Cu}_3\text{Sn}/\text{Cu}$ interface can occur in solder joints made with Sn-3.5Ag and SAC alloys, causing some embrittlement under shear.
- ☞ Only ductile failure was observed in all solder joints made from the Co- and Fe-modified SAC alloys after aging for 1,000 h.
- ☞ Modifying a strong (high Cu content) SAC solder alloy with a substitutional alloy addition for Cu seems effective for producing a solder joint that retains both strength and ductility after extreme (at least 1000 h) aging at high temperatures (up to 150°C).

Young's Moduli and Hardness of (Cu, Ag)-Sn Intermetallics

| | Cu | Sn-3.5Ag solder | Pure Sn | Ag_3Sn | Cu_6Sn_5 | Cu_3Sn |
|------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| Young's Modulus (GPa) | 117 ± 5 | 55 ± 2 | 47 ± 3 | 79 ± 4 | 112 ± 5 | 134 ± 7 |
| Hardness (GPa) | 1.7 ± 0.2 | 0.3 ± 0.1 | 0.2 ± 0.0 | 3.3 ± 0.2 | 6.4 ± 0.2 | 6.0 ± 0.2 |

Plastic properties of Cu, solder, Ag₃Sn, η phase, and ε phase

| Phase | | Yield Strength (MPa) | Work Hardening Exponent n |
|--------------------|----------|----------------------|------------------------------|
| Cu | | 180 ± 9 | 0.11 ± 0.003 |
| Solder | Sn-3.5Ag | 50 ± 2 | 0.077 ± 0.003 |
| | Pure Sn | 35 ± 0.4 | 0.049 ± 0.003 |
| Ag ₃ Sn | | 794 ± 92 | 0.072 ± 0.027 |
| η-Sn ₅ | | 2009 ± 63 | - |
| ε-Sn ₃ | | 1787 ± 108 | - |

Reliability Issues

- Thermal fatigue (Kang, ECTC 2004)
- IMC Spalling from Ni(P) (Sohn, ECTC2004)
- Kirkendall Void Formation (Chiu, ECTC2004)
- Impact reliability (Date, ECTC2004)
- Sn whiskers
- Sn pest
- Electromigration

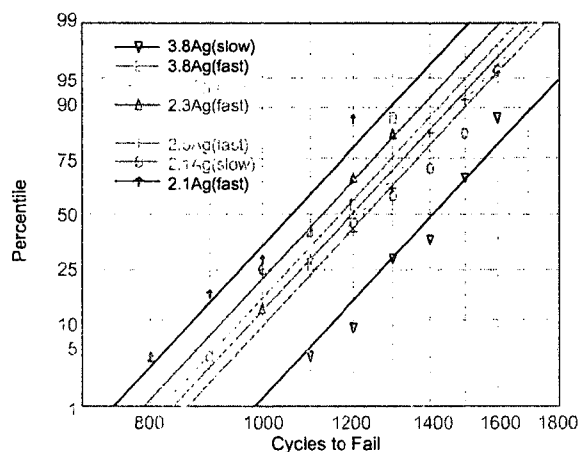
(9/04, SKK)

Thermal Fatigue Life of Sn-Ag-Cu BGA Joints

- SAC alloys with reduced Ag
 - Sn-3.8Ag-0.7Cu (control)
 - Sn-2.3Ag-0.4Cu-0.2Bi (optimized alloy)
 - Sn-2.7Ag-0.7Cu (intermediate Ag)
 - Sn-2.3Ag-0.9Cu (low Ag, w/o Bi)
- Test vehicles; ceramic modules on organic card
- Assembly cooling rates; 0.5 (slow) vs. 1.7 C/s (fast)
- ATC conditions
 - 0 to 100C; 30 min
 - 0 to 100C; 120 min
 - -40 to 125C; 42 min

(6/04, SKK)

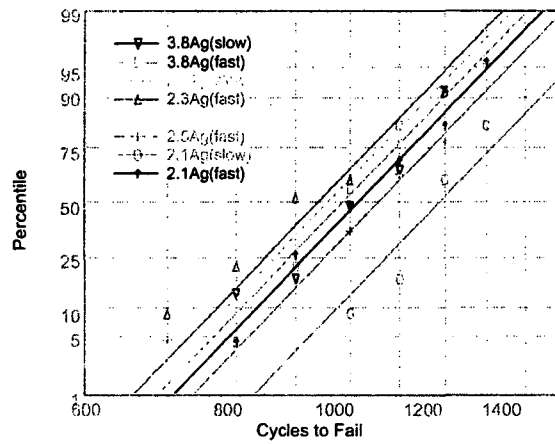
Failure Data for 0 C to 100 C (30 min Cycle Time)



Multiple Sample Lognormal Probability Plot
Global Common $\sigma = 0.153$

(Kang et al, Mat's Trans, JIM 2004)

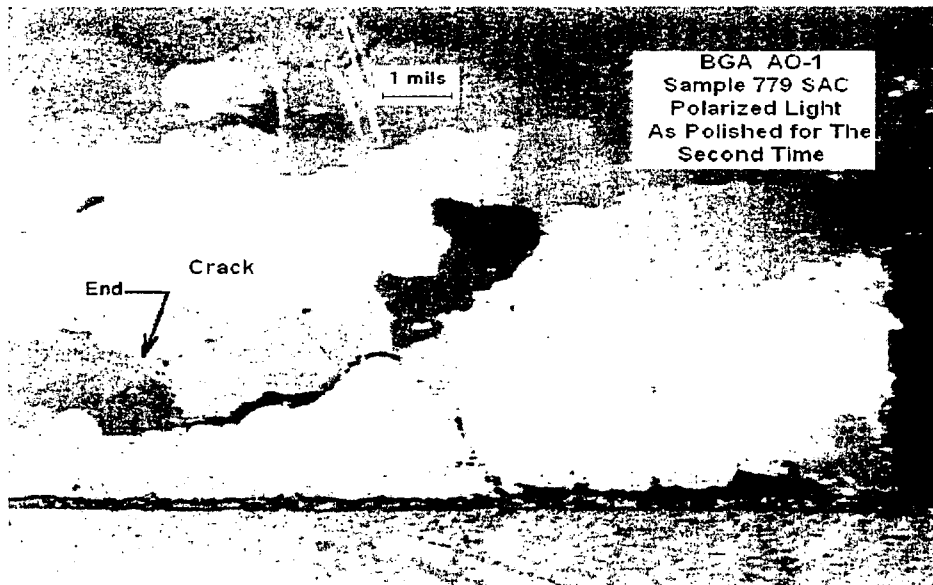
Failure Data for 0 C to 100 C (120 min Cycle Time)



Multiple Sample Lognormal Probability Plot
Global Common $\sigma = 0.153$

(Kang et al, Mat's Trans, JIM 2004)

Sn-3.8Ag-0.7Cu in CBGA (-40 to 125C, 761cyl)



(D. Henderson, TMS2004)

Fatigue Failure Mechanisms

- **Sn-Pb eutectic solder joints**
 - Coarsening of eutectic microstructure near the interface
 - Localized softening due to the coarsening
 - Fatigue crack propagation in the coarsened area
- **Sn-Ag-Cu solder joints**
 - Recrystallization of Sn matrix near the interface
 - Sn grain boundaries weakened by dislodging of fine intermetallic particles.
 - Fine grains more susceptible for creep deformation (grain boundary sliding or cracking)
 - Easy fatigue crack propagation in the recrystallized area

(6/04, SKK)

Summary

- Thermo-mechanical fatigue behavior of SAC joints was investigated in terms of Ag content, cooling rate, and ATC test condition.
- Sn-2.1Ag-0.9Cu joints (slow cooled) have the best life over high-Ag joints for 0-100C, 120 min ATC.
- Sn-3.8Ag-0.7Cu joints (slow cooled) have the best life over other joints for 0-100C, 30 min ATC.
- Slow cooling rate (0.5C/s) is more beneficial than fast cooling (1.7C/s) regardless of Ag content or ATC test.
- Fatigue life of low-Ag joints is less dependent on cooling rate in comparison to high-Ag joints.
- The crack propagation in low-Ag joints is more within the solder joint, while for high Ag joints it confines to the interface.
- The composition of SAC is recommended to be Ag < 2.7% to minimize the reliability risk factors.

(6/04, SKK)



Effect of Thermal Aging on Board Level Drop Reliability for Pb-free BGA Packages

Cheng Chiu, Kejun Zeng, Roger Stierman,
Darvin Edwards, Kazuaki Ano

Texas Instruments

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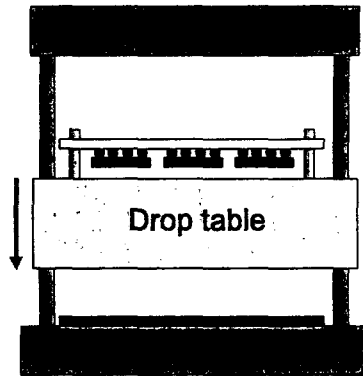
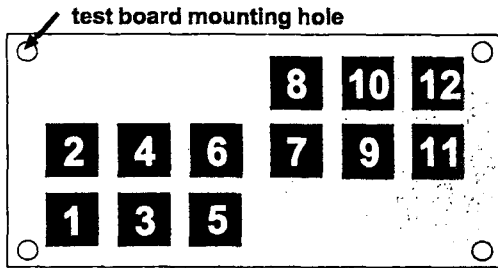
Introduction

- Drop induced interconnect failure is a major reliability concern for portable electronic applications
- Impact reliability is function of material characteristics and system level component layout
 - Layout and support for the PCB cause non-uniform stresses under impact
 - The impact loading leads to brittle intermetallic fracture at package to solder joint interface
- Bare Cu or OSP-Cu is considered as an alternative to electrolytic or electroless NiAu for BGA substrates or PCBs.
 - Without a barrier material, the diffusion of Cu and growth of IMC under aging is a reliability concern.

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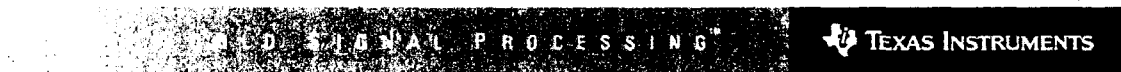


Drop test setup

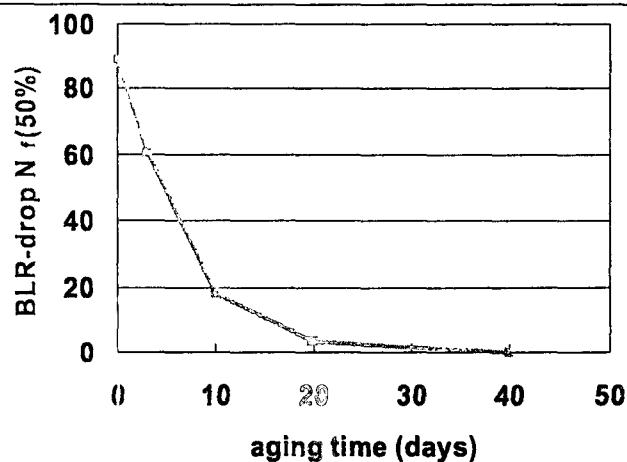


- **Test board:**
 - 12 plastic BGA packages with SnAgCu solder joints
 - Units were monitored in situ with event detector
 - only data from units 6 and 7 were analyzed
- **Impact condition:** 1ms triangular-shaped acceleration pulse with 1500g peak
- **Thermal aging:** 125°C for 3, 10, 20 and 40 days

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Effect of aging on BLR-drop



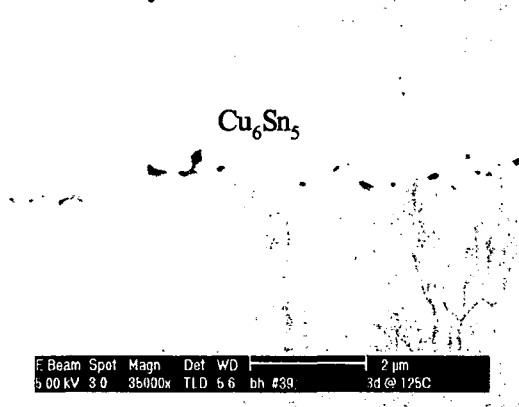
- Drop reliability degrades significantly after 125°C/10 days aging
- BLR-drop dependency on component location is not observed for the case of 40 days aging
 - All components failed within 2nd drop after 40 days aging

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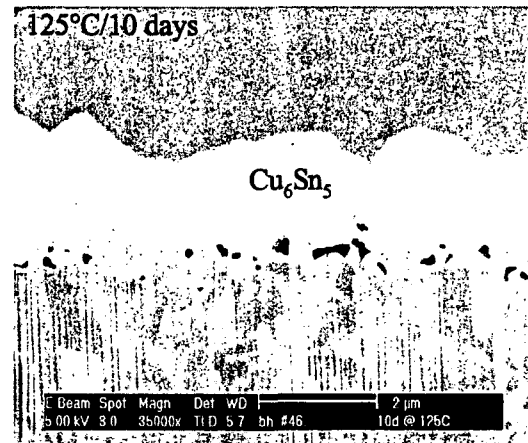


Cu/SnAgCu interface (125°C/3 & 10 days)

125°C/3 days



125°C/10 days



After 125°C/10 days, the largest voids were about 1 μm, indicated by the red arrow.

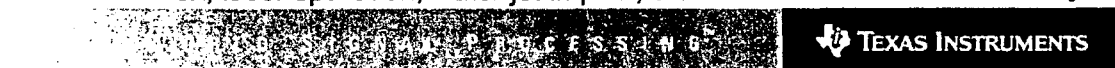
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Summary

- Very strong correlation between drop reliability and voiding for Cu/SnAgCu solder interface
 - Kirkendall voids at Cu/Cu₃Sn interface are detrimental to the drop reliability after aging
 - Similar trend is expected for temperature cycling reliability
 - Voiding process is activated at as low as 100°C
 - Bare Cu or OSP-Cu surface finish is not suitable for higher temperature applications
- Ball shear testing does not correlate to drop test performance. Ball pull strength is not a good indicator of shock reliability either
 - The only parameter correlating to BLR-drop was the percentage of bulk solder failure in ball pull testing
 - Alternative component level testing technique is needed
 - ex, laser spallation, water jet impact, etc

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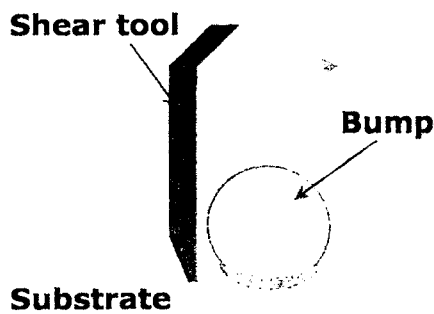
Reliability of Solder Joints

- Outline**
1. Introduction
 - Mechanical tests for BGA solder joints
 2. Sample preparation
 3. Results
 - Reliability of solder bumps on Cu
 - Reliability of solder bumps on Au/Ni(P)
 4. Summary

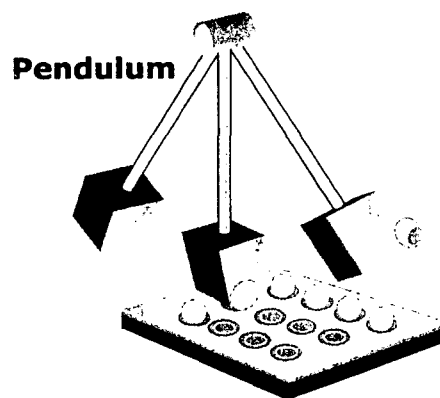
Masayoshi Date, King-Ning Tu
 Department of Materials Science and Engineering, UCLA
Tatsuya Shoji, Masaru Fujiyoshi, Koji Sato
 Hitachi Metals, Ltd.

Mechanical Tests for Solder Bumps

Conventional: Shear test

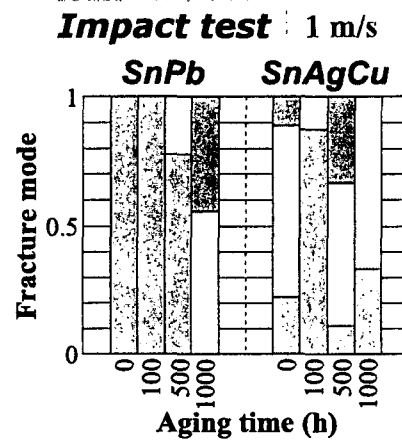
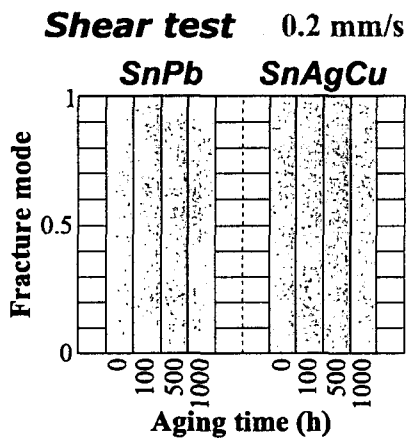
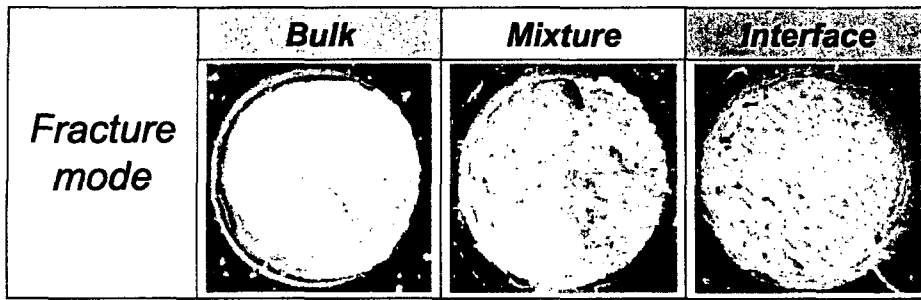


New technique: Impact test



(Morita et al., Hitachi Ltd.)

| Test method | Shear test | Impact test |
|----------------|-------------------|--------------------|
| Applied force | Shear | Shear |
| Test speed | 0.1 ~ 7 mm/s | 0.3 ~ 1.4 m/s |
| Measured value | Strength (N) | Toughness (J) |



Cross-sections: (1) Cu Pad

| | Sn-37Pb | Sn-3Ag-0.5Cu | Sn-8Zn-3Bi |
|--------------|---|---|--|
| As reflowed | | | |
| 150°C / 500h | | | |
| | <ul style="list-style-type: none"> - Cu-Sn IMCs (η', ϵ) - Growth of $\epsilon\text{Cu}_3\text{Sn}$ - Void formation | <ul style="list-style-type: none"> - Cu-Sn IMCs (η', ϵ) - Growth of Cu_3Sn - Void formation | <ul style="list-style-type: none"> - Cu-Zn IMC*s (ϵ, γ) - Fast growth of Cu_5Zn_8 - Void formation |

- The solder joints tended to fracture at the bond interface under impact loading.
- In the SnPb-on-Cu samples, the Pb-rich layer on top of Cu-Sn IMCs dominated the impact reliability.
- In the SnAgCu-on-Cu and SnZnBi-on-Cu samples, the degradation in impact reliability was caused by the growth of the interfacial compounds.
- The Ni plating was an effective method to suppress interfacial fracture in the SnPb and SnZnBi solder joints, but not in the SnAgCu.
- The reduction of Ag or Cu concentrations in the SnAgCu solder enabled us to extend the impact failure life.

**Spalling Behaviors of Intermetallic
Compounds during the Reaction between
Electroless Ni(P) and Lead-free Solders**

**The 54th Electronic Components and Technology Conference
June 2, 2004**

**Yoon-Chul Sohn, Jin Yu, Sung K. Kang*, Da-Yuan Shih*
and Taek-Yeong Lee****

Dept. of Mater. Sci. Eng., KAIST, Daejeon, Korea

***IBM T. J. Watson Research Center, NY, USA**

****Dept. of Mater. Eng., Hanbat National University, Daejeon, Korea**

Applications

- **CBGA (Farooq, ECTC2003)**
- **CuCGA (Interrante, Semicon2003)**
- **Flip Chips (Ebersberger, ECTC2004)**
- **Wafer Bumping by IMS (Gruber, ECTC2004)**

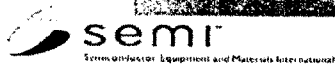
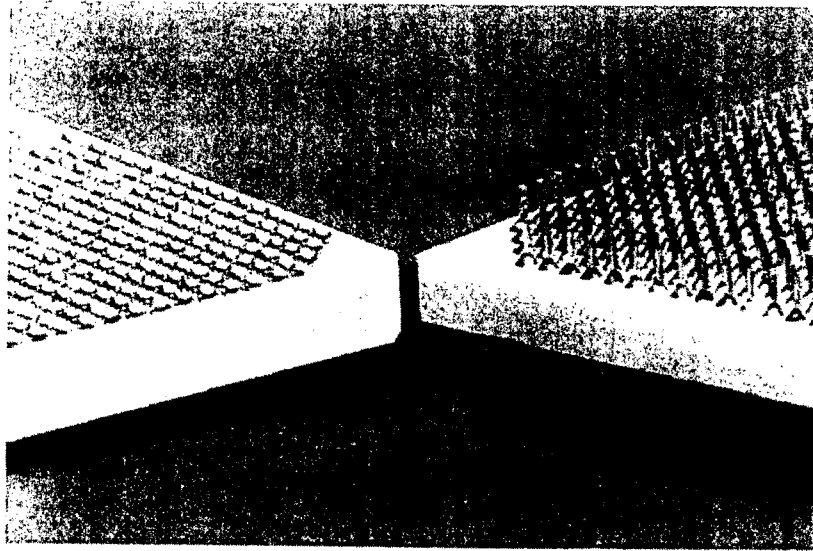
(9/04, SKK)

Lead-Free Package Interconnections for Ceramic Grid Arrays

Mario Interrante, Jeffrey Coffin, Marie Cole, Isabel De Sousa, Mukta Farooq, Lewis Goldmann, Charles Goldsmith, Janet Jozwiak, Tasha Lopez, Gregory Martin, Van Thanh Truong, David Welsh

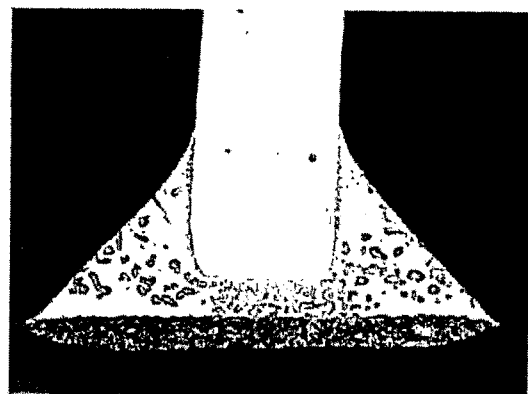
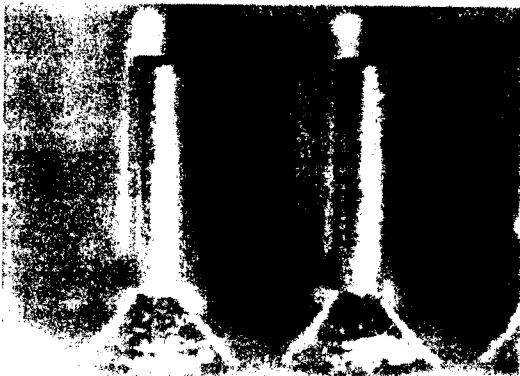
*IBM Microelectronics
East Fishkill, NY*

Lead-Free SAC CBGA and CuCGA



M. Cole, IBM Microelectronics - Slide 4

Lead-Free CCGA Interconnect



M. Cole, IBM Microelectronics - Slide 10

Conclusions

- **Lead-free second level interconnects developed for ceramic packages**
 - SAC CBGA
 - 1.0mm pitch packages exhibit higher reliability than SnPb CBGA
 - Fatigue resistant SAC solder
 - CuCGA
 - Lower inductance than 87 mil CLASP CCGA
 - Similar thermal fatigue life to CLASP CCGA
 - 2X thermal fatigue life of SAC CBGA



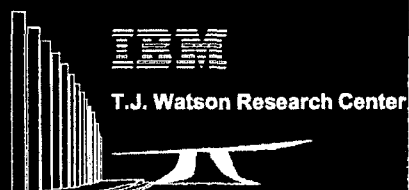
M. Cole, IBM Microelectronics - Slide 24

Injection Molded Soldering (IMS) Technology for Pb-free Wafer Bumping

*Peter Gruber, Da-Yuan Shih
IBM T.J. Watson Research Center*

*Luc Belanger, Guy Brouillette, David Danovitch, Valerie
Oberson, Michel Turgeon
IBM Canada, Microelectronics Division*

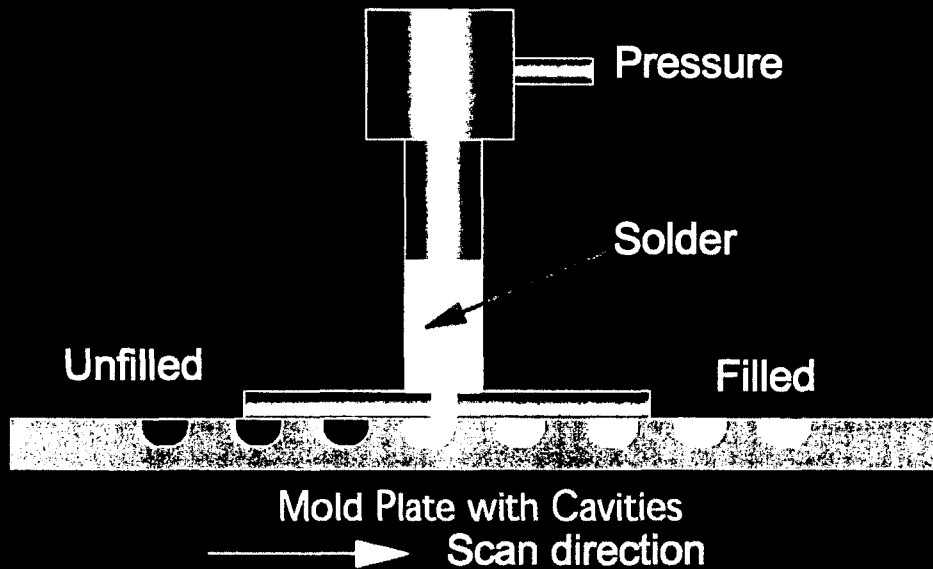
*Hideo Kimura
IBM Japan*



IMS Process Description

MOLD PLATE FILL

Side View



IMS Technology for Pb-free Wafer Bumping

ECTC 2004

IBM

IMS For Wafer Bumping

ADVANTAGES

- Simplicity - process similar to stencil printing; mold plates scan under fixed solder head
- No volume change - finer bump size & pitch possible than with paste
- Transfer process - inspect mold before transfer
- Low material cost - uses bulk alloy w/o converting to paste, pre-form, chemical solution
- Alloy independence - esp. beneficial for ternary & quaternary Pb-free alloys
- Efficient solder usage - environmental & economic benefits, esp. with costlier alloys

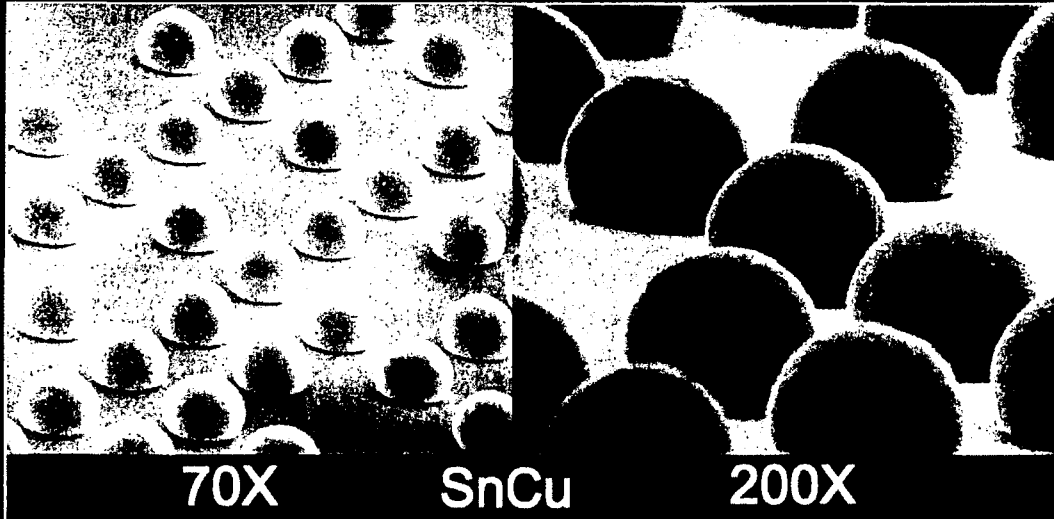
IMS Technology for Pb-free Wafer Bumping

ECTC 2004

IBM

IMS Process Description

Pb-free bumps after reflow



IMS Technology for Pb-free Wafer Bumping

ECTC 2004

IBM

Conclusions

- The convergence of flip chip growth, 300mm transition and Pb-free requirements provide an ideal opportunity for IMS, a new bumping technology that combines *"high-end capabilities with low-end process simplicity and cost"*.
- With recent enhancements, IMS has been extended to process Pb-free alloys for wafer bumping.
- Ordinary solder and transfer process afford IMS advantages in volume control, bump pitch, solder efficiency and alloy flexibility
- Preliminary feasibility evaluations suggest good manufacturability and robust chip interconnects

IMS Technology for Pb-free Wafer Bumping

ECTC 2004

IBM

Qualification of SnAg Solder Bumps for Lead-Free Flip Chip Applications



Bernd Ebersberger, *Platform Technologies*

Robert Bauer, *Reliability Methodology*

Lars Alexa, *Failure Analysis*

Bernd Ebersberger
Infineon Technologies AG

3rd June 2004

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Infineon Technologies AG, Munich, Germany
Corporate Logic

Conclusion

- SnAg *bump* reliability determined by IMC formation at high temperature and high current
- Flip chip *package* reliability (underfill) determines mechanical lifetime (temp. cycling, humidity)
- Good high temperature stability of SnAg bumps with thick Ni UBM
- Current carrying capability superior to eutectic SnPb bumps

Bernd Ebersberger
Infineon Technologies AG

3rd June 2004

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- Electroplated SnAg bumps are a viable solution for lead-free flip chip packaging
- Quality with respect to assembly requirements and reliability under harsh operating conditions are equal and partly superior to traditional eutectic SnPb bumps

Bernd Ebersberger
Infineon Technologies AG

3rd June 2004

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Summary

The implementation of Pb-free solder technology is making good progress in electronic industry.

Further understanding on fundamental issues on Pb-free solders/processes is required to reduce reliability risk factors of Pb-free solder joints.

Several reliability issues including thermal fatigue, impact reliability, IMC growth, spalling, void formation are reviewed for Pb-free solder joints.

Several applications of Pb-free technology are discussed, such as Pb-free, CBGA, CuCGA, flip chips, and wafer bumping by IMS.

(9/04, SKK)