Proceedings of International Conference on Astronomy and Space Science
Celebrating 20th Anniversary of Korea Space Science Society, Jeju, 2004

DESIGN AND IMPLEMENTATION OF TELEMETRY SYSTEM INTERFACE FOR KSLV-I

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(Received September 25, 2004; Accepted October 1, 2004)

ABSTRACT

KSLV (Korea Space Launch Vehicle)-I telemetry system will be composed of two telemetry streams: a lower stage telemetry stream and an upper stage telemetry stream. In this paper, the authors present design, implementation and test results of the upper stage telemetry interface for KSLV-I. The telemetry system currently is in the stage of the prototype model development, and its engineering model and flight model will be developed in the near future.

Keywords: telemetry interface, PCM, KSLV-I, MIL-STD-1553B, UART, verilog HDL, FPGA, telemetry processing

1. INTRODUCTION

The telemetry system of launch vehicle interfaces with all of the other onboard units directly or indirectly. Thus it is important for the telemetry system to be able to interface with those units regardless of various interface protocols employed onboard. The telemetry system, specifically telemetry processing unit, of KSLV-I collects data from three main resources: control system, remote telemetry units and payload (satellite). To accomodate all the necessary interfaces and to provide high reliability, design of new telemetry processing unit had been required.

A UART (Universal Asynchronous Receiver Transmitter) is designed and implemented in the telemetry processing unit with an FPGA to interface with payload telemetry system. As a main telemetry bus between telemetry processing unit and control system, MIL-STD-1553B data bus is employed in the telemetry processing unit. The telemetry processing unit transmits the telemetry data to the ground system through PCM (Pulse Code Modulation) generator which is implemented by an FPGA with a double-buffered memory. In the following, design and implementation of telemetry processing unit are presented in detail.

2. DESIGN OF THE TELEMETRY SYSTEM INTERFACE FOR KSLV-I

Telemetry processing unit collects telemetry data from other onboard units in launch vehicle MIL-STD-1553B link. The unit includes two MIL-STD-1553B communication chains. Chain #1

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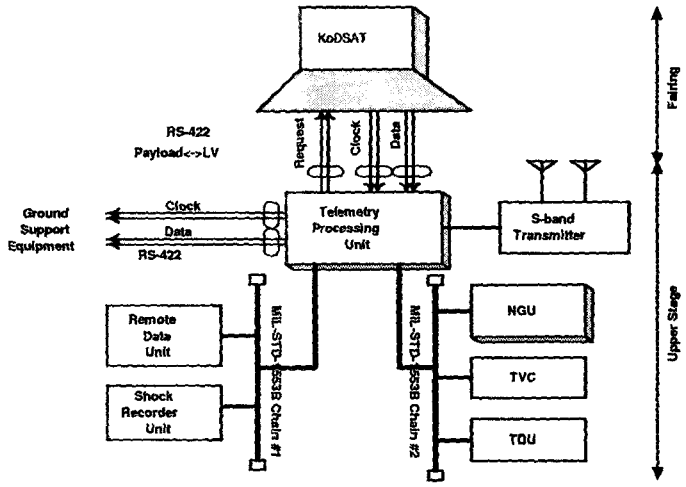

Figure 1. Interface diagram of KSLV-I upper stage telemetry system.

interfaces with remote data unit(s) and one pyro-shock unit, while chain #2 interfaces with onboard control units. The telemetry processing unit collects payload (KoDSat: Korea Demonstration Satellite) telemetry data via RS-422 serial link. The telemetry processing unit then also formats PCM telemetry data and transmits the formatted data to the ground support system via RS-422 link and to the S-band transmitter. Figure 1 shows interface diagram of the upper stage telemetry system in KSLV-I (Kim et al. 2003a,b).

3. IMPLEMENTATION OF TELEMETRY SYSTEM INTERFACE- MIL-STD

-1553B interface

The telemetry processing unit operates as a BC (Bus Controller) to collect environmental telemetry data from RTs (Remote Terminal). The unit controls bus traffic by issuing dedicated commands to RTs to send the measured data. Upon receiving the command, the RT responds by transmitting the telemetry data to the bus controller.

The telemetry processing unit operates as an RT to receive control system telemetry data. These control system telemetry data are then embedded into PCM stream with asynchronous data which is partitioned into two fields : frame information and data.

- Payload Interface

In order to process satellite telemetry data, a UART is implemented and employed in the processing unit. After power on reset, the UART sends the request command to DAU (Data Acquisition Unit) located in the KoDSat. Upon receiving the request of data, the DAU transmits the satellite telemetry data 36words-consecutively via RS-422 serial link. The UART waits until the frame header word is detected by the correlator. Once detected the frame header word, the UART stores the serial data in the asynchronous RAM embedded in the FPGA. Data transfer execution in this design is synchronized by frame formatter, which occurs every two minor frames (2.5 ms). The UART is coded by Verilog HDL (Hardware Description Language) on a Xilinx FPGA QPRO XC4013. Figure 2 shows the architecture of the UART and interface with PCM frame formatter (Kim et al. 2003b).

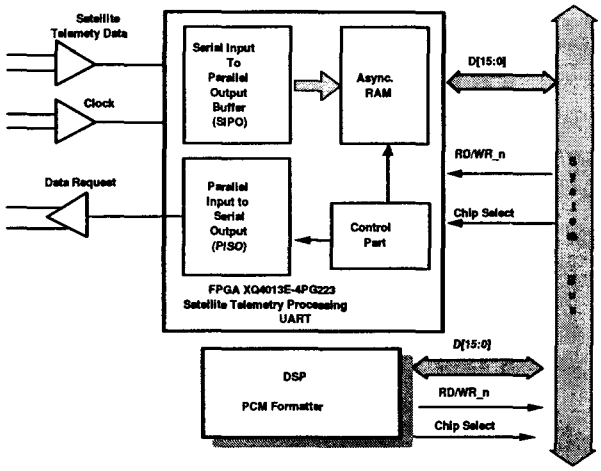

Figure 2. UART (payload data processing) interface diagram.

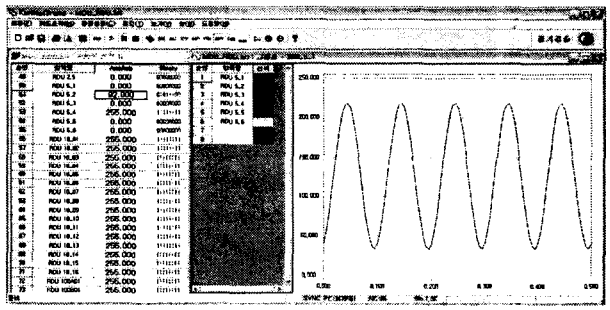

Figure 3. Test result of telemetry processing unit and remote data unit with MIL-STD-1553B.

- PCM generator interface

PCM generator makes use of a double buffered memory. After PCM data is written into one bank, the PCM generator reads the other bank data. When one bank of the double buffered memory is empty, the PCM generator produces an interrupt signal to PCM formatter to write PCM data to the other memory bank. Frame formatting processor formats PCM frame with the stored data using the frame format program. The formatted PCM data is stored in the queue memory. The PCM generator is implemented on a Xilinx QPRO XC4005 FPGA.

- Telemetry system test

To validate the interface design, interface tests for each interface protocol are performed, between telemetry processing unit and other systems (KoDSat DAU, remote data unit and telemetry test equipment). Figure 3, which is captured by test equipment, shows the test result of MIL-STD-1553B, remote data unit, telemetry processing unit and telemetry test equipment. As shown in the figure, remote data unit acquires and converts input data (10Hz sine wave) into telemetry data. The telemetry processing unit gathers the telemetry data with 200 messages per second via MIL-STD-1553B and outputs PCM data to test equipment in real time.

4. CONCLUSIONS

The objective of interface development for telemetry processing unit is to provide interface functions with other units or resources. The telemetry processing unit, which controls all of the upper stage telemetry, has been implemented with a UART for payload telemetry, MIL-STD-1553B two chains for remote telemetry data as well as control system telemetry, and double-buffered memory for telemetry generator module. These modules are implemented by Verilog HDL to support compatibility. The result of this paper will be utilized for the successful development of the telemetry system for KSLV-I upper stage, through the further development.

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