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EFFICIENT THERMAL MODELING IN DEVELOPMENT OF A SPACEBORNE ELECTRONIC EQUIPMENT

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ABSTRACT

The initial thermal analysis needs to be fast and efficient to reduce the feedback time for the optimal electronic equipment designing. In this study, a thermal model is developed by using power consumption measurement values of each functional breadboard, that is, semi-empirical power dissipation method. In modeling heat dissipated EEE parts, power dissipation is imposed evenly on the EEE part footprint area which is projected to the printed circuit board, and is called surface heat model. The application of these methods is performed in the development of a command and telemetry unit (CTU) for a geostationary satellite. Finally, the thermal cycling test is performed to verify the applied thermal analysis methods.

Keywords: thermal analysis, thermal design, electronic equipment, geostationary satellite

1. INTRODUCTION

A key factor of a spaceborne electronic equipment design is the efficient circuit designing followed by considering the adequate status on current, voltage and temperature with operational margin, that is, derating requirements. Especially, the temperature of a EEE part should be considered to keep the performance specification and high reliability of the EEE part in the space environments since the initial design phase of the equipment. In this paper, the fast and reliable thermal analysis methods are presented on the initial design phase of spaceborne electronic equipment. The application of these methods is performed in the development of a command and telemetry unit (CTU) for a geostationary satellite.

2. EQUIPMENT THERMAL MODELING AND TEST RESULTS

CTU is composed of two of the electrical power converter (EPC) boards and six of digital boards (command, telemetry, and uplink board with three of their redundancy) and shown in Figure 1. Thermal design philosophy of CTU shows that the thermal path segregation between the EPC board and digital boards to not influence to each other. EPC boards are mounted on the page frame and support frame to transfer heat from the EEE parts toward the CTU baseplate. Six digital boards utilize the PCB retainer for heat transfer toward the CTU sidewall housing. CTU housing and PCBs are

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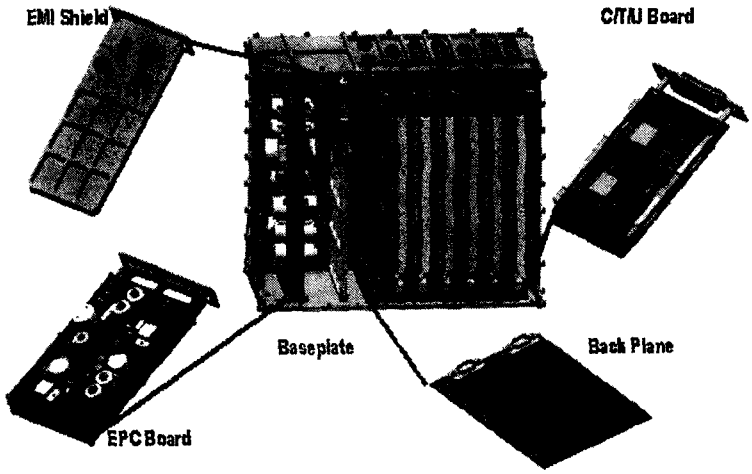


Figure 1. Command and telemetry unit (CTU) assembly.

Table 1. Power dissipation and power consumption data of functional boards.

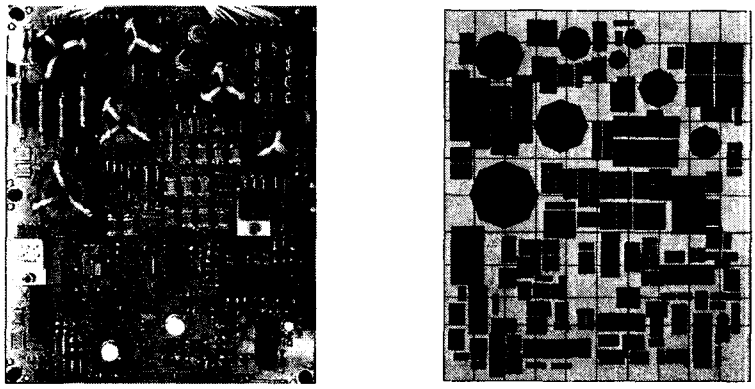
Functional board name	Maximum predicted Power dissipation $(W, \Sigma Q_{max,i,board})$	Experimental power consumption (W, P_{board})	Weighting factor $\left\{ \frac{(1-\eta)\, P_{board}}{\sum Q_{max,i,board}} \right\}$
Command	3.22	0.744	0.231
Telemetry	2.38	1.3	0.544
Uplink-1553B	5.75	3.675	0.64
EPC	7.96	6.755	0.85

modeled by the thermal plate modeling which is the heat transfer through the thickness direction is ignored. The effective thermal conductivity of PCB is modeled by using the relation data between the copper coverage of the PCB layers and thermal resistance per square (Kraus & Bar-Cohen 1983). The power dissipation is most important input parameter in the thermal analysis. The thermal analysis results and verification of the thermal design are resulted directly from the accuracy of power dissipation data. The maximum power dissipation is readily calculated by hand from the electrical designed circuit schematics. Generally, the maximum power dissipation is far from the actual dissipation. In this study, the breadboard power consumption measurement value is multiplied to the theoretical maximum power dissipation value (that is why semi-empirical method) of each EEE part as a weighting factor shown in eq. (1). Table 1 shows resulted weighting factor of CTU functional board.

$$Q_i = Q_{max,i} \left\{ \frac{(1-\eta)\, P_{board}}{\sum Q_{max,i,board}} \right\} \tag{1}$$

where Q_i is the weighted power dissipation value of i part, $Q_{max,i}$ is the theoretical maximum power dissipation of i part, P_{board} is the power consumption value of each breadboard, and η(=0 for the thermally worst case) is the efficiency of the breadboard.

In the previous studies (Park & Chang 2002), thermal modeling of the each EEE part is established by using a lumped capacity node for a heat dissipated part having difficulty and time-consuming in physical assigning and synchronizing the PCB meshes or nodes. Importing the EEE



(a) Real layout (b) Surface heat model

Figure 2. Surface heat model of CTU EPC board.

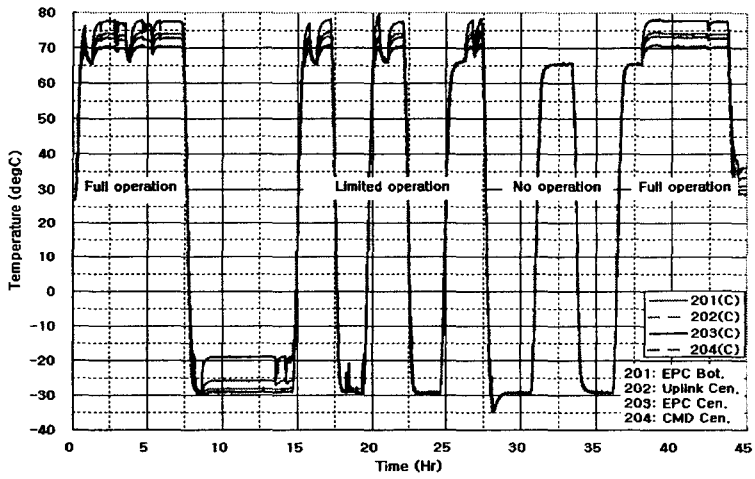


Figure 3. CTU temperature profile in thermal cycling test.

part footprint in the form of convenient computational files from the electrical parts arrangement software, a EEE part is divided by four or more detailed capacity node and added by surface heat for that part footprint. The area-weighted heat transfer from the EEE part to the adjacent PCB meshes or nodes is calculated by using the thermal analysis software such as SINDA (System Improved Numerical Difference Analyzer), TAS (Thermal Analysis System). The surface heat model of CTU EPC board is shown in Figure 2.

The thermal cycling test is performed for the purpose of the verification on the developed thermal model. The several points of temperature profile having six cycles is shown in Figure 3, and the results of thermal analysis and test for hot plateau condition is listed in Table 2. The location of measurement in the test is determined as the hottest and coldest zone in the thermal analysis results (hot/cold zone of all PCB is located in the center/bottom area of PCB respectively). Table 2 shows that the developed thermal model of CTU closely simulates and agrees well with the test results

Table 2. Results of analysis and test for hot plateau case.

Component	Position	Analysis (°C)	Test (°C)
Top housing	-	68	67
Bottom	-	67	67
Side wall (left)	-	68	68
Side wall (right)	-	68	68
Front housing	-	67	67
Baseplate	-	66	67
EPC board	Center	79	78
	Bottom	72	74
Command board	Center	71	71
	Bottom	69	70
Telemetry board	Center	72	72
	Bottom	71	71
Uplink-1553B board	Center	77	75
	Bottom	71	72
Backplane	Rear	N/A	69
	Front	N/A	69

using semi-empirical power dissipation method and surface heat modeling.

3. CONCLUSIONS

A thermal model is developed by using semi-empirical power dissipation method and surface heat model of the EEE part footprint to accomplish the fast and efficient thermal design of spaceborne electronic equipment. Developed thermal models are applied to analyze the thermal behavior of CTU for a geostationary satellite equipment. Thermal analysis results of CTU agree well with the thermal responses of thermal cycling test.

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