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IO BOARD DESIGN OF NEXT GENERATION SATELLITE USING THE SPACE WIRE INTERFACE

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ABSTRACT

This paper presents a feasibility study of an advanced IO board design for the next generation of low-earth orbit satellites. Advanced IO board design includes sensor interface, A/D, D/A, Digital Module, Serial Module etc, and allows to process increasing data rates between IO board and CPU board. The higher data rate involved in modern IO board additionally introduce issues such as noise, fault tolerance, command and data handling, limited pin count and power consumption problems. The experience in KOMPSAT-1 and 2 program with this kind of problems resulted in using SMCS chip set, a high speed serial link technology based on IEEE-1355 (Space Wire Protocol) (ESA-ESTEC 2003, Parkes 1999), as a standard for next generation of satellite IO board design.

Keywords: IO board, spacewire, IEEE-1355, SMCS chipset

1. INTRODUCTION

In order to connect IO board to CPU board using the serial link, a communication controller is necessary. This one is responsible for the data transfer between the CPU and IO. The SMCS332 and the SMCS116 (Christen 1999, 2001) are communication controllers for the connection to an IEEE-1355 link (Stephan et al. 2004). For next satellite generation, we investigated the SMCS chipset functions and characteristics and performed a communication mode trade-off study. A general description of the SMCS chip set is provided in chapter2. The result of a SMCS chipset communication mode trade off study is presented in chapter 3. IO board conceptual design and communication protocol are presented in chapter 4. The fifth chapter contains the conclusion and summarizes the purpose of this paper.

2. DESCRIPTION OF THE SMCS332/SMCS116

2.1 SMCS332 Description

The SMCS332 provides three IEEE-1355 links with up to 200Mbit/s data transmit rate. Each parallel interface of the device can be configured to 8, 16, 32 bits. Furthermore a checksum can be

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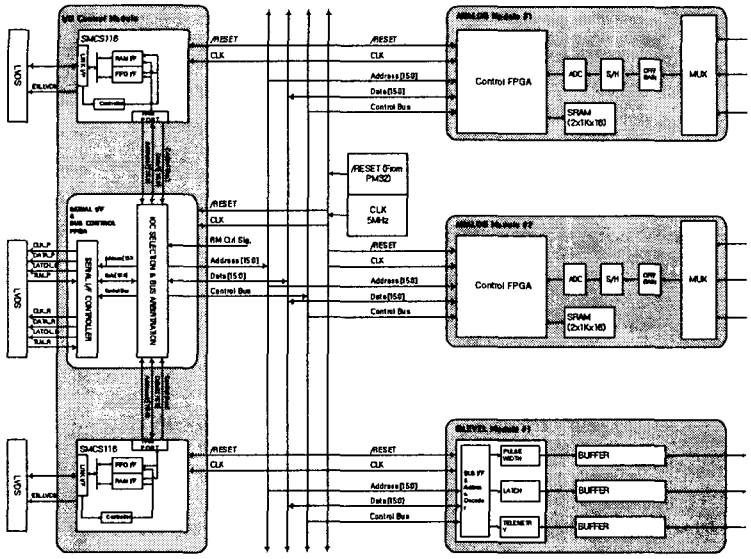

Figure 1. IO Board and CPU Board Detailed Design.

generated or checked at packet level. Each channel consists of a DS (Data Strobe) macro cell, a receive section, a transmit section, and a protocol processing unit. In order to perform autonomous accesses to the communication memory a COMI (Communication Memory Interface) exists. The HOCI (Host Control Interface) provides read and write access to the configuration registers and the DS channels for the CPU. The PRCI (Protocol Command Interface) collects commands from the protocol units. Furthermore, the SMCS332 comprises a JTAG test interface.

2.2 SMCS116 Description

The SMCS116 or SMCSlite comprises only one IEEE-1355 link with up to 200Mbit/s data transmit rate. The device was developed for nodes which need a small communication controller to manage the communication to the IEEE-1355 link. Several applications do not need the three links of the SMCS332 and therefore the smaller SMCS116 was designed, It's parallel interface can be configured to 8 or 16 bits and a checksum can be generated or checked at packet level.

A special functionality of the SMCS116 is that this device allows an easy data transfer between an ADC or a DAC and the IEEE-1355 link. This is managed by the ADC I/F and the DAC I/F whereby the interfaces allow the read (write) from an AD (DA) Converter. Furthermore, with the RAM I/F four different banks of memory are addressable. The FIFO I/F provides control signals like full, empty, read or write. Additionally, the SMCS116 comprises a General Purpose Interface (GPIO), two independent UARTs and a JATG test interface.

3. SMCS COMMUNICATION MODE TRADE OFF STUDY

SMCS chipset provides 2 different communications mode; one is the transparent mode the other is the simple protocol mode. Table 1 shows the advantages and disadvantages of each mode.

The simple protocol mode just controls the SCMS internal registers and uses only the SMCS internal functions, ADC, DAC, and RAM interfaces. This mode does not control the 1355 low level

Table 1. SMCS Communication Mode.

		SIMPLE PROTOCOL MODE	TRANSPARENT MODE
H/W	Advantage	- Same Architecture regardless Protocol Mode	
		- Used SMCS116 Internal Function	
		- Reduce Board design time	
		- Used RAM I/F (No limitation of I/O Number)	
	Disadvantage	- Set many registers	- Require I/O Control FPGA for
		- Packet Size Limited (SMCSlite FIFO SizeLimit)	protocol decoding - Require SRAM for COMI
		- After Reset, SMCSLite must be initialized by Link	- Do not use SMCSlite internal function - Require time to controller debugging
S/W	Advantage	- Reduce time to I/O Telemetry Acquisition	
		- Multiple Data Read/Write	
	Disadvantage	- Transmit packet by packet (CPU Overhead)	- Take more time to I/O Telemetry Acquisition
		- Low Level setting required	- Low Level setting required

protocol. It has several advantages. The design of the IO controller is simpler and it is easier to increase the IO board number in case of channel extension. However, the control of the internal registers might cause some difficulties.

The transparent mode supports user defined packet design, various protocols and it's mode doesn't restrict the packet size. Since the IO controller requires for this mode a protocol decoding logic the controller design is more complicated and requires more effort.

A communication mode trade off study recently performed concludes that the simple protocol mode should be the design baseline for the IO controller of the next satellite.

4. IO BOARD DESIGN AND COMMUNICATION PROTOCOL

The IO board design uses the SMCS chip with the SMCS332 as master in the CPU board and the SMCS116 as slave in the IO Control board. The IO controller board uses the SMCS116 Chip and FPGA for target IO Control. Figure 1 shows the overall IO board design using the RAM interface method.

For emergency and safety reasons, each of the 2 CPU boards, primary & redundant board, has the SMCS332 as SpaceWire controller. One 332chip can connect 3 links. The IO board consists of an analog, a digital Bilevel and a serial board. The analog board and the serial board are equipped with an IO Control FPGA for data acquisition and contain a serial interface for data transfer between RAM block and target IO. Table 2 shows the communication protocol between SMCS332 & 116. It is divided into address area & data area.

The address area contains information about board number and target IO address. It is decoded in control FPGA in each IO board. Each IO board has a maximum of 32768 Target IO's because the address consists of 15 bits.

The data area contains the actual data command. A digital command is directly transmitted to the target IO. An analog IO command is firstly sent to the IO control FPGA, decoded and then sent to the target IO.

5. CONCLUSIONS

This paper shows the IO conceptual design for the next generation of satellites. A serial inter-

Table 2. Communication Protocol for IO control.

COM/TLM	Port Address	Description 1	Description 2	Address[15:0]	Data[15:0]
0/1	0x43	Analog B'D	Setting Register	0x0000 ~ 0x001F	Setting Value
0/1	0x43	Analog B'D	GAIN/OFFSET	0x0020 ~ 0x0FFF	GAIN/OFFSET
0/1	0x43	Analog B'D	ADC VALUE	0x1000 ~ 0x1FFF	ADC Value
0/1	0x43	Serial I/F B'D	Command	0x2000 ~ 0x2FFF	Command
0/1	0x43	Serial I/F B'D	Telemetry	0x2000 ~ 0x2FFF	Telemetry
0/1	0x43	Bilevel B'D	Latch	0x3000 ~ 0x30FF	16Bit Latch Type
0/1	0x43	Bilevel B'D	Pulse	0x3100 ~ 0x31FF	Pulse Width Value/Type
0/1	0x43	Bilevel B'D	Status	0x3200 ~ 0x32FF	Bilevel Telemetry Request Command

face, the Space Wire IEEE-1355 protocol developed by ESA for space application, is basically used for communication between CPU board & Target IO board. This protocol, already space qualified and implemented in several space programs, fully supports high speed communications, the design is fault tolerant and RH hard space parts are implemented.

The next SMCS chip set is currently under development and may be available by end of this year (Stephan et al. 2004). It is also planned to finalize the conceptual board design and to develop the actual IO board. The final diagram and test result are supposed to be provided end of this year. In our opinion, Space Wire communication has many advantages, but bears also some risk, because it is the first time that this new technology will be used in Korea. If the development is successfully finished, the next satellite generation will benefit from this. Furthermore, we are going to start our own protocol developing and communication method.

REFERENCES

Christen, A. Z. 1999, SMCS332 User Manual, Issue 2,
http://www.atmel.com/dyn/products/devices.asp?family_id=641#787

Christen, A. Z. 2001, SMCSlite User Manual, Issue 1.1,
http://www.atmel.com/dyn/products/devices.asp?family_id=641#787

ESA-ESTEC 2003, SpaceWire Standard, ECSS-E-50-12A,
http://www.estec.esa.nl/tech/spacewire/standards/

Parkes, S. M. 1999, SpaceWire: the standard, DASIA, pp.111-116

Stephan, F., Paul, R., Uwe, L., & Timothy, P. 2004, The New SpaceWire Compliant SMCS332SpW /SMCS116SpW ASIC, DASIA, pp.88-92