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Measurement of Wall Voltage in Reset Discharge of Plasma Display Panel

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In AC plasma display, it is very important to quantify the wall voltage induced by the wall charge accumulated on the dielectric surface. If we know the quantities of the wall voltage in each period of every sequence; reset period, address period and sustain period, then it helps us to design the optimal driving waveform for high efficiency plasma display. The purpose of this study is to experimentally investigate the exact wall voltage profiles at each period of every sequence and then provide the basic data to driving sequence designer. We develop a new method to measure the wall voltage with VDS (Versatile Driving Simulator) system. The wall voltage has been experimentally measured at the reset period by this new method. The reset period in driving sequence of plasma display plays an important role in improvement of the display quality. All unit cells in panel is initialized and is settled to have same amount of wall charge in reset period of driving sequence, and stable initialization of wall charge state for all cells can improve the accuracy of writing discharge in address period. It is very important to know the wall voltage quantity and wall charge state for design of the optimal reset driving waveform, which enables perfect initialization.

[References]

[1] E. H. Choi *et al*, Jpn. J. Appl. Phys. 38(1999) 6073

[2] T. S. Cho *et al*, Jpn. J. Appl. Phys. 39(2000) 4176

[3] J. J. Ko *et al*, Jpn. J. Appl. Phys. 39(2000) 28