Design and Simulation of an RSFQ 1-bit ALU

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We have designed and simulated an 1-bit ALU (Arithmetic Logic Unit) by using a half adder. An ALU is the part of a computer processor (CPU) that carries out arithmetic and logic operations on the operands in computer instruction words. The designed ALU had limited operation functions of OR, AND, XOR, and ADD and had a pipeline structure. We constructed an 1-bit ALU by using a half adder and three control switches. We designed the control switches in two ways, dc switch and NDRO (Non Destructive Read Out) switch. We used dc switches because they were simple to use. NDRO pulse switches were used because they can be easily controlled by control signals of SET and RESET and show fast response time. The simulation results showed that designed circuits operate correctly and the circuit minimum margin was 27%. In this work, we used simulation tools of XIC and WRSPICE. The circuit layouts were also performed. The circuits are being fabricated.

Keywords: single flux quantum, ALU, superconductivity, NDRO, half adder